

SPECIFICATION FOR APPROVAL

() Preliminary Specification
() Final Specification

T:11 =	47 0" CVCA TET LCD
LITIO	1/ U SX(3A IFI I (3)

BUYER	LGE
MODEL	

SUPPLIER	LG.Philips LCD Co., Ltd.
*MODEL	LM170E03
SUFFIX	TLL2

^{*}When you obtain standard approval, please use the above model name without suffix

	SIGNATURE	DATE
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Please return 1 copy for your confirmation with

your signature and comments.

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Ver 1.0 Jan. 22, 2007 1 / 28



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RECORD OF REVISIONS

Revision No	Date	Page	Description
Ver 0.1	Dec. 12, 2006		Preliminary Specification
Ver 1.0	Jan. 22, 2007	Page 4	Update For Power Consumption
		Page 6	Update For Power Supply Input Current & Power Consumption
		Page 12	Update For Signal Timing Specification : Hsync Max Timing (952 → 1022)
		Page 15	Update For Power Sequence : T3 Min. (500ms → 200ms) : T6 Max. (10ms → 2000ms)
			Final Specification

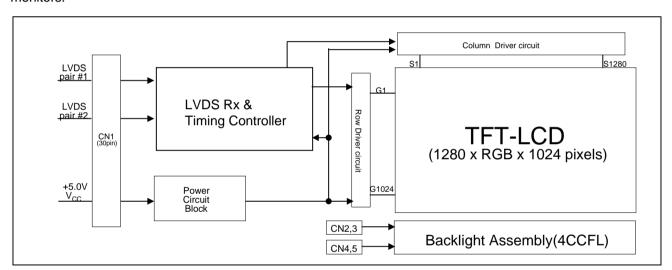


1. General Description

The LM170E03-TLL2 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has a 17.0 inch diagonal measured active display area with SXGA resolution(1024 vertical by 1280 horizontal pixel array) Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16.7M colors with A-FRC(Advanced-Frame Rate Control).

The LM170E03-TLL2 has been designed to apply the interface method that enables low power, high speed,low EMI. FPD Link or compatible must be used as a LVDS(Low Voltage Differential Signaling) chip.

The LM170E03-TLL2 is intended to support applications where thin thickness, wide viewing angle, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LM170E03-TLL2 characteristics provide an excellent flat panel display for office automation products such as monitors.



[Figure 1] Block diagram

General Features

Active screen size	17.0 inch (43.27cm) diagonal
Outline Dimension	358.5(H) x 296.5(V) x 16.0(D) mm(Typ.)
Pixel Pitch	0.264 mm x 0.264 mm
Pixel Format	1280 horiz. by 1024 vert. Pixels. RGB stripe arrangement
Display Colors	16.7M colors
Luminance, white	300 cd/m ² (Typ. Center 1 point)
Power Consumption	21.1 Watts(Typ.)
Weight	1600g (Typ.)
Display operating mode	Transmissive mode, normally white
Surface treatments	Hard coating (3H), Anti-glare treatment of the front polarizer



2. Absolute maximum ratings

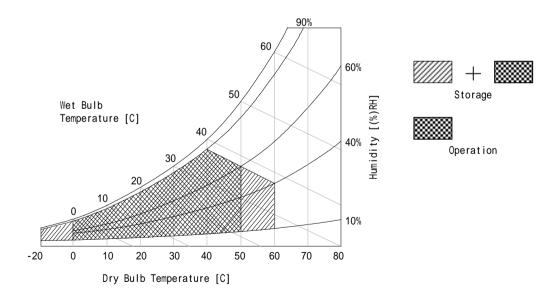
The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. Absolute Maximum Ratings

Doromotor	Cumbal	Valu	ıes	Unito	Notes
Parameter	Symbol	Min.	Max.	Units	Notes
Power Supply Input Voltage Operating Temperature Storage Temperature Operating Ambient Humidity Storage Humidity	V_{CC} T_{OP} T_{ST} H_{OP} H_{ST}	- 0.3 0 - 20 10 10	+ 5.5 + 50 + 60 + 90 + 90	V _{dc} %RH %RH	At 25 1 1 1 1

Note: 1. Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39 °C Max, and no condensation of water.



[Figure 2] Temperature and relative humidity

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Hrs

8



Product Specification

3. Electrical specifications

Life Time

3-1. Electrical characteristics

The LM170E03-TLL2 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. Another which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. Electrical Characteristics

Parameter	Symbol	Values			Units	Notes
Parameter	Зуньон	Min.	Тур.	Max.	Ullits	Notes
MODULE :						
Power Supply Input Voltage	V_{CC}	4.5	5.0	5.5	V	
Permissive Power Input Ripple	V_{RF}	-	-	0.1	V	
Power Supply Input Current	I _{CC}	-	640	740	mA	1
Differential Impedance	Zm	90	100	110	ohm	
Power Consumption	P_{C}	-	3.2	3.7	Watts	
Rush Current	I _{RUSH}	-	2.0	3.0	Α	2
LAMP for each CCFL:						
Operating Voltage	V_{BL}	628	640	740	V_{RMS}	3
		(@7.5mA)	(@7.0mA)	(@3.0mA)	Tavio	
Operating Current	I_BL	3.0	7.0	7.5	mA_RMS	
Established Starting Voltage	V_{BS}					4
at 25 °C		-	-	1000	V_{RMS}	
at 0 °C		-	-	1250	V_{RMS}	
Operating Frequency	f_{BL}	40	60	70	kHz	5
Discharge Stabilization Time	T_S	-	-	3	Minutes	6
Power Consumption	P_BL	-	17.90	19.70	Watts	7

Note. The design of the inverter must have specifications for the lamp in LCD Assembly.

The performance of the Lamp in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC Inverter. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter(no lighting, flicker, etc) never occurs. When you confirm it, the LCD Assembly should be operated in the same condition as installed in your instrument.

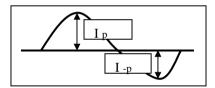
Note. Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.

50,000

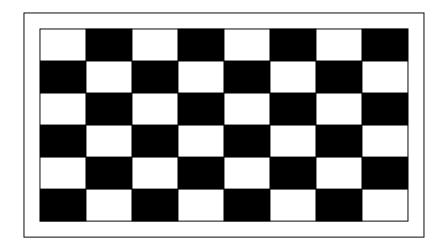
- 1. The specified current and power consumption are under the V_{CC}=5.0V, 25°C, f_V(frame frequency) =60Hz condition. Mosaic(black & white) pattern shown in the [Figure 3] is displayed.
- 2. The duration of rush current is about 5ms. And V_{CC} rise time is 500us \pm 20%.
- Operating voltage is measured under 25 .The variance of the voltage is ± 10%.
- 4. The voltage above V_{BS} should be applied to the lamps for more than 1 second for start-up. Otherwise, the lamps may not be turned on.



- 5. The output of the inverter must have symmetrical(negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interference with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away as possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.
- Let's define the brightness of the lamp after being lighted for 5 minutes as 100%.
 T_s is the time required for the brightness of the center of the lamp to be not less than 95%.
 The used lamp current is the lamp typical current.
- 7. The lamp power consumption shown above does not include loss of external inverter under 25. The used lamp current is the lamp typical current.
- 8. The life time is determined as the time at which brightness of lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2 .
- Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp.
 - It shall help increase the lamp lifetime and reduce its leakage current.
 - a. The unbalance rate of the inverter waveform should be 10% below;
 - b. The distortion rate of the waveform should be within $2 \pm 10\%$;
 - c. The ideal sine wave form shall be symmetric in positive and negative polarities.



- * Asymmetry rate = $|I_p I_{-p}| / I_{rms}$ * 100%
- * Distortion rate = I_p (or I_{-p}) / I_{rms}
- 10. Inverter open voltage must be more than lamp starting voltage.
- 11. The inverter which is combined with this LCM, is highly recommended to connect coupling(ballast) condenser at the high voltage output side. When you use the inverter which has not coupling(ballast) condenser, it may cause abnormal lamp lighting because of biased mercury as time goes.



[Figure 3] Mosaic pattern for power consumption measurement



3-2. Interface Connections

LCD Connector(CN1): AL230R-ALG1D-P (Manufactured by P-TWO)

or KDF71G-30S-1H (Manufactured by HIROSE)

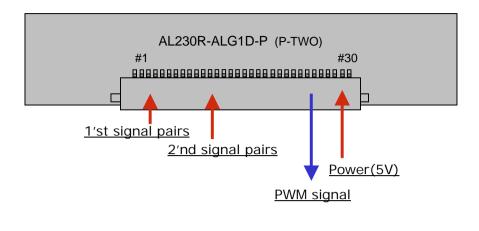
or FI-X30SSL-HF (Manufactured by JAE) or GT103-30S-H23-M (Manufactured by LSC)

Mating Connector: FI-X30H and FI-X30HL (manufactured by JAE) or equivalent

Table 3. Module connector pin configuration

Pin No	Symbol	Description	
1	RxO0-	LVDS Signal of Odd Channel 0(-)	
2	RxO0+	LVDS Signal of Odd Channel 0(+)	
3	RxO1-	LVDS Signal of Odd Channel 1(-)	
4	RxO1+	LVDS Signal of Odd Channel 1(+)	
5	RxO2-	LVDS Signal of Odd Channel 2(-)	
6	RxO2+	LVDS Signal of Odd Channel 2(+)	First Pixel Data
7	GND	Ground	
8	RxOC-	LVDS Signal of Odd Channel Clock(-)	
9	RxOC+	LVDS Signal of Odd Channel Clock(+)	
10	RxO3-	LVDS Signal of Odd Channel 3(-)	
11	RxO3+	LVDS Signal of Odd Channel 3(+)	
12	RxE0-	LVDS Signal of Even Channel 0(-)	
13	RxE0+	LVDS Signal of Even Channel 0(+)	
14	GND	Ground	
15	RxE1-	LVDS Signal of Even Channel 1(-)	
16	RxE1+	LVDS Signal of Even Channel 1(+)	
17	GND	Ground	Second Pixel Data
18	RxE2-	LVDS Signal of Even Channel 2(-)	
19	RxE2+	LVDS Signal of Even Channel 2(+)	
20	RxEC-	LVDS Signal of Even Channel Clock(-)	
21	RxEC+	LVDS Signal of Even Channel Clock(+)	
22	RxE3-	LVDS Signal of Even Channel 3(-)	
23	RxE3+	LVDS Signal of Even Channel 3(+)	
24	GND	Ground	
25	PWM_OUT	PWM_OUT signal for control burst frequence	cy of inverter
26	NC	No connection	
27	NC	No connection	
28	VCC	Power supply (5.0V Typ.)	
29	VCC	Power supply (5.0V Typ.)	
30	VCC	Power supply (5.0V Typ.)	







Rear view of LCM

[Figure 4] Connector diagram

- Notes: 1. All GND(ground) pins should be connected together and should also be connected to the LCD's metal frame.
 - 2. All V_{CC}(power input) pins should be connected together.
 - 3. All NC pins should be separated from other signal or power.
 - 4. PWM_OUT signal controls the burst frequency of a inverter. This signal is synchronized with vertical frequency, it's frequency is 3 times of vertical frequency, and it's duty ratio is 50%. If you don't use this pin, it is no connection.



Interface chip must be used LVDS, part No. SN75LVDS83 (Tx, Texas Instrument) or compatible.

Table 4. Required signal assignment for Flat Link (TI:SN75LVDS83) Transmitter

VCC	Din	Pin Pin Name Require Signal Pin Pin Name Require Signal						
2 D5 TTL Input(R7) 30 D26 TTL Input(DE) 3 D6 TTL Input(R5) 31 TxCLKIN TTL Level clock Input 4 D7 TTL Input(G0) 32 PWR DWN Power Down Input 5 GND Ground pin for TTL 33 PLL GND Ground pin for PLL 6 D8 TTL Input(G1) 34 PLL VCC Power Supply for PLL 7 D9 TTL Input(G2) 35 PLL GND Ground pin for PLL 8 D10 TTL Input(G2) 36 LVDS GND Ground pin for PLL 8 D10 TTL Input(G2) 36 LVDS GND Ground pin for PLL 9 VCC Power Supply for TTL Input 37 TxOUT3+ Positive LVDS differential data output3 10 D11 TTL Input(G3) 39 TxCLKOUT+ Positive LVDS differential clock output 11 D12 TTL Input(G4) 40 TxCLKOUT+ Positive LVDS differential data output2 14 D14 TTL Input(G5)		Pin Name	Require Signal		Pin Name	Require Signal		
3	1	VCC	Power Supply for TTL Input	29	GND	Ground pin for TTL		
4 D7 TTL Input(G0) 32 PWR DWN Power Down Input 5 GND Ground pin for TTL 33 PLL GND Ground pin for PLL 6 D8 TTL Input(G1) 34 PLL VCC Power Supply for PLL 7 D9 TTL Input(G6) 36 LVDS GND Ground pin for LVDS 8 D10 TTL Input(G6) 36 LVDS GND Ground pin for LVDS 9 VCC Power Supply for TTL Input 37 TXOUT3+ Positive LVDS differential data output3 10 D11 TTL Input(G7) 38 TXOUT3- Negative LVDS differential data output3 11 D12 TTL Input(G3) 39 TXCLKOUT- Positive LVDS differential clock output 12 D13 TTL Input(G4) 40 TXCLKOUT- Negative LVDS differential clock output 13 GND Ground pin for TTL 41 TXOUT2- Positive LVDS differential data output2 14 D14 TTL Input(B5) 42 TXOUT2- Negative LVDS differential data output2	2	D5	TTL Input(R7)	30	D26	TTL Input(DE)		
5 GND Ground pin for TTL 33 PLL GND Ground pin for PLL 6 D8 TTL Input(G1) 34 PLL VCC Power Supply for PLL 7 D9 TTL Input(G2) 35 PLL GND Ground pin for PLL 8 D10 TTL Input(G6) 36 LVDS GND Ground pin for LVDS 9 VCC Power Supply for TTL Input 37 TXOUT3+ Positive LVDS differential data output3 10 D11 TTL Input(G7) 38 TXCLKOUT- Negative LVDS differential clock output 11 D12 TTL Input(G3) 39 TXCLKOUT- Negative LVDS differential clock output 12 D13 TTL Input(G4) 40 TXCLKOUT- Negative LVDS differential clock output 13 GND Ground pin for TTL 41 TXOUT2+ Positive LVDS differential clock output 14 D14 TTL Input(G5) 42 TXOUT2- Negative LVDS differential data output2 15 D15 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS </td <td>3</td> <td>D6</td> <td>TTL Input(R5)</td> <td>31</td> <td>TxCLKIN</td> <td>TTL Level clock Input</td>	3	D6	TTL Input(R5)	31	TxCLKIN	TTL Level clock Input		
D8	4	D7	TTL Input(G0)	32	PWR DWN	Power Down Input		
7 D9 TTL Input(G2) 35 PLL GND Ground pin for PLL 8 D10 TTL Input(G6) 36 LVDS GND Ground pin for LVDS 9 VCC Power Supply for TTL Input 37 TxOUT3+ Positive LVDS differential data output3 10 D11 TTL Input(G7) 38 TxOUT3- Negative LVDS differential data output3 11 D12 TTL Input(G3) 39 TxCLKOUT+ Positive LVDS differential clock output 12 D13 TTL Input(G4) 40 TxCLKOUT- Negative LVDS differential clock output 13 GND Ground pin for TTL 41 TxOUT2+ Positive LVDS differential data output2 14 D14 TTL Input(B5) 42 TxOUT2- Negative LVDS differential data output2 15 D15 TTL Input(B0) 43 LVDS VCC Power Supply for LVDS 16 D16 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS 17 VCC Power Supply for TTL Input 45 TxOUT1+ Positive LVDS diffe	5	GND	Ground pin for TTL	33	PLL GND	Ground pin for PLL		
8 D10 TTL Input(G6) 36 LVDS GND Ground pin for LVDS 9 VCC Power Supply for TTL Input 37 TxOUT3+ Positive LVDS differential data output3 10 D11 TTL Input(G7) 38 TxOUT3- Negative LVDS differential data output3 11 D12 TTL Input(G3) 39 TxCLKOUT+ Positive LVDS differential clock output 12 D13 TTL Input(G4) 40 TxCLKOUT- Negative LVDS differential clock output 13 GND Ground pin for TTL 41 TxOUT2+ Positive LVDS differential data output2 14 D14 TTL Input(G5) 42 TxOUT2- Negative LVDS differential data output2 15 D15 TTL Input(B0) 43 LVDS VCC Power Supply for LVDS 16 D16 TTL Input(B1) 45 TxOUT1+ Positive LVDS differential data output1 18 D17 TTL Input(B7) 46 TxOUT1+ Negative LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+	6	D8	TTL Input(G1)	34	PLL VCC	Power Supply for PLL		
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D11	8	D10	TTL Input(G6)	36	LVDS GND	Ground pin for LVDS		
11 D12 TTL Input(G3) 39 TxCLKOUT+ Positive LVDS differential clock output 12 D13 TTL Input(G4) 40 TxCLKOUT- Negative LVDS differential clock output 13 GND Ground pin for TTL 41 TxOUT2+ Positive LVDS differential data output2 14 D14 TTL Input(G5) 42 TxOUT2- Negative LVDS differential data output2 15 D15 TTL Input(B0) 43 LVDS GND Ground pin for LVDS 16 D16 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS 17 VCC Power Supply for TTL Input 45 TxOUT1+ Positive LVDS differential data output1 18 D17 TTL Input(B7) 46 TxOUT1- Negative LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS	9	VCC	Power Supply for TTL Input	37	TxOUT3+	Positive LVDS differential data output3		
12 D13 TTL Input(G4) 40 TxCLKOUT- Negative LVDS differential clock output 13 GND Ground pin for TTL 41 TxOUT2+ Positive LVDS differential data output2 14 D14 TTL Input(G5) 42 TxOUT2- Negative LVDS differential data output2 15 D15 TTL Input(B0) 43 LVDS GND Ground pin for LVDS 16 D16 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS 17 VCC Power Supply for TTL Input 45 TxOUT1+ Positive LVDS differential data output1 18 D17 TTL Input(B7) 46 TxOUT0+ Positive LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL I	10	D11	TTL Input(G7)	38	TxOUT3-	Negative LVDS differential data output3		
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14 D14 TTL Input(G5) 42 TxOUT2- Negative LVDS differential data output2 15 D15 TTL Input(B0) 43 LVDS GND Ground pin for LVDS 16 D16 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS 17 VCC Power Supply for TTL Input 45 TxOUT1+ Positive LVDS differential data output1 18 D17 TTL Input(B7) 46 TxOUT0- Negative LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R1) 24 D22 TTL Input(RSVD) 53 GND Ground pin for TTL 26	12	D13	TTL Input(G4)	40	TxCLKOUT-	Negative LVDS differential clock output		
15 D15 TTL Input(B0) 43 LVDS GND Ground pin for LVDS 16 D16 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS 17 VCC Power Supply for TTL Input 45 TxOUT1+ Positive LVDS differential data output1 18 D17 TTL Input(B7) 46 TxOUT1- Negative LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24	13	GND	Ground pin for TTL	41	TxOUT2+	Positive LVDS differential data output2		
16 D16 TTL Input(B6) 44 LVDS VCC Power Supply for LVDS 17 VCC Power Supply for TTL Input 45 TxOUT1+ Positive LVDS differential data output1 18 D17 TTL Input(B7) 46 TxOUT1- Negative LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL I	14	D14	TTL Input(G5)	42	TxOUT2-	Negative LVDS differential data output2		
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18 D17 TTL Input(B7) 46 TxOUT1- Negative LVDS differential data output1 19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	16	D16	TTL Input(B6)	44	LVDS VCC	Power Supply for LVDS		
19 D18 TTL Input(B1) 47 TxOUT0+ Positive LVDS differential data output0 20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	17	vcc	Power Supply for TTL Input	45	TxOUT1+	Positive LVDS differential data output1		
20 D19 TTL Input(B2) 48 TxOUT0- Negative LVDS differential data output0 21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	18	D17	TTL Input(B7)	46	TxOUT1-	Negative LVDS differential data output1		
21 GND Ground pin for TTL Input 49 LVDS GND Ground pin for TTL 22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	19	D18	TTL Input(B1)	47	TxOUT0+	Positive LVDS differential data output0		
22 D20 TTL Input(B3) 50 D27 TTL Input(R6) 23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	20	D19	TTL Input(B2)	48	TxOUT0-	Negative LVDS differential data output0		
23 D21 TTL Input(B4) 51 D0 TTL Input(R0) 24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	21	GND	Ground pin for TTL Input	49	LVDS GND	Ground pin for TTL		
24 D22 TTL Input(B5) 52 D1 TTL Input(R1) 25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	22	D20	TTL Input(B3)	50	D27	TTL Input(R6)		
25 D23 TTL Input(RSVD) 53 GND Ground pin for TTL 26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	23	D21	TTL Input(B4)	51	D0	TTL Input(R0)		
26 VCC Power Supply for TTL Input 54 D2 TTL Input(R2) 27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	24	D22	TTL Input(B5)	52	D1	TTL Input(R1)		
27 D24 TTL Input(HSYNC) 55 D3 TTL Input(R3)	25	D23	TTL Input(RSVD)	53	GND	Ground pin for TTL		
	26	vcc	Power Supply for TTL Input	54	D2	TTL Input(R2)		
28 D25 TTL Input(VSYNC) 56 D4 TTL Input(R4)	27	D24	TTL Input(HSYNC)	55	D3	TTL Input(R3)		
	28	D25	TTL Input(VSYNC)	56	D4	TTL Input(R4)		

Notes: 1. Refer to LVDS Transmitter Data Sheet for detail descriptions.

2. 7 means MSB and 0 means LSB at R,G,B pixel data



The backlight interface connector is a model 35001HS-02LD(YEONHO).

The mating connector part number is 35001WR-02L or equivalent.

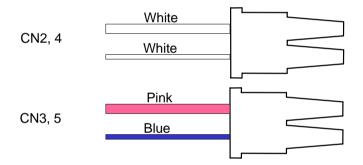
The pin configuration for the connector is shown in the table 5.

Table 5. Backlight connector pin configuration

Pin	Symbol	Description	Notes
1	HV	High Voltage for lamp	1
2	LV	Low Voltage for lamp	1,2

Notes: 1. The high voltage side terminal is colored white or pink. The low voltage side terminal is white or Blue.

2. The backlight ground should be common with LCD metal frame.



[Figure 5] Backlight connector view



3-3. Signal Timing Specifications

This is the signal timing required at the input of the LVDS Transmitter. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

Table 6. Timing table

	Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
D _{CLK}	Period	t _{CLK}	14.6	18.5	22.2	ns	
	Frequency	f _{CLK}	45	54	68	MHz	
Hsync	Period	t _{HP}	688	844	1022	_	Horizontal period
	Width	t _{WH}	16	56	-	t _{CLK}	should be even
Vsync	Period	t _{VP}	1032	1066	1536		
	Width	t _{VW}	2	3	24	t _{HP}	
	Frequency	f _V	50	60	76	Hz	
DE	Horizontal Valid	t _{HV}	640	640	640		
(Data Enable)	Horizontal Back Porch	t _{HBP}	16	124	-	_	
,	Horizontal Front Porch	t _{HFP}	8	24	-	t _{CLK}	
			-	-	-		
	Vertical Valid	t _{VV}	1024	1024	1024		
	Vertical Back Porch	t _{VBP}	5	38	124	4	
	Vertical Front Porch	t _{VFP}	1	1	-	t _{HP}	
		-	-	-	-		
	DE Setup Time	t _{SI}	4	-	-		For D _{CLK}
	DE Hold Time	t _{HI}	4	-	-	ns	
Data	Data Setup Time	t _{SD}	4	-	-	no	For D _{CLK}
	Data Hold Time	t _{HD}	4	-	-	ns	

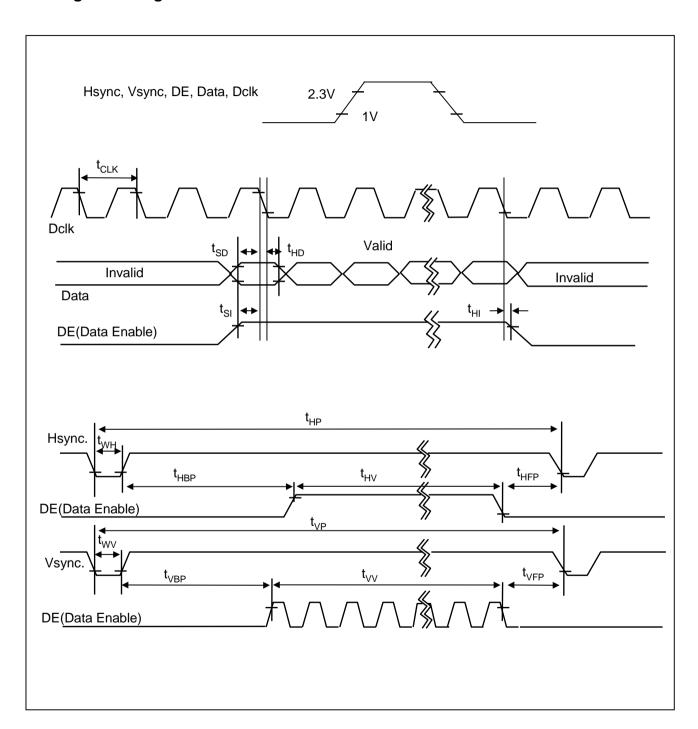
Notes: 1. DE Only mode operation

- 2. $t_{HFP} + t_{WH} + t_{HBP} < (1/2) t_{HV}$
- 3. t_{VFP} + t_{WV} + t_{VBP} < $t_{H_{max}}/t_{v_{min}}$
- 4. tHFP, tWH and tHBP should be any times of a character number (8).
- 5. No variation of the total number of Hsync and DE in a frame is required for normal operation.
- 6. No variation of the total number of clock in a Hsync period for t_{VBP} is required for normal operation.

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3-4. Signal Timing Waveforms



[Figure 6] Signal timing waveforms



3-5. Color Input Data Reference

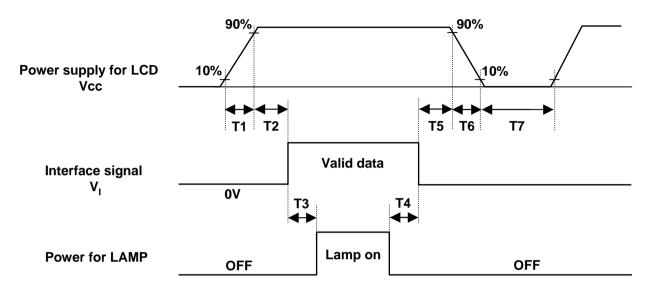
The brightness of each primary color(red,green and blue) is based on the 8-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 7. Color data reference

												Inp	ut (colo	or d	lata	l								
	Color	Red MSB					Green LSB MSB LSB						S B	Blue MSB LSB											
		R7		R5	R4	R3	R2	R1		G7	G6	G5	G4	G3	G2			B7	B6	B5	B4	ВЗ	B2	B1	В0
Basic colors	Black Red(255) Green(255) Blue(255) Cyan Magenta Yellow White	0 1 0 0 0 1 1	0 1 0 0 0 1 1	0 1 0 0 0 1 1	0 1 0 0 0 1 1	0 1 0 0 0 1 1	0 1 0 0 1 1	0 1 0 0 0 1 1	0 1 0 0 1 1	0 0 1 0 1 0 1	0 0 0 1 1 1 0	0 0 0 1 1 1 0	0 0 1 1 1 0	0 0 0 1 1 1 0	0 0 1 1 1 0	0 0 1 1 1 0	0 0 0 1 1 1 0	0 0 1 1 1 0							
Red	Red(000) dark Red(001) Red(002) : Red(253) Red(254) Red(255) bright	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 1 : 0 1	0 1 0 : 1 0 1	0 0 0 : 0 0	0 0 0 : 0 0 0	0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0
Green	Green(000)dark Green(001) Green(002) : Green(253) Green(254) Green(255)bright	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 0 0	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 1 : 0 1	0 1 0 : 1 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0
Blue	Blue(000) dark Blue(001) Blue(002) : Blue(253) Blue(254) Blue(255) bright	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 0 0	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1	0 0 0 : 1 1 1	0 0 1 : 0 1 1	0 1 0 : 1 0



3-6. Power Sequence



[Figure 7] Power sequence

Table 8. Power sequence time delay

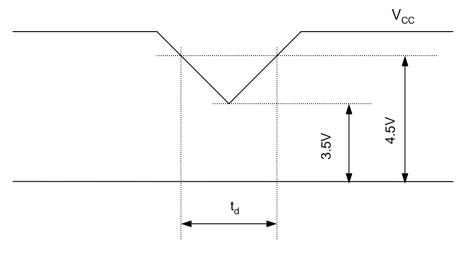
Danamatan		Values							
Parameter	Min.	Тур.	Max.	Units					
T ₁	0.5	-	10	ms					
T_2	0.01	-	50	ms					
T ₃	200	-	-	ms					
T_4	200	-	-	ms					
T ₅	0.01	-	50	ms					
T_6°	0.01	-	2000	ms					
T_7	1	-	-	s					

Notes: 1. Please avoid floating state of interface signal at invalid period.

- 2. When the interface signal is invalid, be sure to pull down the power supply for LCD $\rm V_{CC}$ to 0V.
- 3. Lamp power must be turn on after power supply for LCD and interface signals are valid.



3-7. V_{CC} Power Dip Condition



[Figure 8] Power dip condition

1) Dip condition

$$3.5V V_{CC} < 4.5V$$
, t_d 20ms

2)
$$V_{CC} < 3.5V$$

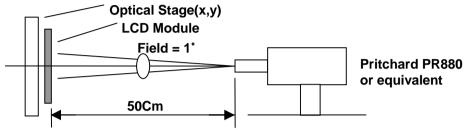
 $V_{\rm CC}$ -dip conditions should also follow the Power On/Off conditions for supply voltage.



4. Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 °C. The values specified are measured at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.

Figure. 9 presents additional information concerning the measurement equipment and method.



[Figure 9] Optical characteristic measurement equipment and method

Table 9. Optical characteristics

(Ta=25 °C, V_{CC} =5.0V, f_V =60Hz Dclk=54MHz, I_{BL} =7.0mArms)

Davan	4	Cymala al		Values		Units	Natas
Paran	neter	Symbol	Min.	Тур.	Max.	Units	Notes
Contrast ratio		CR	500	800	-		1
Surface luminance, white		L_WH	250	300	-	cd/m ²	2
Luminance uniformity		L_9	75	-	-	%	3
Response time	Response time Rise time Decay time		- -	5 1.2 3.8	10 2.4 7.6	ms	4
CIE color coordi	nates Red Green Blue White	XR YR XG YG XB YB XW YW	0.605 0.312 0.268 0.581 0.117 0.040 0.283 0.299	0.635 0.342 0.298 0.611 0.147 0.070 0.313 0.329	0.665 0.372 0.328 0.641 0.177 0.100 0.343 0.359		
X axis, Y axis,	by CR ≥ 10) right(ϕ =0°) left (ϕ =180°) up (ϕ =90°) down (ϕ =270°)	θr θl θu θd	70 70 60 70	80 80 75 85		degree	5
X axis, Y axis,	by $CR \ge 5$) right(ϕ =0°) left (ϕ =180°) up (ϕ =90°) down (ϕ =270°)	θr θl θu θd	75 75 70 70	88 88 85 85	- - - -	degree	
Relative brightne Luminance unifo Angular depend	ormity -		-	-	1.7		6 Figure 10



Notes: 1. Contrast ratio(CR) is defined mathematically as:

Surface luminance with all white pixels

Contrast ratio =

Surface luminance with all black pixels

- Surface luminance is the center point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see [Figure 10].
 When I_{BI} =6.5mA, L_{WH}=250cd/m²(Min.) 300cd/m²(Typ.)
- 3. The uniformity in surface luminance , L_g is determined by measuring L_{ON} at any point in test area. But the management of L_g is determined by measuring Lon at each test position 1 through 9, and then dividing the maximum L_{ON} of 9 points luminance by minimum L_{ON} of 9 points luminance. For more information see [Figure 10].

 $L_9 = Minimum (L_{ON1}, L_{ON2}, L_{ON9}) \div Maximum (L_{ON1}, L_{ON2}, L_{ON9}) \times 100 (\%)$

- 4. Response time is the time required for the display to transition from white to black(Rise Time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see [Figure 11]. The sampling rate is 2,500 sample/sec.
- 5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see Figure 12.
- 6. Gray scale specification

Table 10. Gray scale

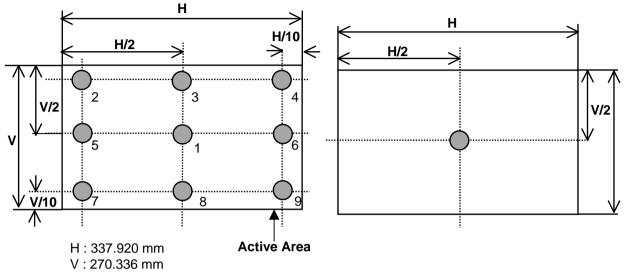
Gray level	Luminance(%) (Typ.)
L0	0.13
L31	1.08
L63	5.10
L95	12.2
L127	22.5
L159	37.0
L191	56.9
L223	80.8
L255	100



[Figure 10] Luminance measuring point

<Measuring point for luminance variation>

<Measuring point for surface luminance>



< Luminance Uniformity - angular - dependence (L_R& T_B) >

TCO '03 Luminance uniformity – angular dependence, is the capacity of the VDU to present the same luminance level independently of the viewing direction. The angular-dependent luminance uniformity is calculated as the ratio of maximum luminance to minimum luminance in the specified measurement areas.

0.

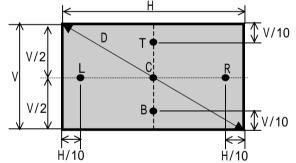
Test pattern: 80% white pattern

Test point: 2-point

Test distance : D * 1.5 = 64.77cm

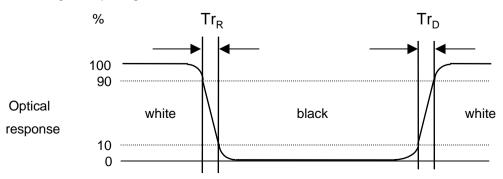
@ H,V: Active Area

$$\begin{split} \text{Test method} : L_{\text{R}} &= ((L_{\text{max.+30deg.}} \ / \ L_{\text{min. +30deg.}}) \\ &+ (L_{\text{max. -30deg.}} \ / \ L_{\text{min. -30deg.}})) \ / \ 2 \\ T_{\text{B}} &= ((L_{\text{max.+15deg.}} \ / \ L_{\text{min. +15deg.}}) \end{split}$$



[Figure 11] Response time

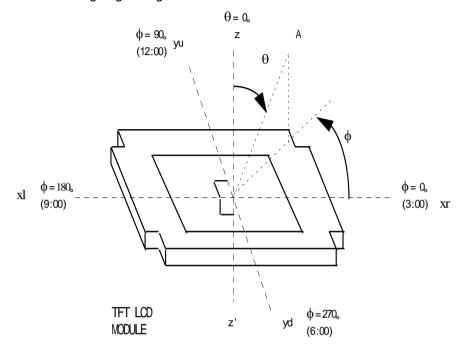
The response time is defined as the following Figure and shall be measured by switching the input signal for "black" and "white".





[Figure 12] Viewing angle

<Dimension of viewing angle range>





5. Mechanical Characteristics

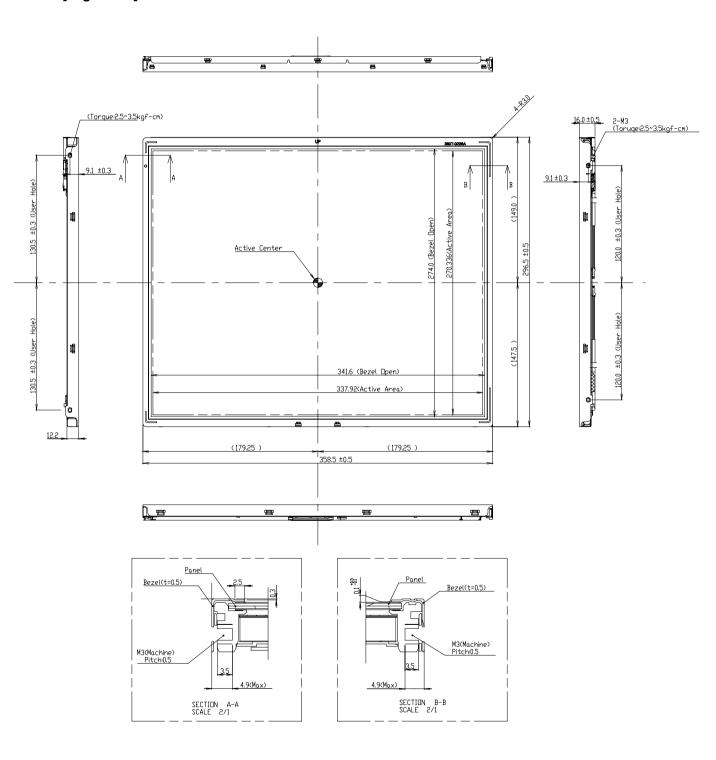
Table 11. provides general mechanical characteristics for the model LM170E03-TLL2. Please refer to Figure 13,14 regarding the detailed mechanical drawing of the LCD.

Table 11. Mechanical characteristics

	Horizontal	358.5 ± 0.5mm
Outside dimensions	Vertical	296.5 ± 0.5mm
	Depth	$16.0\pm0.5\text{mm}$
Darol oros	Horizontal	341.6 ± 0.5mm
Bezel area	Vertical	274.0 ± 0.5 mm
Active display area	Horizontal	337.920mm
Active display area	Vertical	270.336mm
Weight(approximate)	1600g(Typ.),	1680g(Max.)
Surface Treatment	Hard coating(3H) Anti-glare treatment c	of the front polarizer

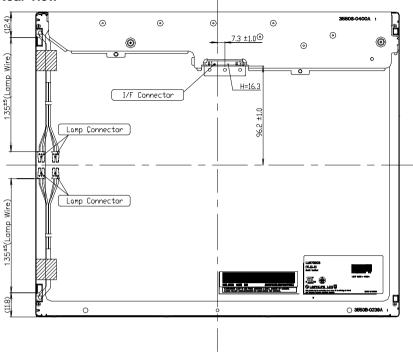


[Figure 13] Front view





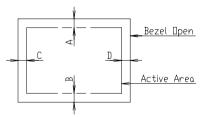
[Figure 14] Rear view



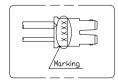
NOTES

- 1. Backlight : 4 Cold Cathode Fluorescent Lamps.
- 2. I/F Connector Specification.
- P-TWD AL230R-ALG1D-P or Equivalent.

 3. Lamp Connector Specification.
- YEDNHD 35001HS-02LD
- 4. Depth of user hole screw insertion: Max 4.9mm.
- 5. Torque of user hole: 2.5~3.5kgf-cm.
- 6. Unspecified tolerances to be \pm 0.5mm.
- 7. Tilt and partial disposition tolerance of display area as following.
 - (1) Y-Direction : A-B < 1.0
 - (2) X-Direction : C-D < 1.0



8. Lamp(CCFL) lot No. is marked at backlight connector.



9. Do not wind conductive tape around the backlight wires.



6. Reliability

Table 12. Environment test condition

No.	Test item	Conditions
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 240h 50%RH
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0G RMS Bandwidth : 10-500Hz Duration : X,Y,Z, 20 min. One time each direction
6	Shock test (non-operating)	Shock level: 120G Waveform: half sine wave, 2ms Direction: ± X, ± Y, ± Z One time each direction
7	Altitude storage / shipment	0 - 40,000 feet(12,192m)

{ Result evaluation criteria }

There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.



7. International Standards

7-1. Safety

a) UL 60950-1:2003. First Edition, Underwriters Laboratories, Inc.,

Standard for Safety of Information Technology Equipment.

b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association,

Standard for Safety of Information Technology Equipment.

c) EN 60950-1:2001. First Edition.

European Committee for Electrotechnical Standardization(CENELEC)

European Standard for Safety of Information Technology Equipment.

d) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

7-2. EMC

- a) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. "American National Standards Institute(ANSI), 1992
- b) C.I.S.P.R. "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special Committee on Radio Interference.
- c) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization.(CENELEC), 1998 (Including A1: 2000)



8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

А	В	С	D	E	F	G	Н	I	J	K	L	М
---	---	---	---	---	---	---	---	---	---	---	---	---

A,B,C : SIZE(INCH) D : YEAR

E: MONTH $F \sim M$: SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	Α	В	С

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module. This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box: 10pcs

b) Box size: 410mm X 323mm X 423mm



9. Precautions

Please pay attention to the following when you use this TFT LCD module.

9-1. Mounting Precautions

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force(ex. twisted stress) is not applied to the module.
 - And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach a transparent protective plate to the surface in order to protect the polarizer.

 Transparent protective plate should have sufficient strength in order to the resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not describe because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are determined to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)
- (2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
 And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
- (7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can not be operated its full characteristics perfectly.
- (8) A screw which is fastened up the steels should be a machine screw (if not, it causes metal foreign material and deal LCM a fatal blow)



9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.

 It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

- (1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the Bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the Bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.