SPECIFICATIONS No.06TLM743	ISSUE:Jan.12.2007

To: Lite On Technology Corporation

Specifications for

TFT -LCD Monitor

MODEL : COM35T3137KTX

APPROVED BY	
Signature	:
Name	:
Section	:
Title	:
Date	:

CASIO

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REVISIONS

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Aug.7.2006		-	First issue.
Oct.20.2006	P.6	Addition	Barcode label on S case C at Outward Form
	P.7	Addition	Distinction of barcode label
△A X4	P.9	Addition	The course of selection the connector
	P.44	Addition	Barcode label on Packing outer carton
Jan.12.2007	P.6	Change	The specification of the Label.
	P.40	Addition	Ditail drawing of 11.1 appearance specification.
△B X5	P.40	Change	Ndfilter 1%→5%
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	P.41	Addition	Ditail drawing of touch panel swell.

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1.APPLICATIONS

These specifications apply to 8.79cm(3.5inch) TFT-LCD monitor products, which are intended for civilian use.

○ As to the use of these products, and/or the use of the information and/or the drawings in these specifications, CASIO shall not guarantee or grant Lite On Technology Corporation to use or exercise an industrial right, intellectual property, or any other rights of a third party.
Therefore CASIO shall not be liable to infringement of rights of a third party by Lite On Technology Corporation arising from the use of the products.
These specifications contain CASIO's proprietary informaition that is protected by the copyright. Therefore, Lite On Technology Corporation shall treat this information with utmost care, and shall not duplicate any part of these specifications without prior permission from CASIO.

○ If these products will be used in an application where a higher level of reliability and safety is needed,in terms of function and accuracy, such as transportation equipment (aircraft,train,automobile, etc.), disaster-prevention, security equipment, or various safety equipment, Lite On Technology Corporation shall contact CASIO for technical assistance in advance.

○ These products shall not be used in critical application that requires the highest level of reliability and safety, such as aerospace equipment, main lines of telecommunications equipment, control equipment for nuclear plants, or medical life-support equipment.

○ CASIO shall not be liable for any damage arising from the misuse, abuse, and/or miss-operation of these products that do not meet with the operating conditions and precautions described in these specifications.

○ If any issues arise as to the information provided in these specifications or any other information, CASIO will discuss them with Lite On Technology Corporation in good faith and try to seek solutions or improvements.

○ CASIO shall not be obliged to burden the responsibility for destruction by static electricity broken out in your processes, such as the protection film peeling off process.

○ CASIO apply these specifications, only when carried in your company Grobal Positioning System product. When used for the other use, since CASIO do not do, please understand a guarantee entirely.

○ Complaint about non-conformance to the specifications on this document shall be notified to CASIO within six months from the date of production or three months from the date of shipment, together with return of the actual products .
After the expiration date designated above, CASIO shall have the right to reject any complaint.

2.GENERAL SPECIFICATIONS

Item	Specification	Remarks
Display type	TN type 16,777,216 Colors,transmissive mode Normally white	Back light use
Driving method	a-Si TFT Active matrix Line-scanning, Non-interlace	
Dot arrangement	RGB stripe arrangement	Refer to figure 1
Input signal type	R G B, Line inverse signal, 8 bit pararel input	
Backlight	LED sidelight	
Touch panel	Resistance type, trancemissive analog tablet	
Viewing direction	Downward (6 o'clock)	

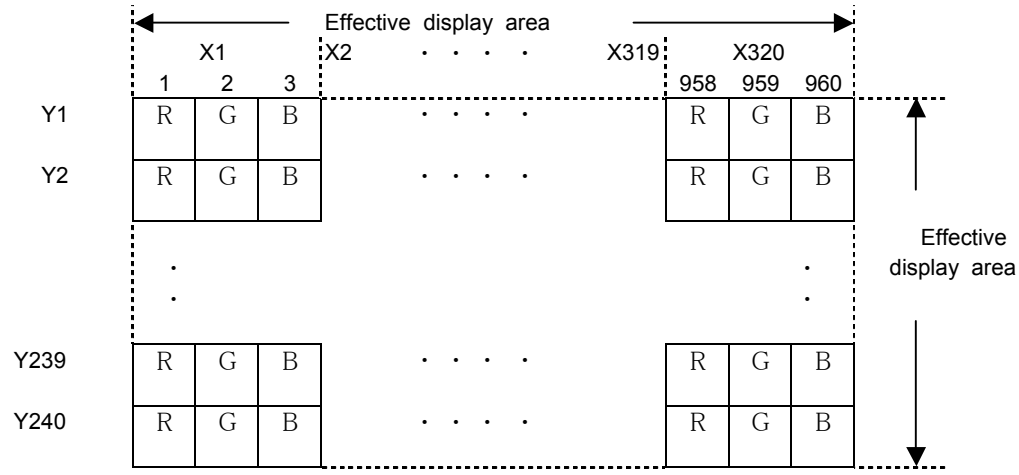

Figure 1 Dot arrangement (down for FPC CASIO logo)

3.1 DIMENSIONS

3. DIMENSIONS AND OUTWARD FORM

Item	Specification	Unit	Remarks
Module outline dimensions	76.90(H)×63.90(V)×4.53(D)	mm	Refer to 3.2 Outward Form Cable partial convex size is not included
Effective display area	70.32(H)×52.74(V)	mm	Diagonal:8.79cm
Number of dots	960(H)×240(V)	Dot	
Dot pitch	73.25(H)×219.75(V)	um	
Hardness of Touch Panel surface	2	H	It complies with the way of test method JIS K5400. However,the adding weight is set to 4.9N.
Weight	41.0	g	

EC No.	REV. No.	REVISE	DATE (Y:M:D)	APPROVED	CHECKED	PREPARED
	Ⓐx4	Add B LABEL on S CASE C	06:09:05			FUJIWARA
	Ⓐx8	The specification of the label is changed.	06:12:22			FUJIWARA

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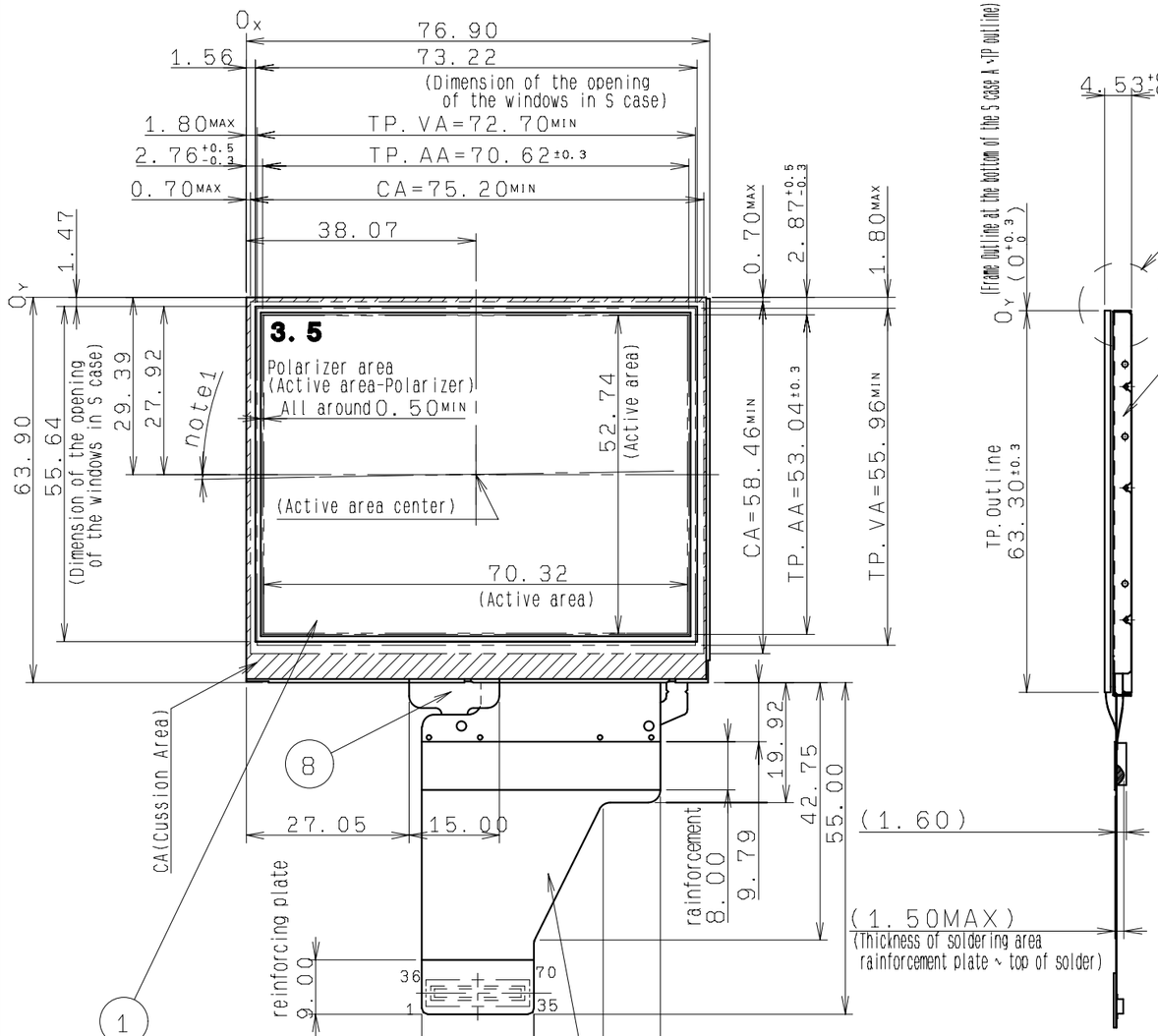
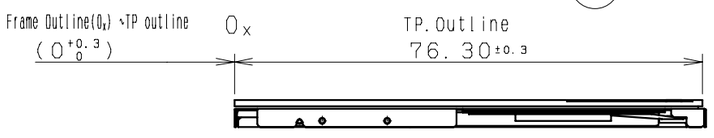
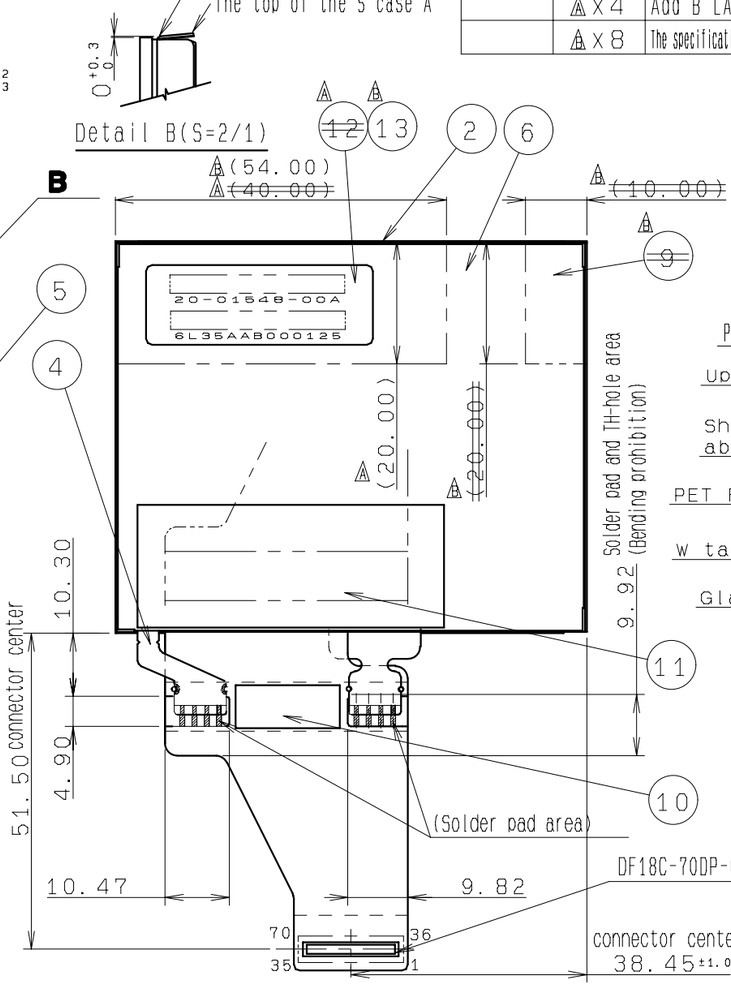
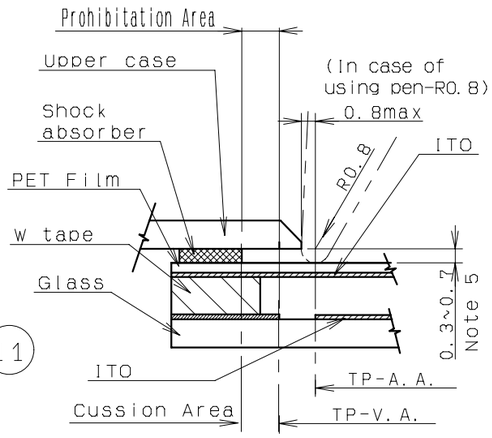
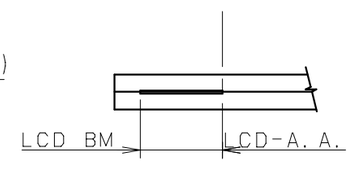
3.2 Outward Form











	PART NAME	ITEM	PART CODE	MATERIAL GRADE	REMARK
	B LABEL	Ⓐ13		Barcode standard:CODE39	(37x13x0.75t)
Ⓐ	~~B LABEL~~	~~Ⓐ12~~		Barcode standard:CODE39	(30x10x0.05t)
	PET TAPE	11			(20x45x0.05t)
	W TAPE	10		form backing	(7x17x1.6t)
Ⓐ	~~S LABEL~~	~~9~~			(10x1.85x0.075t)
	TP FPC	8			
	TOUCH PANEL	7		Film-Glass(0.7t)	
	S CASE C	6			
	S CASE A	5			
	BL FPC	4			
	FPC	3			
	S CASE B	2			
	LCD	1		Glass substrate thickness=0.5t	

Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than [±40'].

Note 2. S label is affixed the area shown in the drawing.
The thickness of the S label will be added to that of S case's surface.

Note 3. Recommended FPC connectors
For FPC(Item No.4) : HIROSE, part number: DF18C-70DP-0.4V(51) (Header)

Note 4. A.A. : Active Area of touch panel
V.A. : View Area of touch panel

Note 5. Keep a gap, for example 0.3 to 0.7mm between the bezel edge and T/P surface to avoid the bezel edge from making contacting with the T/P surface that may cause a "false touch" with the bottom layer.

APPROVED	GENERAL TOLERANCE ±0.5	SCALE 1/1(2/1.5/1)	UNIT mm
CHECKED	ISSUE (Y:M:D) 05:09:07	MODEL COM35T3137KTX	
CHECKED	NAME Specification of TFT-LCD Monitor Outer Dimensions		
DESIGN 大橋貴文			
DRAW 大橋貴文			

CASIO
CASIO COMPUTER CO., LTD.

DRAWING NO.	REV.	SHEET	DIV.
RJD507716D301			

PART 6

3.3 SERIAL LABEL(S LABEL)

1) Contents

The content of the S-label shall include the unit's place of the year (1digit), production lot month (1digit), module model code (5digits), and serial number of the module (6digits).

* Content of Characters

*	*	*****	******
a	b	c	d

	Content of Characters			
a	The unit's place of the year			
b	Production Lot (month)	Jan.-A	May.-E	Sept.-I
		Feb.-B	Jun.-F	Oct.-J
		Mar.-C	July.-G	Nov.-K
		Apr.-D	Aug.-H	Dec.-L
c	Model code	35AGX,35ASX,35ATX		
d	Serial Number			

* Example of SERIAL LABEL(S LABEL)

・In case of COM35T3137KTX (made in Japan)

6E35AGX500125

means May 2006, 3.5" AG type, X version No.500125

・In case of COM35T3137KTX (made in Malaysia)

6E35ASX500125

means May 2006, 3.5" AS type, X version No.500125

・In case of COM35T3137KTX (made in China)

6E35ATX500125

means May 2006, 3.5" AT type, X version No.500125

2) SERIAL LABEL(S LABEL) location

Refer to Subsection 3.2 Outward Form.

△A 3) Distinction of Barcode label

The original Barcode label is prepared for each model.

・HSD panel ----- Lite On P/N: 20-01548 -00A -------COM35T3137KTX

・CASIO panel ----- Lite On P/N: 20-01932 -00A -------COM35T3137KTXA

(Barcode label is sticked the products and packing outer carton.)

4.INTERFACE TERMINALS ASSIGNMENT

MODULE

No.	Symbol	Functions
1	XL	X-axis left terminal
2	YL	Y-axis lower terminal
3	XR	X-axis right terminal
4	YU	Y-axis upper terminal
5	NC	NC
6	VCOM	Common electrode signal
7	D27	Display data(B) 00H: Black D20:LSB D27:MSB Driver has internal gamma conversion.
8	D26	
9	D25	
10	D24	
11	D23	
12	D22	
13	D21	
14	D20	
15	D17	Display data(G) 00H: Black D10:LSB D17:MSB Driver has internal gamma conversion.
16	D16	
17	D15	
18	D14	
19	D13	
20	D12	
21	D11	
22	D10	
23	D07	Display data(R) 00H: Black D00:LSB D07:MSB Driver has internal gamma conversion.
24	D06	
25	D05	
26	D04	
27	D03	
28	D02	
29	D01	
30	D00	
31	BLON	Logic signal for external backlight circuit control
32	CS	Serial communication chip select (Low: Active)
33	DI	Serial communication data
34	SCK	Serial communication clock
35	VSYNC	Vertical sync signal
36	HSYNC	Horizontal sync signal
37	CLK	Clock to read display data
38	VSSA	Source driver analog circuit GND
39	VSS	Source driver logic GND
40	POCB	Power on clear (Low: Active)
41	VBC	Source driver bias setting
42	VSREF	Gamma circuit reference voltage
43	COMDC	Common electrode drive voltage
44	VDD	3V for Source driver
45	VDD2	Power supply for source driver analog circuit

No.	Symbol	Functions
46	C1P	Connection terminal 1 for capacitor for charge pump
47	C1M	Connection terminal 2 for capacitor for charge pump
48	C2M	Connection terminal 3 for capacitor for charge pump
49	C2P	Connection terminal 4 for capacitor for charge pump
50	VDD	3V for Gate driver
51	COMOUT	Square wave for common electrode drive
52	VVCOM	Voltage output for COMOUT
53	VSSA	Gate driver analog circuit GND
54	VSSP	Gate driver power circuit GND
55	VSS	Gate driver logic GND
56	C3M	Connection terminal 5 for capacitor for charge pump
57	C3P	Connection terminal 6 for capacitor for charge pump
58	C4M	Connection terminal 7 for capacitor for charge pump
59	C4P	Connection terminal 8 for capacitor for charge pump
60	VDD3	Power supply for VVCOM
61	C5M	Connection terminal 9 for capacitor for charge pump
62	C5P	Connection terminal 10 for capacitor for charge pump
63	VGH	Positive voltage for gate driver
64	C6P	Connection terminal 11 for capacitor for charge pump
65	C6M	Connection terminal 12 for capacitor for charge pump
66	VGL	Negative voltage for gate driver
67	BLL2	Backlight drive 2 (cathode side)
68	BLH2	Backlight drive 2 (anode side)
69	BLH1	Backlight drive 1 (anode side)
70	BLL1	Backlight drive 1 (cathode side)

* Please refer to the "Outline drawing" for terminal order.

* Recommended connector: HIROSE ELECTRIC Co.,ltd.DF18C-70DP-0.4V(51). This terminal uses the gilding.

⚠A This connector is specified by Lite On Technology Corporation. In case of trouble for this connector ,CASIO will discuss them with Lite On Technology Corporation.

5. ABSOLUTE MAXIMUM RATINGS

VSS=0 V

Items	Symbol	Condition	Rating MIN.	Rating MAX.	Unit	Appricable terminal
Logic Power voltage	VDD	Ta=25℃	-0.3	6.0	V	VDD
Source driver Power voltage	VDD2		-0.3	6.0	V	VDD2
	VSREF		-0.3	6.0	V	VSREF
Gate driver Power voltage	VGH		-0.3	VGL+36	V	VGH
	VGL		VGH-36	0.3	V	VGL
	VDD3		-0.3	VGL+36	V	VDD3
Logic input Voltage	VI		-0.3	VDD+0.3	V	POCB,CLK,VSYNC,HSYNC D[27:00],CS,DI,SCK
Common electrode voltage	VCOMDC		-0.3	VDD2+0.3	V	COMDC
	COMOUT		-0.3	VVCOM +0.3	V	COMOUT
	VVCOM		-0.3	VDD3 +0.3	V	VVCOM
	VCOM		-6.0	10.0	V	VCOM
			-	12.0	Vpp	
LED direction current of order	IF	Ta=25℃	-	35	mA	BLH1-BLL1 BLH2-BLL2
		Ta=70℃	-	15		
		refer to figure 2 on P.11				
Touch Panel Input Voltage	VIT		-	7.0	V	XL,XR,YU,YL
Storage temp. Range	Tstg		-20	80	℃	
Storage humidity Range	Hstg	Ta≦40℃	20	80	%	
		Ta>40℃	It is a thing without drew condensation blow in 40℃ 80%RH of the amount of moisture.			

* Please refer to the power on and off sequence in the "Standby" section of this document.

6.RECOMMENDED OPERATING CONDITIONS

VSS=0V

Item		Symbol	Condition	Rating			Unit	Applicable terminals
				MIN	TYP	MAX		
Supply voltage		VDD		2.7	3.0	3.6	V	VDD
Common electrode signal	Amplitude	VCOMPP	BRIGHT[5:0] =09h～3Fh	3.60	－	6.52	Vp-p	COMOUT
	Center voltage (Note 1)	VCOMDC	VCOMDC[5:0] =10h～34h	0.92	1.42	1.92	V	COMDC
Output amplitude for source driver (Contrast)		VSIGPP	CONTRAST[3:0] =0h～Fh	1.97	－	4.13	Vp-p	
Bias current control resistance		RBCNT		500	560	620	KΩ	VBC
Operational temperature (Note2)		Top		-10	+25	70	℃	Touch Panel surface temp.
Operational humidity Range		Hop	Ta≦30℃	20	－	80	%	
			Ta>30℃	It is a thing without drew condensation blow in 30℃ 80%RH of the amount of moisture.				

Note 1: This range indicates the most probable range for the optimal setting for VCOMDC.
It does not mean that the optimal settings for VCOMDC for all monitors will be in this range.
VCOMDC should be optimized by viewing/using the monitor.

Note 2: Acceptable Forward Current to LED is up to 15mA, when Ta=+70℃.
Do not exceed Allowable Forward Current shown on the chart below.

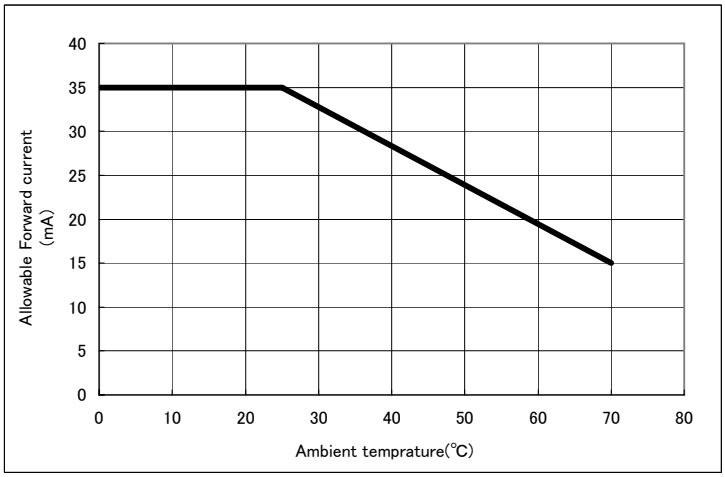


Figure 2

7. CHARACTERISTICS
7.1 DC CHARACTERISTICS

7.1.1 MODULE

If not specified, Ta=25℃,VDD=3.0V,VSS=0V,RBCNT=560KΩ

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
Schmitt input voltage	VP	VDD=2.7～3.6V	0.41× VDD	0.57× VDD	0.72× VDD	V	POCB,CS,DI,SCK CLK,VSYNC HSYNC,D[27:00]
	VN		0.20× VDD	0.40× VDD	0.50× VDD	V	
	VH		0.10× VDD	0.17× VDD	0.26× VDD	V	
Pull up resister value	Rpu		45	91	182	kΩ	POCB
Output voltage	VOH	Io = -1.0mA	VDD - 0.5	―	VDD	V	BLON
	VOL	Io = 1.0mA	0	―	0.5	V	
Current consumption	IDD	VDD=3.0V,BRIGHT[5:0]=13h CONTRAST[3:0]=7h Color bar display fCLK=6.75MHz	―	11.0	16.0	mA	VDD
Standby current	IDDs	VDD=3.0V Other input = DC fixed	―	0.0	3.0	μA	VDD

If not specified, Ta=25℃,VDD=3.0V,VSS=0V,RBCNT=560KΩ

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
Vcom Amplitude	BRIGHT	BRIGHT[5:0]=09h	6.32	6.52	6.72	Vp-p	COMOUT
		BRIGHT[5:0]=1Fh	5.13	5.33	5.53		
		BRIGHT[5:0]=3Fh	3.40	3.60	3.80		
VcomDC Adjustment value	VCOMDC	VCOMDC[5:0]=00h	0.30	0.50	0.70	V	COMDC
		VCOMDC[5:0]=1Fh	1.13	1.33	1.53		
		VCOMDC[5:0]=3Fh	2.00	2.20	2.40		
Contrast Range	CONTRAST	CONTRAST[3:0]=0h	1.87	1.97	2.07	Vp-p	
		CONTRAST[3:0]=8h	3.02	3.12	3.22		
		CONTRAST[3:0]=Fh	4.03	4.13	4.23		

7.1.2 BACKLIGHT

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
Forward current	IL25	Ta=25℃	―	15.0	35.0	mA	BLH1 － BLL1
	IL70	Ta=70℃	―	―	15.0	mA	BLH2 － BLL2
Forward voltage	VL	Ta=25℃, IL=20.0mA	―	9.6	10.5	V	

7.1.3 TOUCH PANEL

Ta=25℃

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
Linearity	LE		―	―	±1.5	%	
Insulation Resistance	RI	DC 25V	20	―	―	MΩ	XL,XR-YU,YL

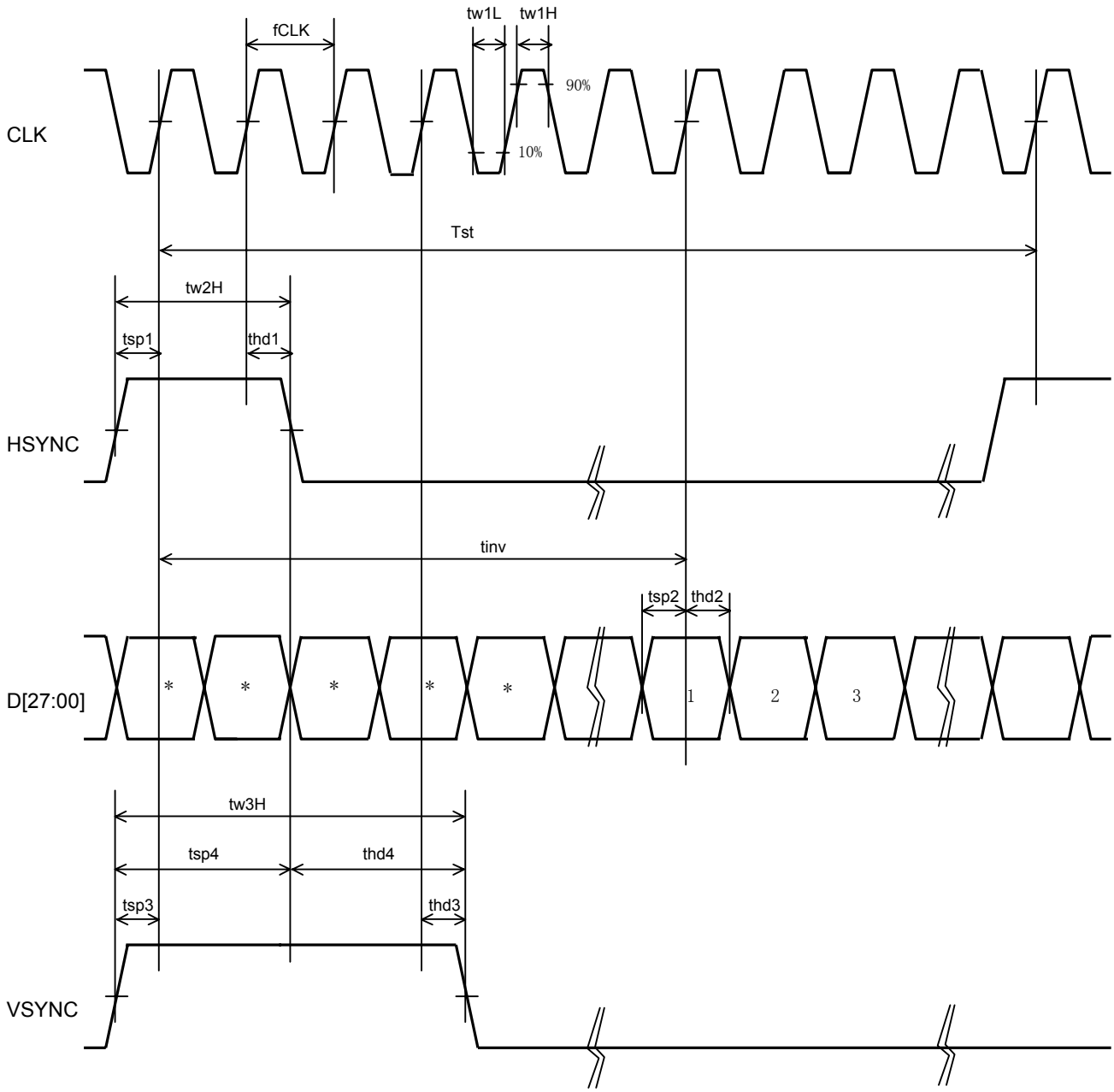
7.2 AC CHARACTERISTICS

7.2.1 DISPLAY

Common Item (If not specified, Ta=25℃,VDD=3.0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminals
			MIN	TYP	MAX		
Clock Low period	tw1L	0.1×VDD or shorter	20	—	—	ns	CLK
Clock High period	tw1H	0.9×VDD or longer	20	—	—	ns	CLK
HSYNC setup time	tsp1		10	—	—	ns	HSYNC,CLK
HSYNC hold time	thd1		10	—	—	ns	HSYNC,CLK
Data setup time	tsp2		10	—	—	ns	D[27:00],CLK
Data hold time	thd2		10	—	—	ns	
VSYNC setup time1	tsp3		10	—	—	ns	VSYNC,CLK
VSYNC hold time1	thd3		10	—	—	ns	VSYNC,CLK
HSYNC pulse width	tw2H		2CLK	—	20μs		HSYNC
VSYNC pulse width	tw3H		4CLK	1H	—		VSYNC
VSYNC setup time2	tsp4		2	—	—	CLK	VSYNC,HSYNC
VSYNC hold time2	thd4		2	—	—	CLK	VSYNC,HSYNC
VSYNC frequency	fVSYNC		50.0	54.7	60.0	Hz	VSYNC
HSYNC frequency	fHSYNC		—	13.2	—	KHz	HSYNC
Clock frequency	fCLK		—	6.75	—	MHz	CLK
HSYNC signal cycle time	Tst		—	512	—	CLK	HSYNC
Invalid data period	tinv	recommended set point	5	11	58	CLK	D[27:00],HSYNC

Switching Characteristics Wave Form

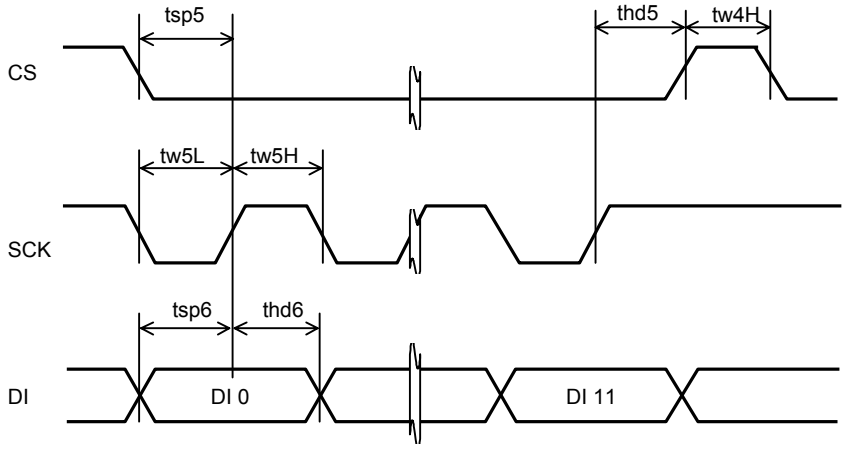


Note : Regulation between 50% of each signal amplitude

7.2.2 SERIAL COMMUNICATIONS BLOCK

(If not specified, Ta=25℃,VDD=3.0V)

Item	Symbol	Condition	Rating			Unit	Applicable Terminals
			MIN	TYP	MAX		
CS setup time	tsp5		20	–	–	ns	CS
CS hold time	thd5		20	–	–	ns	CS
DI setup time	tsp6		20	–	–	ns	DI
DI hold time	thd6		20	–	–	ns	DI
CS pulse High period	tw4H		20	–	–	ns	CS
SCK pulse Low period	tw5L		20	–	–	ns	SCK
SCK pulse High period	tw5H		20	–	–	ns	SCK



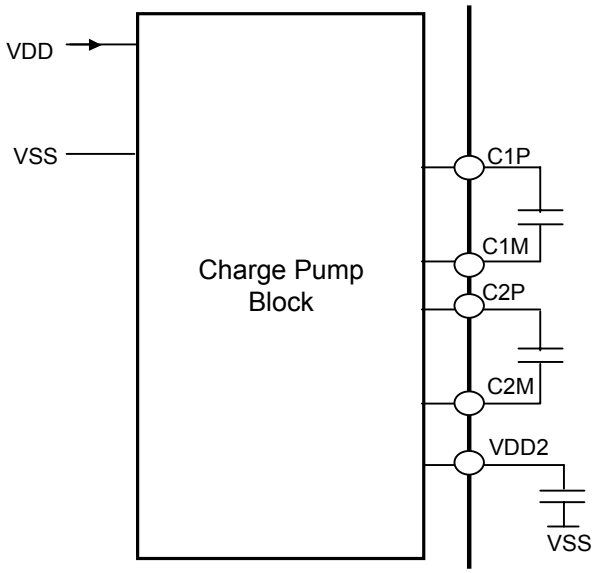
Note : Regulation between 50% of each signal amplitude

8. DESCRIPTION

8.1 POWER SUPPLY

8.1.1 VDD2 CHARGE PUMP

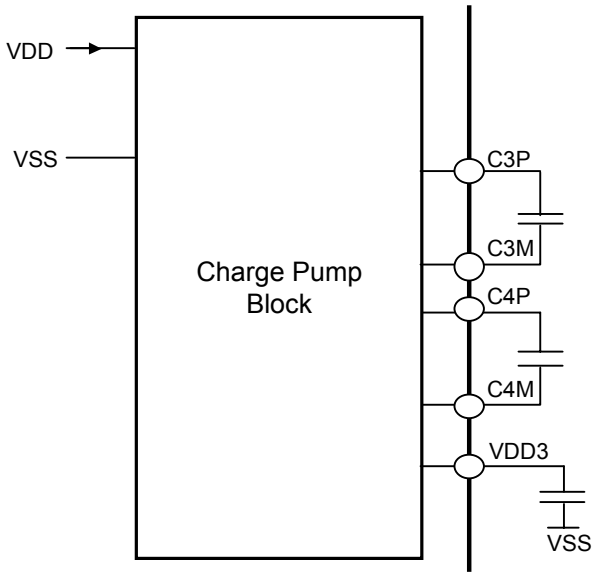
VDD2=4.8V



Use Ceramic capacitors with temperature code B.

8.1.2 VDD3 CHARGE PUMP

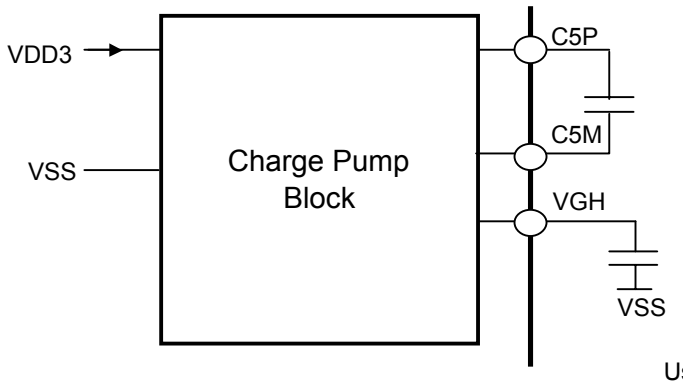
VDD3=6.9V



Use Ceramic capacitors with temperature code B.

8.1.3 VGH CHARGE PUMP

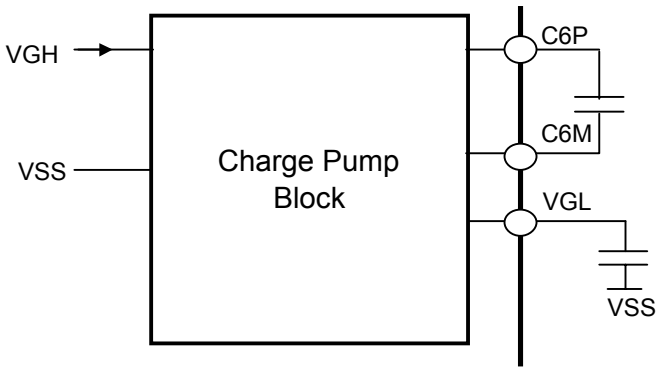
VGH=VDD3*2



Use Ceramic capacitors with temperature code B.

8.1.4 VGL CHARGE PUMP

VGL=VGH*(-1)



Use Ceramic capacitors with temperature code B.

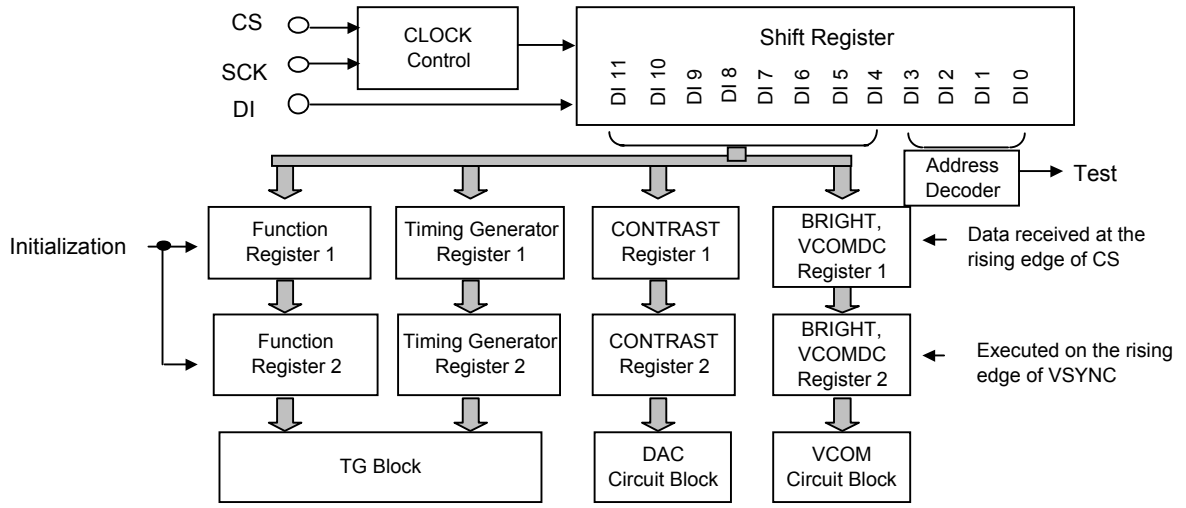
8.2 SERIAL COMMUNICATION

The following is the operational information about the serial communication control.

8.2.1 FUNCTION

Serial communication control block consists of registers which stores data that is obtained from the CS, SCK, and DI terminals. The DAC is used to generate the control voltages from the data stored in the registers.
When the power is turned on, the registers are all set to their initial values.
When register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable values, incorrect operation may occur. Since there is a possibility of causing degradation of liquid crystal etc. in case that the state is left for a long time, perform a serial communication setup as frequently as possible.

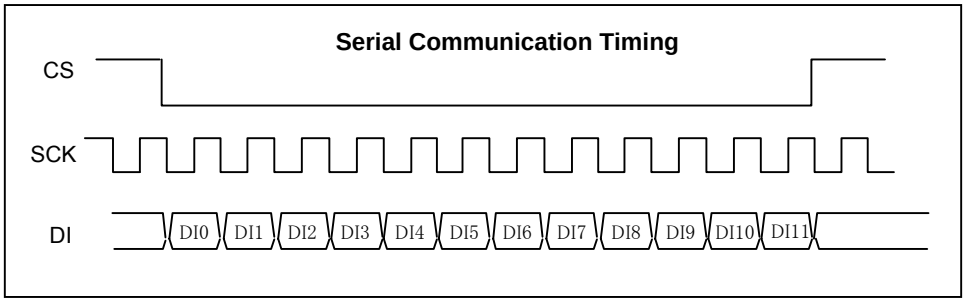
Serial Communication Control Block



8.2.2 SERIAL COMMUNICATION TIMING

On the rising edge of SCK, one of the 12 bits of serial data inputted to DI is read into the Shift Register.
On the rising edge of CS, the 12 bit serial data is decoded and is sent to appropriate control register.
If the DI data read during the low period of CS is less than 12 bits, no data is sent to the control registers.
If the DI data read during the low period of CS is more than 12 bits, the last 12 bits read is used.
The data stored in the registers are performed by VSYNC immediately after the rising edge of CS .
Since the Serial Communication block is independent from other circuitry in the monitor and runs on CLK, controls can be set at any time, regardless if the display is on or in stand-by mode.

Serial Communication Timing



8.2.3 SERIAL COMMUNICATION DATA

The configuration of serial data at DI terminal is as below.

First LSB										Last MSB
DI 0	DI 1	DI 2	DI 3	DI 4	DI 5	DI 6	DI 7	DI 8	DI 9	DI 10	DI 11
Register address				Data							

Note : DI 2=DI 3=1 is for TEST mode.

Register	Address				Resolution	Results when value increases	Initial value (LSB → MSB)								User setting value (LSB → MSB)							
	DI0	DI1	DI2	DI3			DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11	DI4	DI5	DI6	DI7	DI8	DI9	DI10	DI11
BRIGHT	0	0	0	0	6 (DI6-DI11)	Brightness becomes brighter	-	-	1	1	0	0	1	0	-	-	User setting					
VCOMDC	1	0	0	0	6 (DI6-DI11)	DC voltage becomes larger	-	-	0	1	0	0	0	1	-	-	User setting for each panel					
CONTRAST	0	1	0	0	4 (DI4-DI7)	Contrast becomes increases	0	1	1	1	-	-	-	-	User setting				-	-	-	-
PANEL1					3 (DI9-DI11)	-	-	-	-	-	-	0	0	1	-	-	-	-	-	0	0	1
VDISP	1	1	0	0	5 (DI4-DI8)	Vertical flyback time becomes longer	0	0	0	0	0	-	-	-	User setting					-	-	-
PANEL2					2 (DI10-DI11)	-	-	-	-	-	-	-	0	0	-	-	-	-	-	-	0	0
HDISP	0	0	1	0	8 (DI4-DI11)	Horizontal flyback time becomes longer	0	0	0	1	0	0	0	0	User setting							
PANEL3	1	0	1	0	8 (DI4-DI11)	-	0	1	0	0	0	0	0	1	User setting for CLK							
FUNC1	0	1	1	0	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	User setting				0	0	0
FUNC2	1	1	1	0	8 (DI4-DI11)	-	0	0	0	0	0	0	1	1	User setting				1	0	0	1	1
PANEL4	0	0	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL5	1	0	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
PANEL6	0	1	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PANEL7	1	1	0	1	8 (DI4-DI11)	-	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Configuration of FUNC1 Register

bit	Function	Detail
DI 4	TEST 0	Please set to 0.
DI 5	Up/down reverse display	0: Normal display 1: Up/down reverse display
DI 6	Right/left reverse display	0: Normal display 1: Right/left reverse display
DI 7	Backlight control	Select external backlight circuit control signal, BLON 0:Low, 1:High
DI 8	Stand-by control	0: Standby 1: Normal
DI 9	TEST 1	Please set to 0.
DI 10	TEST 2	
DI 11	TEST 3	

Configuration of FUNC2 Register

bit	Function	Detail
DI 4	HSYNC polarity	0: Positive polarity 1: Negative polarity
DI 5	VSYNC polarity	0: Positive polarity 1: Negative polarity
DI 6	CLK polarity	0: Not reverse 1: Reverse
DI 7	TEST 4	Please set to 1.
DI 8	TEST 5	Please set to 0.
DI 9	TEST 6	
DI 10	TEST 7	Please set to 1.
DI 11	TEST 8	

TEST1 ~ TEST8

Please keep DI4,DI 9~DI 11 of the FUNC1 register set to 0 at all times.
Also keep DI 8, DI 9 of the FUNC2 register set to 0 , DI 10,DI 11 set to 1 and DI 7 to 1 at all times.

User setting value

Please set up the user setting value column (PANEL1, PANEL2, FUNC1 DI 9~DI 11, FUNC2 DI 7~DI 11, PANEL4, PANEL5, PANEL6,PANEL7) as a written value.
When the appointed setting value is not set up, it does not operate normaliy.

8.2.4 FUNCTION DETAIL

8.2.4.1.Bright Control (BRIGHT)

Brightness is controlled in 64 levels by 6-bit (DI 6~DI 11) BRIGHT register.
When data value increases, VCOM amplitude becomes small and the screen becomes brighter.
It does not affect Contrast control (voltage between Black and White), which is described later.

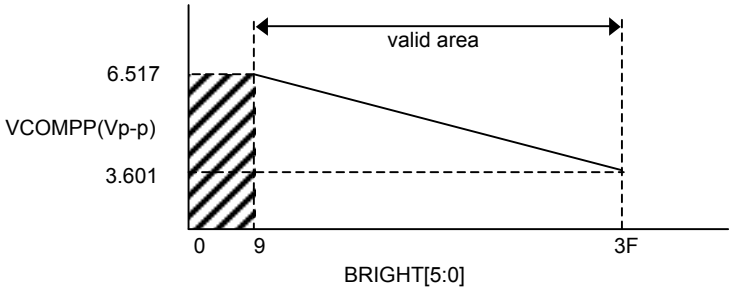
BRIGHT initial value is 5.977Vp-p.
Each increment of BRIGHT is a decrease of 54.0mv for VCOMPP.

Recommendation operation condition setup
Since the specifications state that VCOMPP voltage must be between 3.60V and 6.52V, the valid range of VCOMPP is 09h~3Fh.
Please do not set it to outside this range.

(Typ.)

BRIGHT[5:0]	VCOMPP
09h	6.517Vp-p
0Ah	6.463Vp-p
～	～
13h	5.977Vp-p
～	～
3Eh	3.655Vp-p
3Fh	3.601Vp-p

valid area



8.2.4.2.Common electrode center voltage (VCOMDC)

Common electrode center voltage(VCOMDC) is controlled in 64 level by 6-bit(Dl6-Dl11) VCOMDC register.
VCOMDC register is used to set the center voltage of the common electrode drive signal, VCOM.
When the register value increases, the voltage becomes larger.
This value has to be optimized for each TFT panel. Optimization is mandatory, or liquid crystal may degrade.

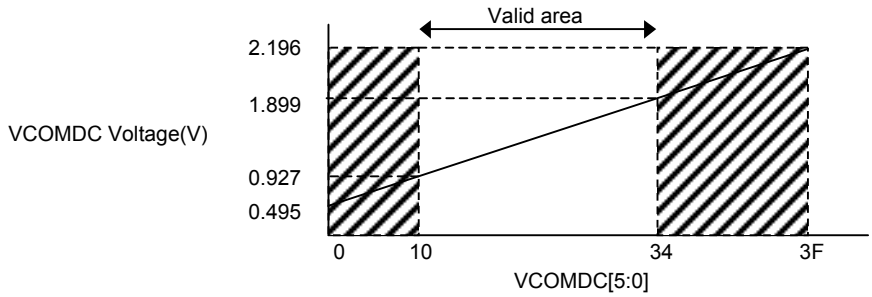
VCOMDC initial value is 1.413V
Each increment of VCOMDC is an increase of 27.0mV for VCOMDC voltage.

Recommended operation condition setup
Since the specifications state that VCOMDC voltage must be between 0.92V and 1.92V, the valid range of VCOMDC is 10h~34h.
Please do not set it to outside this range.

(Typ)

VCOMDC[5:0]	VCOMDC voltage
00h	0.495V
～	～
0Fh	0.900V
10h	0.927V
～	～
34h	1.899V
35h	1.926V
～	～
3Fh	2.196V

Valid area



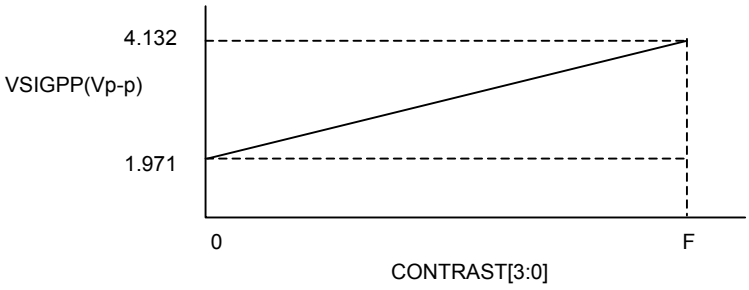
8.2.4.3.Contrast control (CONTRAST)

Contrast is controlled in 16 levels by 4-bit (DI 4~DI 7) CONTRAST register.
When data value increases, amplitude of monitor built-in DAC output becomes larger (it makes voltage larger between black and white), and contrast increases.
It does not affect Bright control, which was described earlier.

CONTRAST initial value is 3.988Vp-p
Each increment of CONTRAST is an increase of 144.0mV for VSIGPP.

(Typ)

CONTRAST[3:0]	VSIGPP
0h	1.971Vp-p
～	～
Fh	4.132Vp-p



8.2.4.4.Panel select 1 (PANEL1)

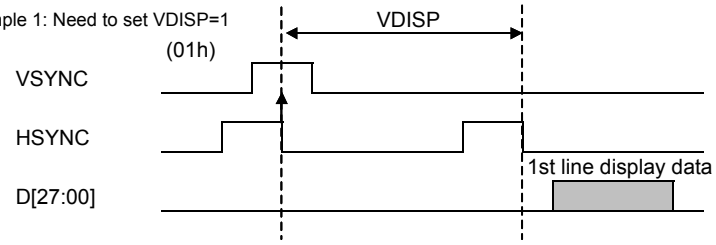
One of 8 different panel condition is selected by 3-bit (DI 9~DI 11) PANEL1 register.
Please set this register as shown below.

DI 9	DI 10	DI 11
0	0	1

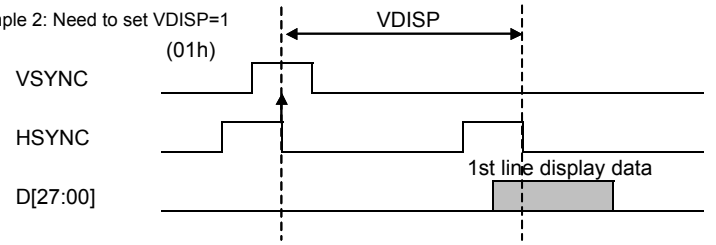
8.2.4.5.Vertical flyback time set (VDISP)

The length of a vertical flyback period can be set up to 0-31H by 5 bits of DI4-DI8 of a VDISP register.
In case of VSYNC and HSYNC are positive polarity, Hi period of VSYNC is detected at the falling edge of HSYNC.
The number of horizontal periods from the timing which detected VSYNC=Hi first to the timing into which the display data of the 1st line is inputted becomes the setting value of VDISP.
Although the display data of the 1st line is inputted before falling of HSYNC like Example 2 depending on a setup of the below-mentioned HDISP, please set up with VDISP=1 like Example 1 also in this case.
When the pulse width of VSYNC includes two or more H like Example 3, the number of horizontal periods from the timing which detected Hi period of VSYNC first to the timing into which the display data of the 1st line is inputted becomes a setting value.
An initial value is 0, and as shown in Example 3 in this case, the display data of the 1st line needs to be inputted immediately after VSYNC.
This VDISP function is effective also as a function of a vertical display range setup (Vertical position setup).
Please set up a register value to shift from the setting value set up first every 2 lines in that case.

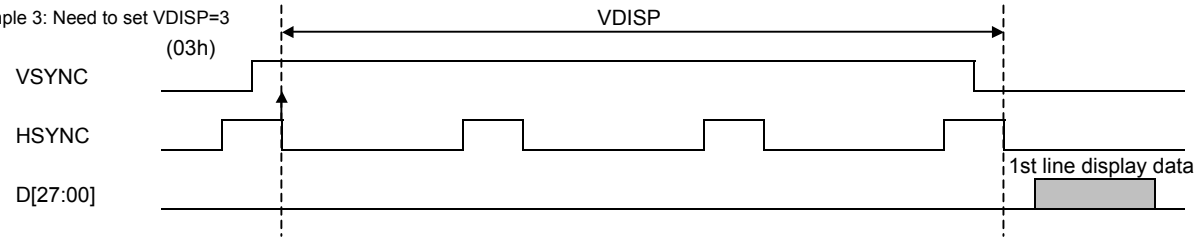
Example 1: Need to set VDISP=1



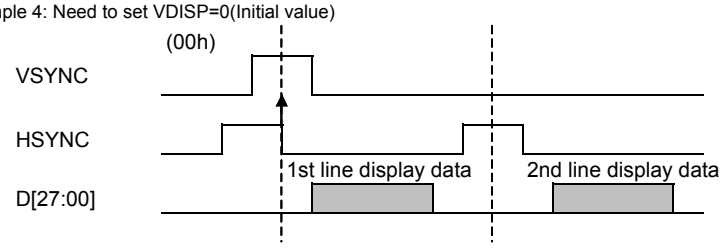
Example 2: Need to set VDISP=1



Example 3: Need to set VDISP=3



Example 4: Need to set VDISP=0(Initial value)



8.2.4.6.Panel select 2 (PANEL2)

One of 4 different panel condition is selected by 2-bit (DI 10~DI 11) PANEL2 register.
Please set this register as shown below.

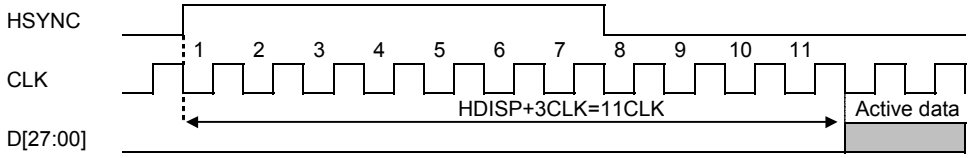
DI 10	DI 11
0	0

8.2.4.7.Horizontal flyback time set (HDISP)

The length of a horizontal flyback time can be set up to 5~258CLK by 8 bits of DI 4~DI 11 of a HDISP register.
However, the setting of value 0~1 is prohibited. Moreover, an actual flyback time serves as "setting value +3CLK."
An initial value is 8, and as shown in the following figure in this case, it starts to display from the data after 8+3CLK=11CLK from rising age of HSYNC.
Horizontal flyback time must be set between 5 and 58 CLK, due to Data invalid period spec.

This function is effective also as a function of a horizontal display area setup (horizontal position setup).

HDISP=8(08h) (Initial value)



8.2.4.8. Panel select 3 (PANEL3)

Optimize the signal drive condition by 8-bit (DI 4~DI 11) PANEL3 register.
Optimal value is defined by number of CLK in 1H period and CLK frequency as below.
If the optimal setting for PANEL3 is not set, the driver may not operate correctly and errors will occur.
Please set the optimal setting for PANEL3 before driving.

Optimal value(decimal) = (Number of CLK in 1H period - 1.0µ x CLK frequency)÷7.75

Rounding off at decimal point.

This optimal setting is strongly recommended, since panel may not work correctly if it is not optimized.

Example: fCLK=6.75MHz, 512CLK in 1H period
Optimal value(decimal) = (512-1.0µ x 6.75M)÷ 7.75 = 65(decimal) = 01000001(binary)
Panel3 register optimal setting is as below.

DI 4	DI 5	DI 6	DI 7	DI 8	DI 9	DI 10	DI 11
1	0	0	0	0	0	1	0

8.2.4.9.Function set 1 (FUNC1)

FUNC1 register selects and switches following functions.

Up/Down Reverse Display Control (Flip Image)

When DI5=0, it is Normal display mode, and when DI5=1, it is Up/down reverse display mode.
Please be aware that the input data arrangement is different between Normal display mode and Up/Down reverse display mode.
Please refer to "8.3 Display Data Transfer" in detail.
The mode is executed at VSYNC after setting serial communication.
This information is in respect to the FPC on the frame of the display being at the bottom.

Right/Left Reverse Display Mode (Mirror Image)

When DI6=0, it is Normal display mode, and when DI6=1, it is Right/left reverse display mode.
Please be aware that the input data arrangement is different between Normal display mode and Right/left reverse display mode.
Please refer to "8.3 Display Data Transfer" in detail.
The mode is executed at VSYNC after setting serial communication.

Backlight control

DI 7 value is applied to the BLON terminal, and turns the backlight driver IC ON or OFF.
Since the output levels are either VDD or VSS, this register can be used to control something other than the backlight.
The mode is executed at VSYNC.

Standby control

When DI 8=0, the module is in standby mode. When DI 8=1, the module is in normal mode.
The initial value right after applying power to the module is DI 8=0 and the module is in standby mode.
All the circuitry of the internal power circuit, timing generation circuit, LCD drive circuit, and current line are disabled in standby mode and will significantly reduce power consumption.
During standby mode, no image is displayed on the screen (white luster display) until DI 8 is set to 1 and the module switches to normal mode.
The serial communication block is operating when the module is in standby mode, and can receive serial data.
Please refer to "8.4 Standby (Power save) Sequence"
When setting it as standby mode from normal operation, image retention process is performed before becoming standby mode.

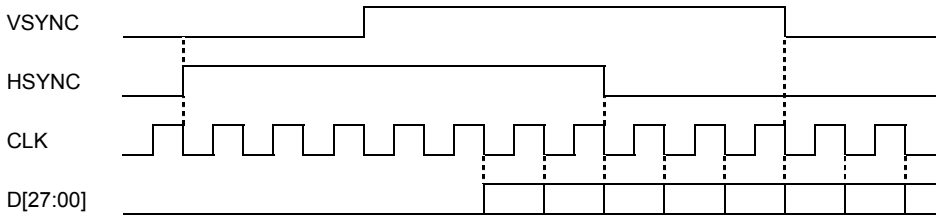
8.2.4.10. Function set 2 (FUNC2)

FUNC2 register selects and switches the following functions.

HSYNC, VSYNC, CLK polarity

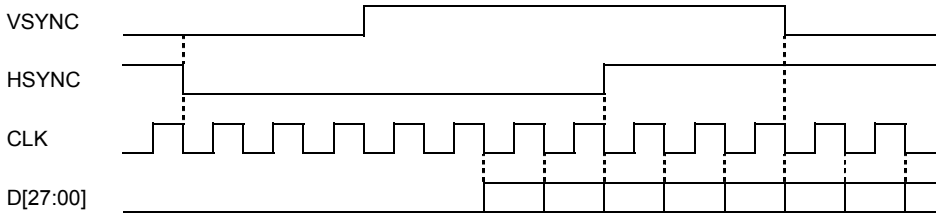
HSYNC polarity is set by DI 4. When DI 4=0, it is positive polarity. When DI 4=1, it is negative polarity.
VSYNC polarity is set by DI 5. When DI 5=0, it is positive polarity. When DI 5=1, it is negative polarity.
CLK polarity is set by DI 6. When DI 6=0, it is not reverse. When DI 6=1, it is reverse.

Initial value is DI 4=DI 5=DI 6=0, and the polarity of each signal is as below.
VSYNC, HSYNC, and display data must be change at falling edge of CLK.

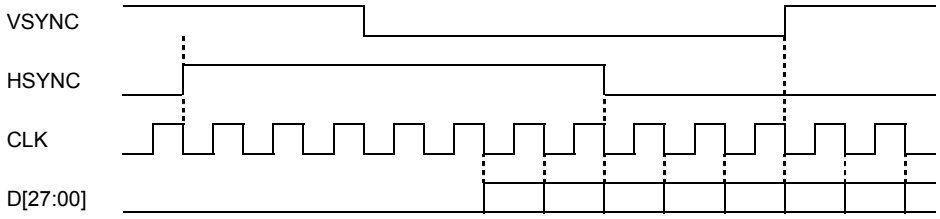


Each signal polarity is set by DI 4, DI 5, and DI 6 independently.

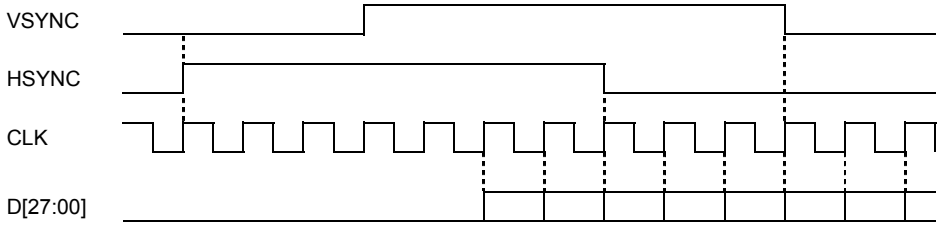
Exsample-1: DI 4=1, DI 5=DI 6=0 (HSYNC is negative polarity and Lo active.)



Exsample-2: DI 4=0, DI 5=1, DI 6=0 (VSYNC is negative polarity and Lo active.)



Exsample-3: DI 4=DI 5=0, DI 6=1 (CLK is reversed, and data is read at falling edge of CLK.)



8.2.4.11. Panel select 4 (PANEL4)

The conditions of operating in the internal signals are decided by 8-bit (DI 4~DI 11) PANEL4 register.
Please set this register as shown below.

DI 4	DI 5	DI 6	DI 7	DI 8	DI 9	DI 10	DI 11
0	0	0	0	0	0	0	0

8.2.4.12. Panel select 5 (PANEL5)

The conditions of operating in the internal signals are decided by 8-bit (DI 4~DI 11) PANEL5 register.
Please set this register as shown below.

DI 4	DI 5	DI 6	DI 7	DI 8	DI 9	DI 10	DI 11
1	0	0	0	0	0	0	0

8.2.4.13. Panel select 6 (PANEL6)

The conditions of operating in the internal signals are decided by 8-bit (DI 4~DI 11) PANEL6 register.
Please set this register as shown below.

DI 4	DI 5	DI 6	DI 7	DI 8	DI 9	DI 10	DI 11
0	0	0	0	0	0	0	0

8.2.4.14. Panel select 7 (PANEL7)

The conditions of operating in the internal signals are decided by 8-bit (DI 4~DI 11) PANEL7 register.
Please set this register as shown below.

DI 4	DI 5	DI 6	DI 7	DI 8	DI 9	DI 10	DI 11
0	1	0	0	0	0	0	0

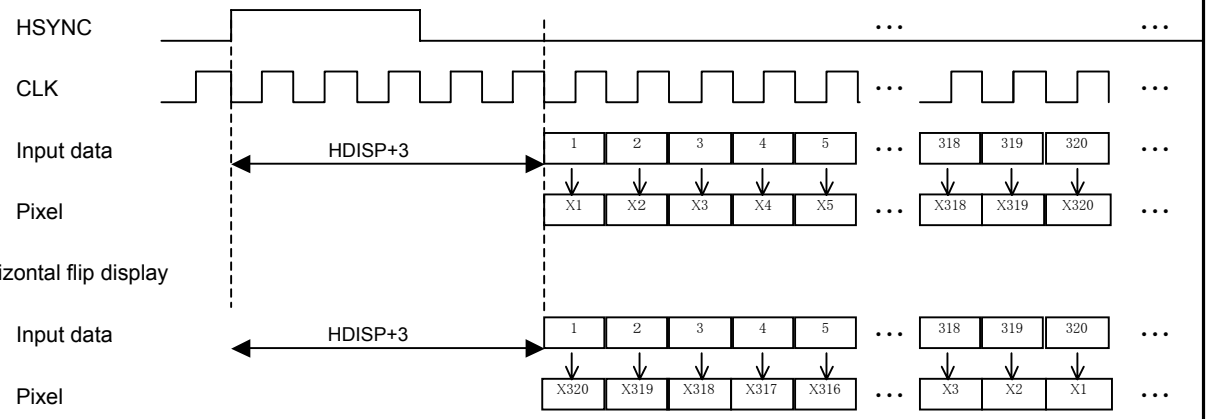
8.3 DISPLAY DATA TRANSFER

Put display data into register D[27:00]. D*0LSB、D*7:MSB

Horizontal timing and Data input order

Display data should be synchronized with CLK. CLK polarity can be selected by register D6 setting of (FUNC2).

Normal display setting ("Normal display setting" is defined as when FPC is at the bottom.)

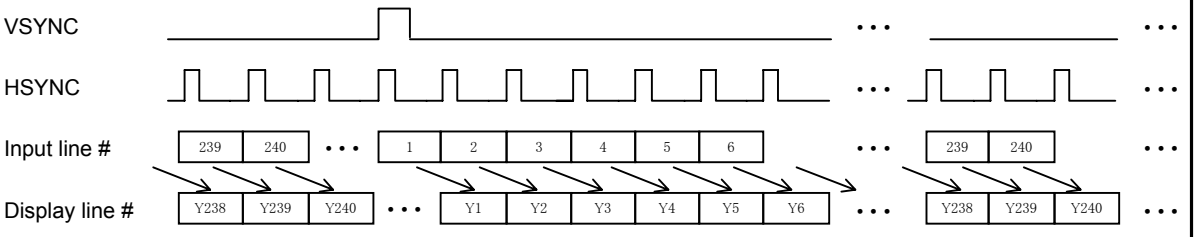


* Above chart is not an actual timing chart. This is a concept diagram to show the relation between Input data and Pixels.

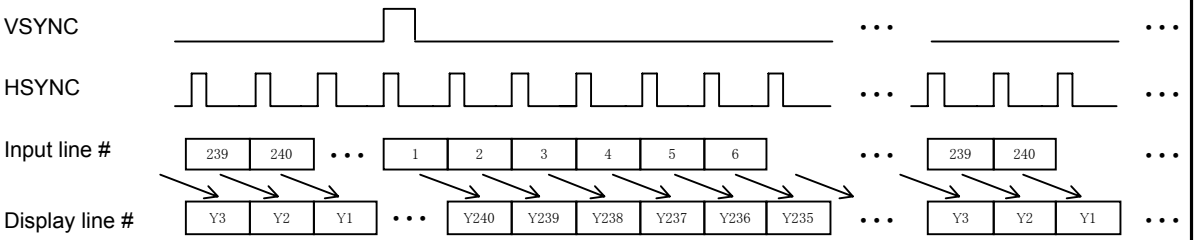
Vertical timing and Line input order

Following explanation is when transferring 240 line display data in 1field.
Relation between Input line and Display line is different when Vertically flip is used or not.

Normal display setting ("Normal display setting" is defined as when FPC is at the bottom.)



Vertically flip display



8.4. STANDBY (Power save) SEQUENCE

HSYNC, VSYNC, D00:D27, CLK, CS, DI, and SCK must be inputted simultaneously or after VDD is applied.
During standby mode, please set all input signals to a fixed DC in order to lower power consumption.
Power consumption can be further reduced by sending serial communications signals when it's required strongly.

Signals and voltages with the (*) mark in the diagram on the next page are generated inside the module and no consideration is needed for their sequence.
Please follow the recommended power on/off sequence described below:

(1) Right after turning on the power, a power-on-clear signal is generated from the POCB capacitor and the internal pull-up resister. This initializes the serial communication registers, including setting the standby control bit to 0, placing the module in standby mode.
Since LCD is in Standby mode, it is possible to save power consumption of LCD block right after turn on power.
No image is displayed on the LCD screend during this period. (white raster display)
Due to the internal power circuit being disabled during standby mode, all voltages except VDD is at 0V.
Prior to sending the serial signals for switch from standby mode to normal mode, apply to start inputting the SYNC signals and display data(HSYNC,VSYNC,D00:D27,CLK).

(2) When the serial signal to set the standby control bit to 1 is sent, the module will switch to standby release process after the next rising edge of VSYNC.
VDD will then be used to internally generate VGH, VDD2, VVCOM, and VGL.
No image will appear on the LCD display (white raster display) until after (5) field periods of VSYNC are inputted after the module switches from standby mode to normal mode.

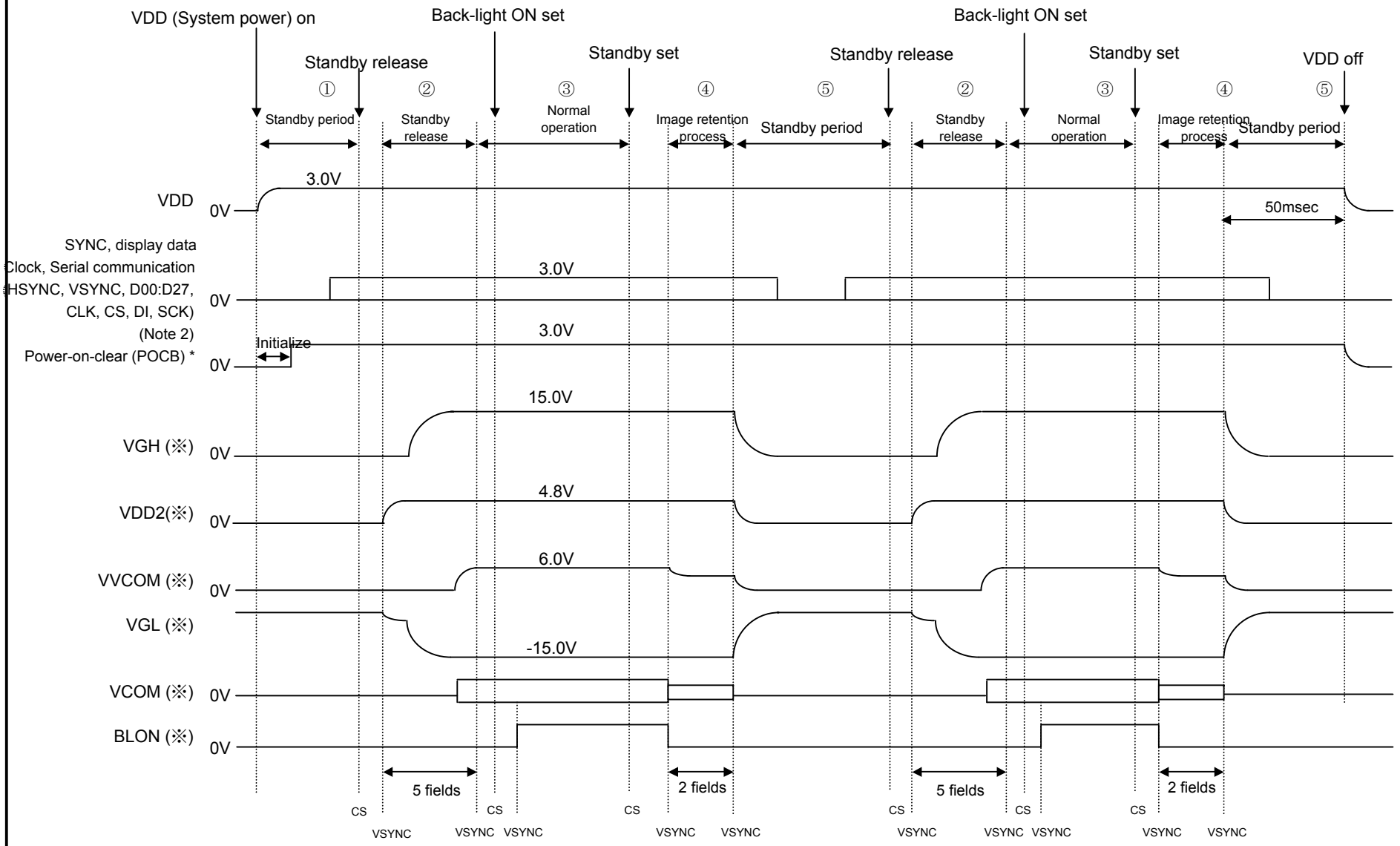
(3) LCD becomes normal display, according to the timing of VSYNC after the procedure (2) is finished.
Please turn on the backlight , after it is sure to becomes normal display
When you use the BLON terminal as a backlight comtrol ,After normal display,
backlight control bit is set to "1" by serial communications.

(4) If the standby control bit is set as 0 by serial communication, image data will serve as FFh immediately after the rising edge of CS, and image retention process will be performed from VSYNC just behind it to VSYNC after 2 fields.
By this processing, it usually changes from a display in normal operation to a white raster in an instant.
In an image retention process period, Vcom becomes the optimal amplitude for image retention process automatically.
Input SYNC signal (HSYNC, VSYNC,CLK) for this period.

(5) LCD becomes Standby mode, which is same as (1) above, at the timing of VSYNC after completion of procedure (4).
Serial communication data is stayed during standby mode. And it is possible serial communication signal and all input signals are stopped during standby mode.

(2) to (4) repeats the same processing as the above.

When you trun off power supplies, please be sure to turn it off in order of this prosedure.
Set standby mode.
Input the sync signals(HSYNC, VSYNC, CLK) until VSYNC since 2 fields after setting standby processing.
Turn off VDD after 50ms.
Stop the sync signals(HSYNC, VSYNC, CLK) between after image retention process and VDD off.



Note-1 When power is off, please make VDD to OFF after certain period 50msec after Image retention process is end.
Note-2 CLK must be supplied all the time when HSYNC, VSYNC, or Display data (D[27:00]) is sent.
Note-3 Please be aware of your power supply circuit design, since rushing in current may become larger at Standby mode release.

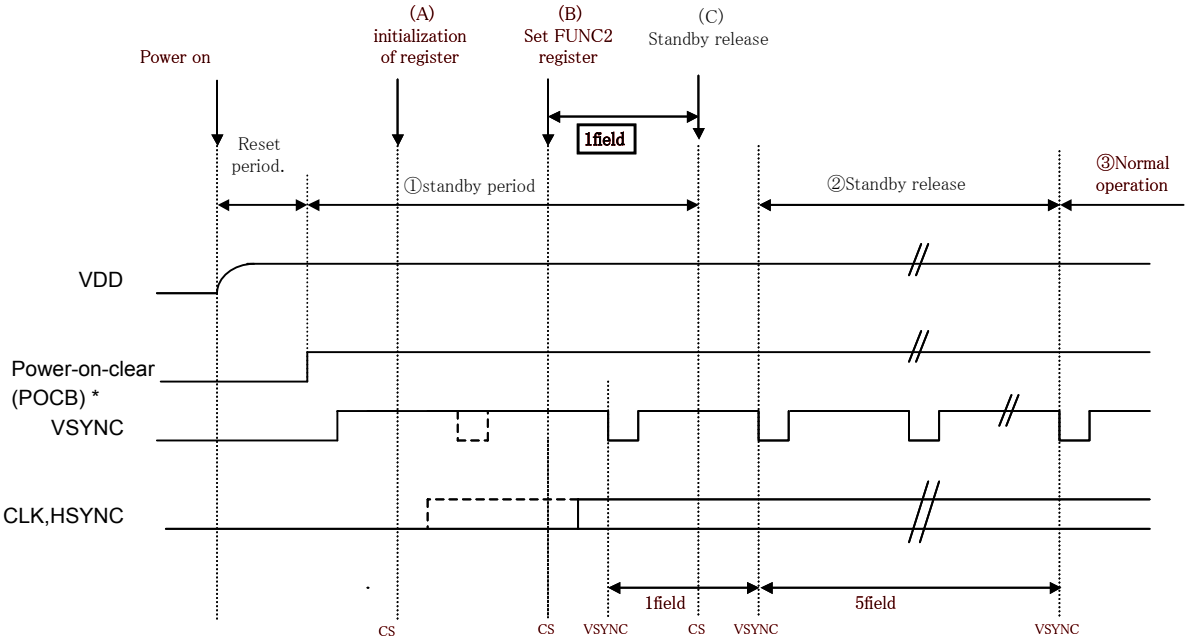
Each voltage is typ value, and not the fixed value.

Sequence of vsync polarity switch

Please follow this sequence though the polarity switch is set for the standby period when the polarity of VSYNC is used by a negative polarity

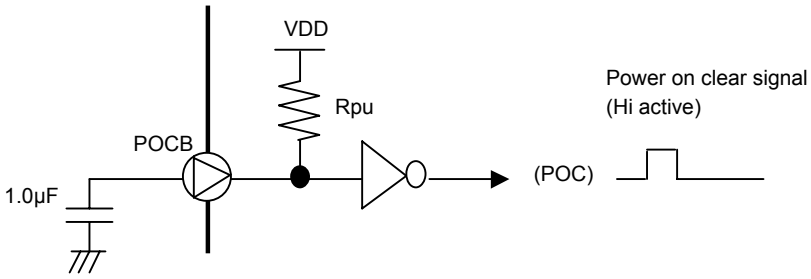
(A) At first, an initial value of the register is set by serial communications for the standby period.
(B) The func2 register is set .(VSYNC polarity switch bit = 1)
The synchronous signal(HSYNC,VSYNC,CLK) begin after this timing.(or ahead of this timing)
It takes more than one field intervals.
(C) Next, the standby release is set.(standby control bit = 1 of the func 1 register)

It is an interval between (B) and (C) to would like you to defend here.
Please give more than one field at these intervals.
Please begin the input of synchronous signal(HSYNC,VSYNC,CLK) ahead of (C).

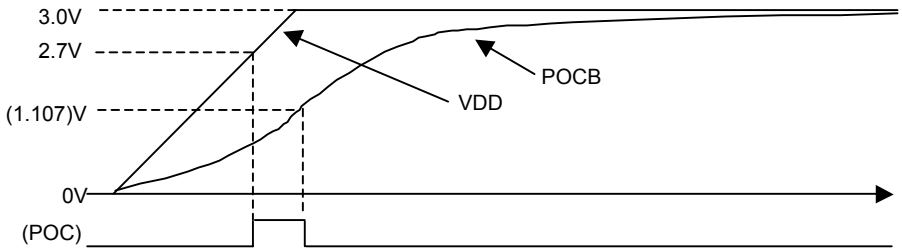


8.5 POWER ON CLEAR (POC)

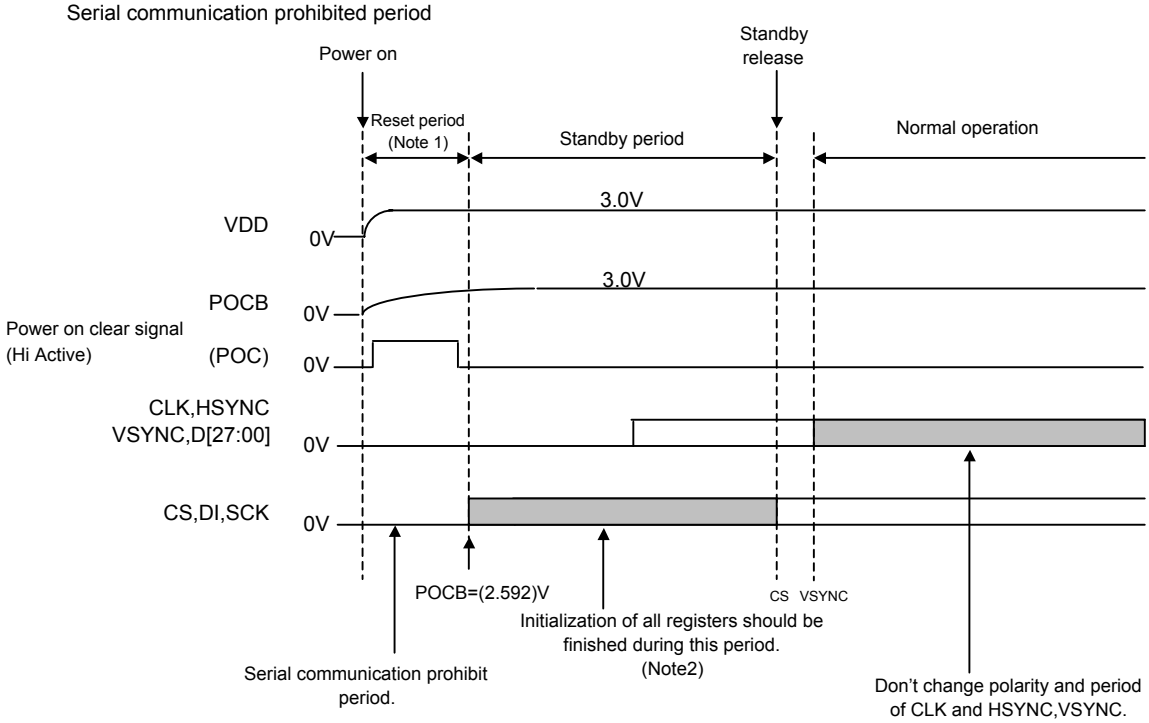
There are some restrictions concerning the power on period and the beginning of serial communication.
Power on clear circuit



The POCB terminal is connected to VDD through and internal pull-up resistor (Rpu).
When the rising time of VDD is long, the POCB waveform may be come unstable and unpredictable.
Please select an external capacitor that will keep POCB under (1.107)V when VDD is 2.7V.



Power ON Sequence
Serial communication prohibited period

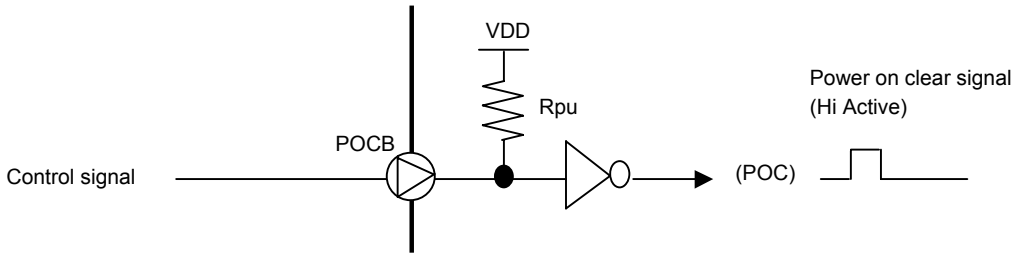


Note 1 All logic input signals are ignored during the Reset period (POC is HI
POC will switch and remain LO when POCB is between (1.107V and 2.592V

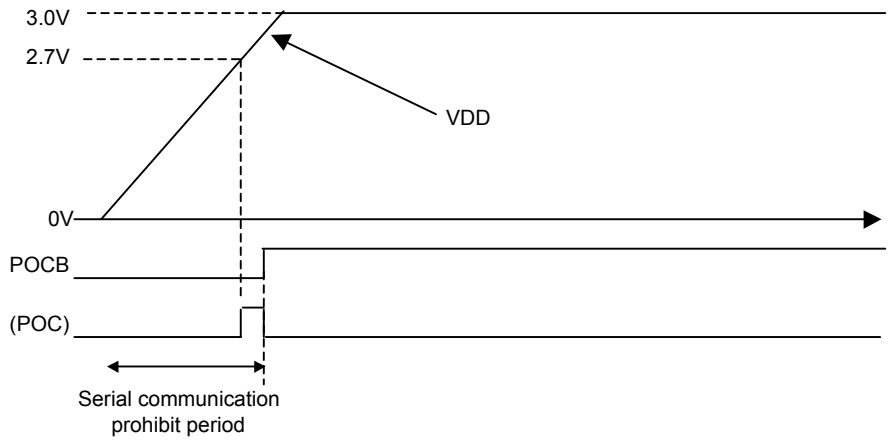
Note 2 Please refer to the vsync polarity switch sequence when you use the polarity of vsync by negative polarity.

If you wish to control the start up of this module yourself, then you should provide a control signal directly to the POCB terminal.

Power on clear circuit



If you use a control signal connected to the POCB terminal, you will need to set POCB to LO when VDD is applied.
After VDD becomes 2.7V or larger, you can switch POCB to HI.
Serial communication is prohibited while POCB is LO.



8.6 OTHER FUNCTIONS

Free-run

When HSYNC or VSYNC is not supplied for a certain period, Free-run function start automatically to avoid image retention.
With this function, HSYNC/VSYNC equivalent signal is generated on panel and white luster is displayed on LCD.
Free-run function will start at the following condition.

No HSYNC for 4096CLK period.
No VSYNC for 512H period.

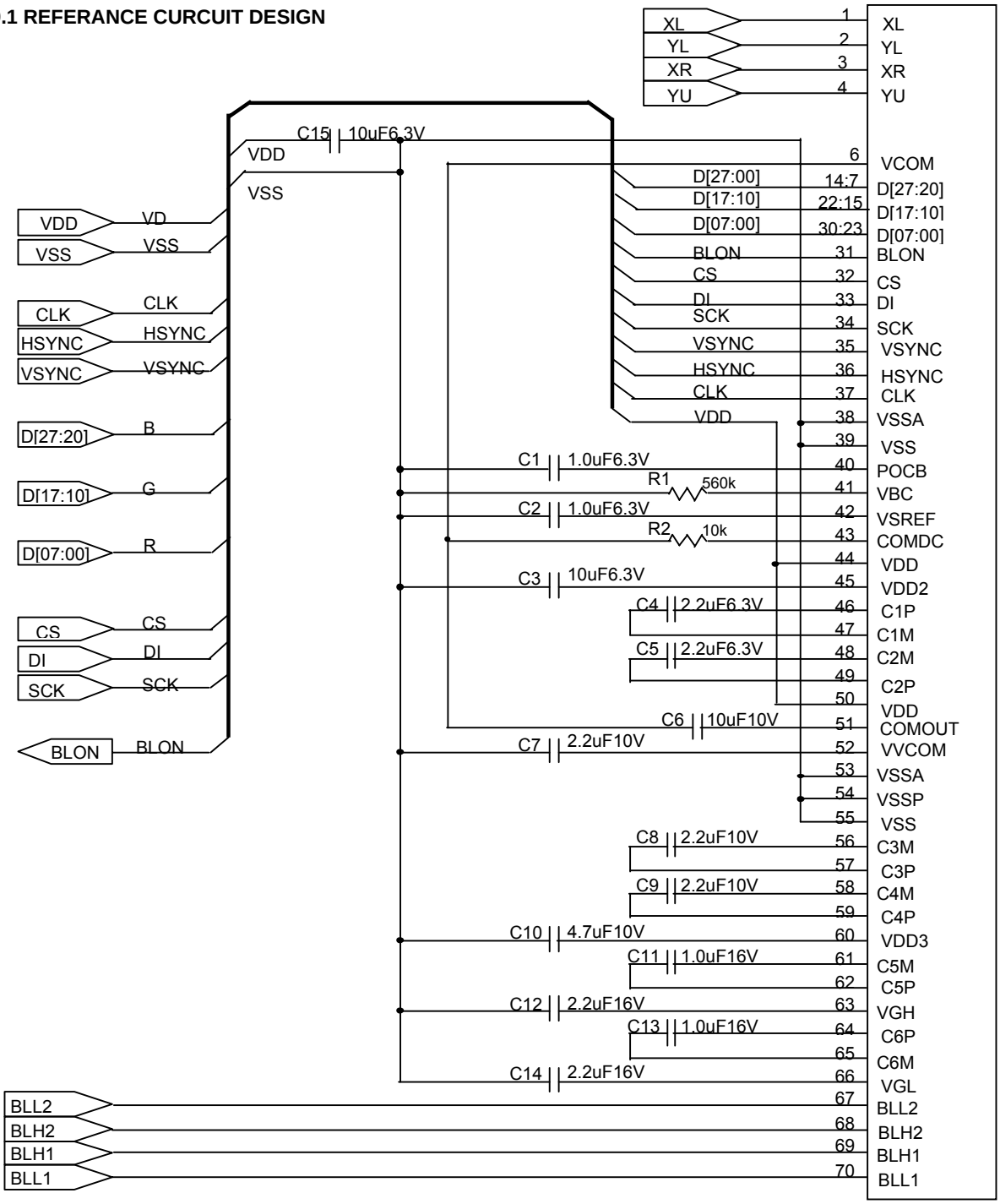
HSYNC and VSYNC supply will stop free-run function, and LCD becomes normal display.

Built in circuit for reducing electric charge remained on panel, in case of sudden power off

"8.4 Standby (Power save) Sequence" is the right procedure to turn off power.
In this sequence, Standby mode setting is followed by Image retention process.
However, Standby mode can't be set in case of sudden power off, such as battery comes off.
Even in that situation, this built-in circuit will reduce electric charge and prevent image retention on panel.

9.CURCUIT DESIGN

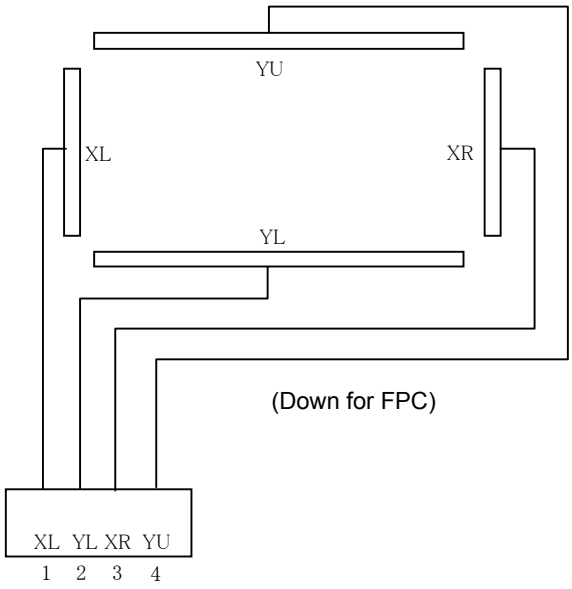
9.1 REFERANCE CURCUIT DESIGN



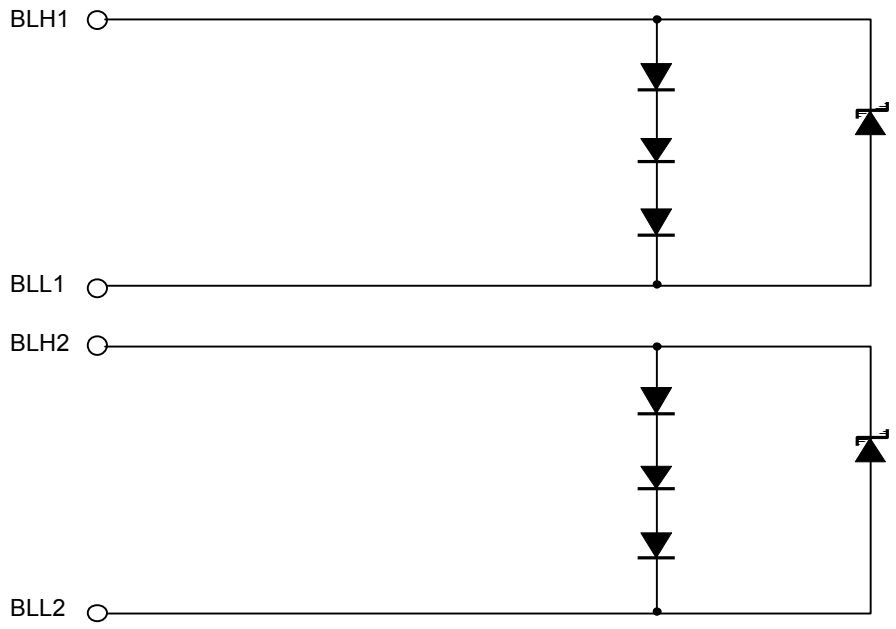
TFT-LCM Reference Circuit

This circuit design is for reference purposes only.Appropriate component values may be different.
Please evaluate on your side.

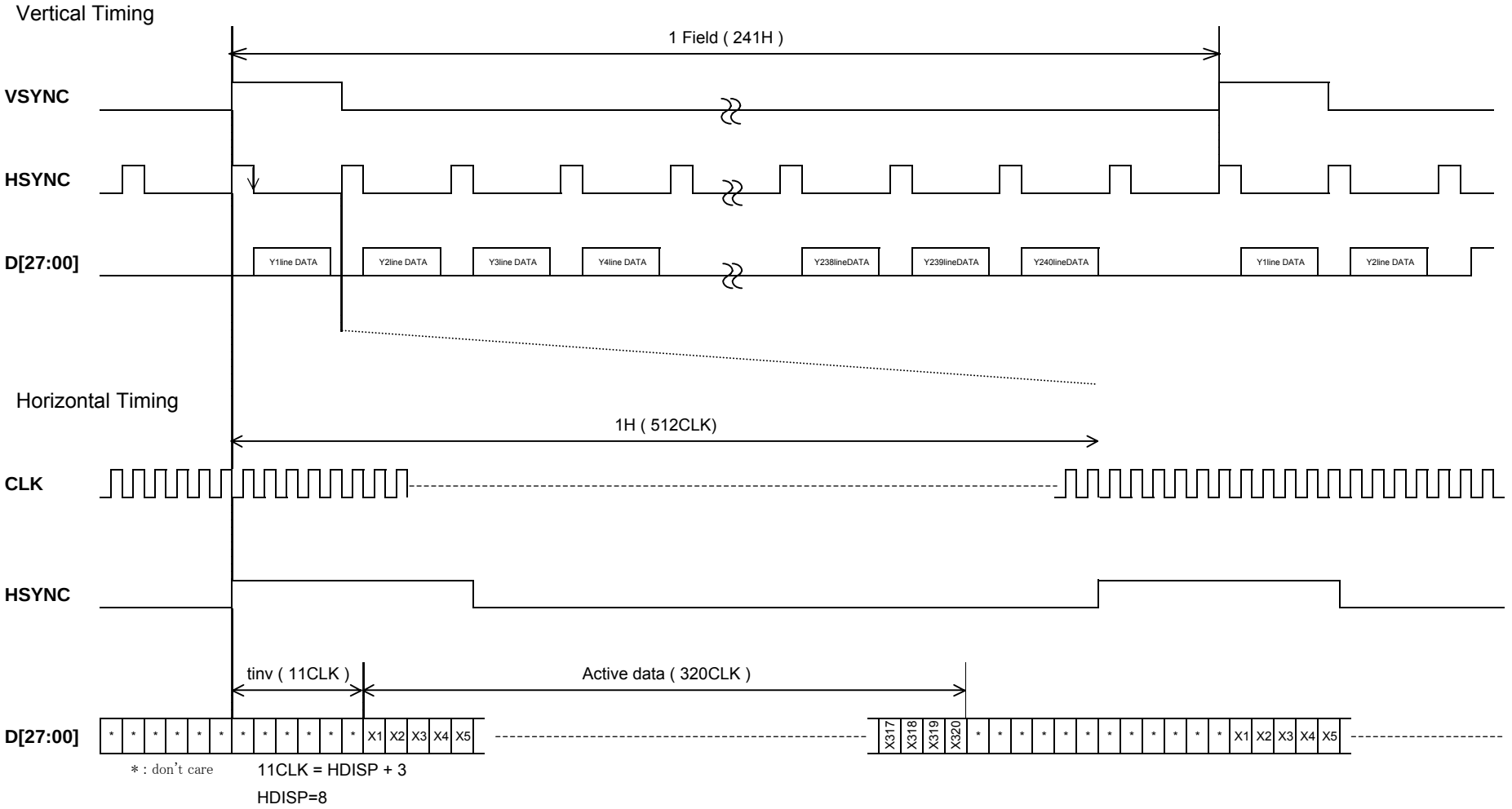
9.2 TOUCH PANEL CIRCUIT



9.3 LED CIRCUIT



Drive Timing Example（In case of normal display, fCLK＝6.75MHz）



10. CHARACTERISTICS

10.1 OPTICAL CHARACTERISTICS

Measuring condition

Measuring equipment CS1000(Konika Minolta),LCD7000(otsuka Electronics)

Driving conditions VDD=3.0V,VSS=0V,

Vcom/C is adjusted to an optimum value.

VLCD=｜Vsigpp±Vcompp｜/2

Back light IL=20.0mA

Measuring temperature Ta=25°C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note #	Remarks
Response time	Rise time	TON	VLCD= 1V→5V	-	-	40	ms	1	※
	Fall time	TOFF	VLCD= 5V→1V	-	-	60	ms		
Contrast ratio		CR	VLCD= 1V／5V	60	-	-		2	
Viewing angle	Left	θL	VLCD= 1V／5V CR≧5	65	-	-	deg	3	※
	Right	θR		65	-	-	deg		
	Up	φU		40	-	-	deg		
	Down	φD		65	-	-	deg		
V-T Threshold voltage		V90		1.5	1.8	2.1	V	4	※
		V50		2.0	2.3	2.6	V		
		V10		2.7	3.0	3.3	V		
White V-T characteristic				See figure 3.					Reference
White chromatically		x	VLCD=1V	See figure 4.				5	
		y							
Maximum contrast angle		CRφ		-15	-7	0	deg	6	※ Downward
Image sticking				No image sticking shall remain after displaying the window pattern for 2 hours				7	
Center brightness			VLCD=1V	200	320	-	cd/m2	8	
Brightness distribution			VLCD=1V	60	-	-	%	9	

＊: Note1-9 Refer to the Appendix "Standed measurement method of optical characteristics for TFT-LCD monitor".

※: Note) The value are measured in module states.

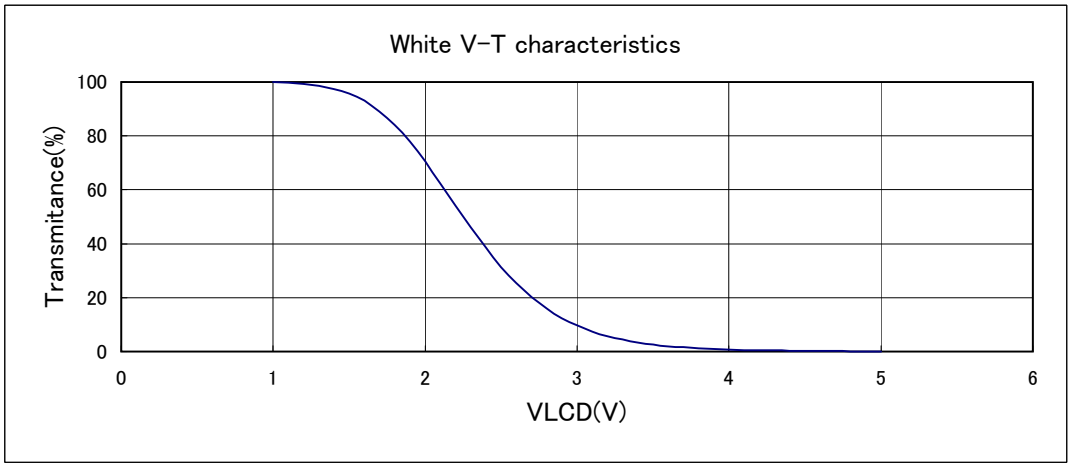
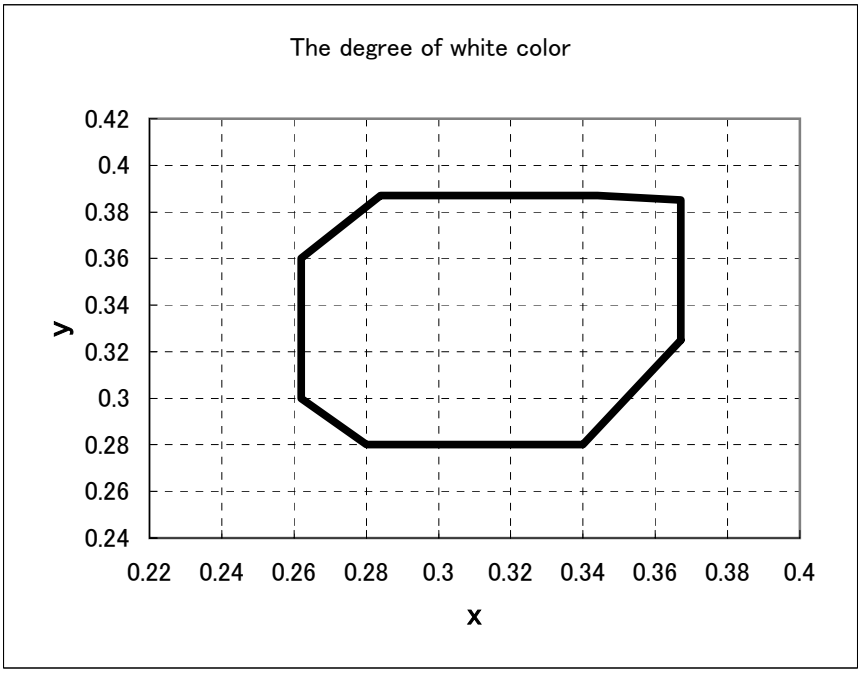


Figure 3 White V-T characteristics



【The degree of white color】

x	y
0.367	0.325
0.367	0.385
0.344	0.387
0.284	0.387
0.262	0.360
0.262	0.300
0.280	0.280
0.340	0.280

Figure 4 The degree of white color

10.2 TEMPERATURE CHARACTERISTICS

Measuring condition

Measuring equipment CS1000(Konika Minolta) ,LCD7000(Otska Electronics)

Driving conditions VDD=3.0V,VSS=0V,

Vcom/C is adjusted to an optimum value.

VLCD=｜Vsigpp±Vcompp｜/2

Back light IL=20.0mA

Item		Rating		Remarks
		Ta=-10°C	Ta=70°C	
Contrast ratio		40 or more	40 or more	
Response time	Rise time	Less than 200ms	Less than 30ms	
	Fall time	Less than 200ms	Less than 50ms	
Display quality		Defects and ununiformity shall be inconspicuous.		As criteria of 11

11. CRITERIA

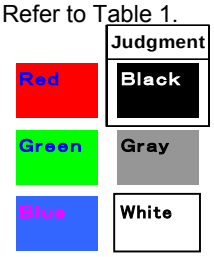
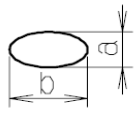
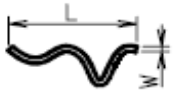
11.1 DISPLAY APPEARANCE SPECIFICATIONS

Testing conditions

Display monitor should be inspected with the following conditions.

Driving signal	Raster pattern(RGB signal color and white)
Signal condition	VLCD:1.5V,2.5V,5V(3steps)
Distance between display and eye	30cm
Illuminance	500 to 1500 LUX
Back light	IL=20.0mA

△B

Item		Definition				Criteria
Display defect	Line defect	Black,white,or color line 3 or more dot defects on a strait line				None
	Dot defect	Unusual brightness of the dots unit due to defects of TFT or Cf, or dust , etc. High brightness defect: Visible through 2% ND filter when VLCD=5V Low brightness defect: Visible through 5% ND filter when VLCD=5V Dark defect: Visible darker when VLCD=2.5V				Refer to Table 1. 
Display quality	Stain	Unevenness of brightness (white stain,black stain,etc.) △B				Invisiblethrough 5%ND filter
	Foreign mater	Dust between the touch panel and the LCD	Dot form	**Diameter**	**Qty**	
				0.25mm<D	N=0	
				0.15<D≦0.25mm	N≦2	
				D≦0.15mm	ignored	
			Line form	**Width** / **Length**	**Qty**	
				0.08mm<W / 3.0mm<L	N=0	
				W≦0.08mm / L≦3.0mm	ignored	
	Flaw	Flaw of touch panel surface		**Width** / **Length**	**Qty**	
				W≦0.02mm / ---	ignored	
				0.02<W≦0.05mm / L≦2mm	ignored	
				0.02<W≦0.05mm / 2<L≦5mm	N≦5	
				0.05mm<W / ---	regarded as a foreign matter	
	Otheres		Due to boundary sample.			

Average of diameters=(long diameter+short diameter)/2:D(mm)

Permissible number :N

Table 1

Model	Bright dot	Dark dot	Total	
COM35T3137KTX	2	1	3	Connected 2 bright defects is counted in 2 dots and that must be within 1 sets. Connected 2 dark defects is not allowed. Connected bright defects- dark defects is not allowed. The distance between bright dots of the same color including connection is 5mm or more.

11.2 APPEARANCE CRITERIA

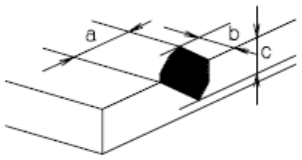
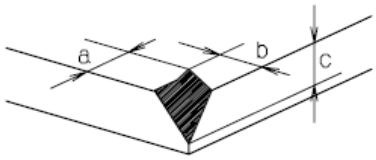
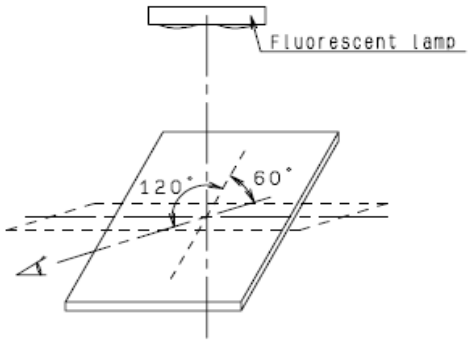
Testing conditions

Illuminance 500～1500Lx

Distance between display and eye 30cm

Item		Criteria	Remarks
Polarizer	Scratch Stain Bubble,dust dent	Invisible items while the monitor is turned on shall be ignored	Applied to effective display area (3.2 form screen area)
S－case		No function trouble	
Cable		No function trouble	

Ⓑ

Item		appearance	Criteria
touch panel	Glass chipping		a≦3 unit: （mm） b≦2 c＜t (t: Glass thick) Ignored
			a≦3 unit: （mm） b≦3 c＜t (t: Glass thick) Ignored
		Progressive cracks	All NG.
	Newton-ring	Interference fringe forming concentric circles.	None
		（In case of doubtful situations） Observe on the 60° from the product surface under a while fluorescent lamp (3-wavelength lamp). 	Average diameter ≦ 8mm: OK Newton-ring level: Due to boundary sample.
	Swell	Measure the height of swell on the film surface. Ⓑ 	H<0.4 unit: （mm） （At the timing of the initial delivery）

12.RELIABILITY

Test item		Test condition	Criteria
Endurance test	High temperature storage	Ta=80°C, 240H	Refer to Table 2.
	Low temperature storage	Ta=-20°C, 240H	Refer to Table 2.
	High temperature/ humidity storage	Ta=60°C, RH=90%, 240H	Functions and pictures shall have no trouble.
	High temperature operation	Tp=70°C, 240H	Refer to Table 2.
	Low temperature operation	Tp=-10°C, 240H	Refer to Table 2.
	High temperature/ humidity operation	Tp=40°C, RH=90%, 240H	Refer to Table 2.
	Thermal shock storage	-20←→80°C (30min/30min) 100cycle	Refer to Table 2.
Mechanical test	Electrostatic discharge test (No operation)	In accordance with EIAJ ED-4701 C-111. C=200pF,R=0Ω,V=±200V 5 times discharge between the power terminal and the other terminals.	No destruction
	Surface discharge test (No operation)	C=250pF,R=100Ω,V=±12kV 5 times discharge at the center of the display. Shield case is connected to the Ground	No destruction
	Vibration test	Amplitude 1.5mm, f=10 to 55Hz, 2 hours each in the X, Y, and Z directions	Functions and pictures shall have no trouble.
	FPC tension test	Apply 3N force for 10 seconds in the direction of ±90 degrees against the FPC original direction (It applies to FPC of LCD.)	Functions and pictures shall have no trouble.
	FPC bend test	Apply 3N force for 10 seconds in the direction of ±180 degrees against the FPC original direction Coming and going three times. (It applies to FPC of LCD.)	Functions and pictures shall have no trouble.
	Impact test	Use CASIO original jigs. Apply half-sine curve of peak acceleration 100(m/s^2 for operation time 6ms, 3 times each in X, Y, and Z directions, in accordance with JIS C 60068-2-27-1995	Functions and pictures shall have no trouble. Refer to the below diagram.
Packing test	Packing vibration-proof test	19.6m/s^2 acceleration and f=10→55→10Hz, apply in each of X, Y, and Z directior for 30 minutes.	Functions and pictures shall have no trouble.
	Packing drop test	Drop the packing from 75cm height, one time each for 6-faces, 3-edges, and 1-corner.	Functions and pictures shall have no trouble.

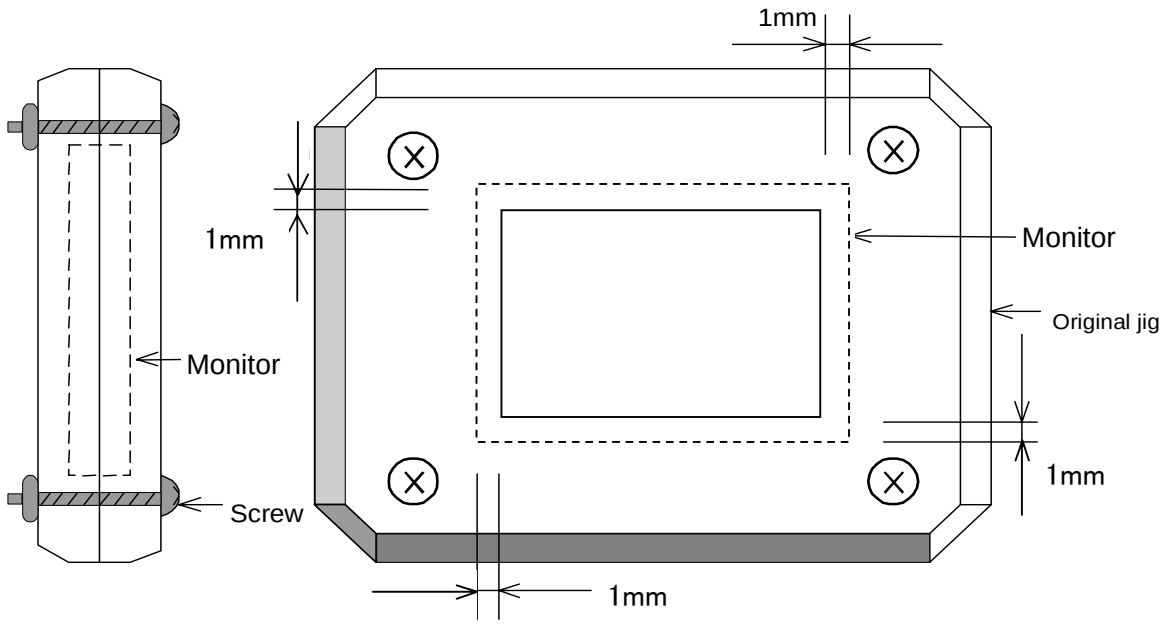
Note : Ta = Ambient temperature Tp = Panel temperature

Table 2 Reliability Criteria

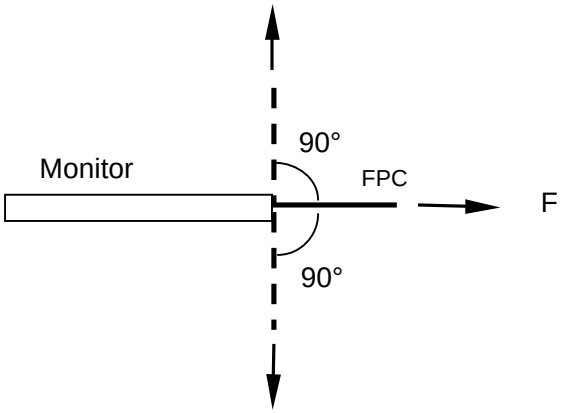
Measure the parameters after leaving the monitors at the room temperature for more than 2 hours from the test completion.

Item	Standard	Remarks
Contrast ratio	40 or more	
Response speed	MAX:TON=60msec TOFF=80msec	
Display quality	No visible abnormality shall be seen	As criteria of 11.

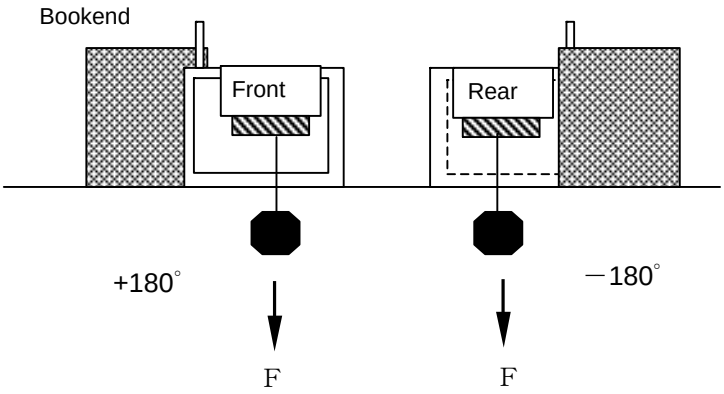
Casio original jig.



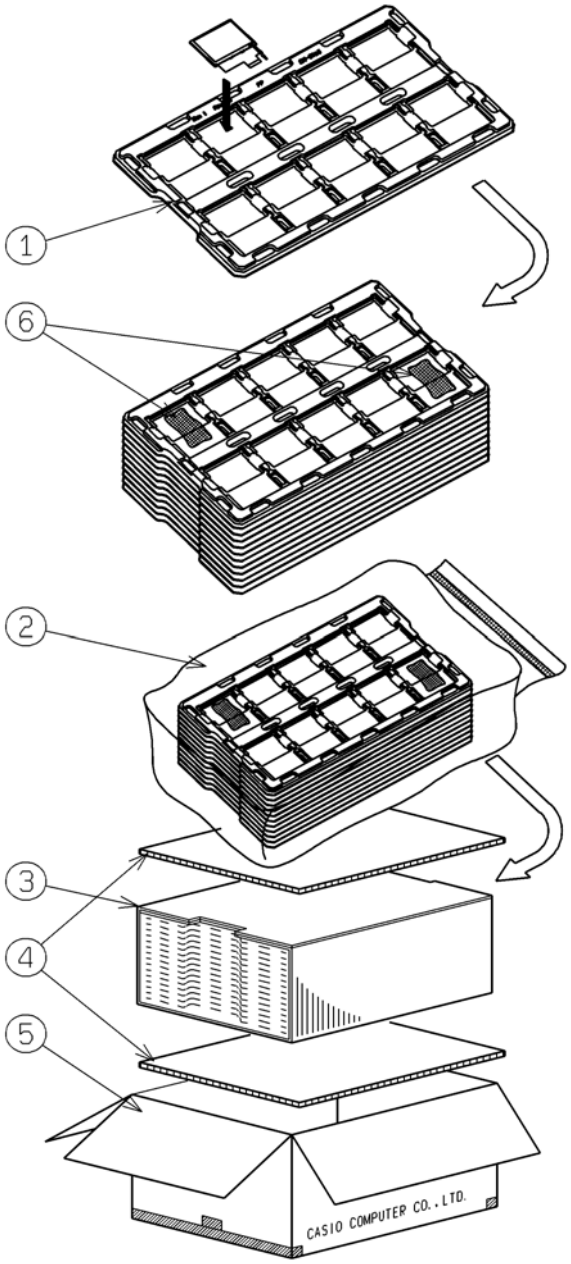
FPC tension test



FPC bend test



13. PACKING SPECIFICATION



Step 1. Each product is to be placed in one of the cut-outs of the tray with the display surface facing upward.
(10 products per tray)

Step 2. Each tray needs to be same orientation respect to the tray below or above it and the trays be in a stack of 10.
One empty tray is to be put on the top of stack of 10 trays.

Step 3. 2 packs of moisture absobers are to be placed on the top tray as shown in the drawing.
Put piled trays into a sealing bag.
Vacuum and seal the sealing bag with the vacuum sealing machine.

Step 4. The stack of trays in the plastic back is to be inserted into a inner carton.

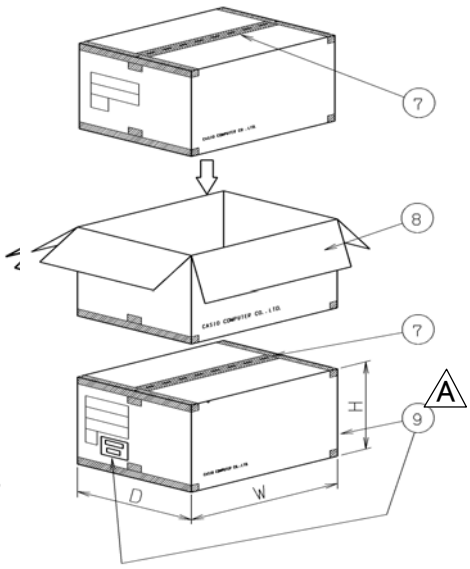
Step 5. A corrugated board is to be placed on the top and on the bottom of the inner carton.
The two corrugated boards and the inner carton is to be inserted into an outer carton.

Step 6. The outer carton needs to sealed with packing tape as shown in the drawing.
The model number, quantity of products, and shipping date are to be printed on the outer carton.
If necessary, shipping labels or impression markings are to be put on the outer carton.

Step 7. The outer carton is to be inserted into a extra outer carton with same direction.
The extra outer carton needs to sealed with packing tape as shown in the drawing.

Step 8. The model number, quantity of products, and shipping date are to be printed on the extra outer carton.
If necessary, shipping labels or impression markings are to be put on the extra outer carton.

Step 9. The barcode label is put on the position shown in Figure.
(2 opposite side)



Remark: The return of packing materials is not required.

	Packing item name	Specs., Material
①	Tray	
②	Sealing bag	
③	Inner carton	Corrugated cardboard
④	Inner board	Corrugated cardboard
⑤	Outer carton	Corrugated cardboard
⑥	Drier	Moisture absorber
⑦	Packing tape	
⑧	Extra outer carton	Corrugated cardboard
A ⑨	Barcode label	(70x45x0.05)

Dimension of extra outer cartor	
D : Approx.	(338mm)
W : Approx.	(549mm)
H : Approx.	(198mm)
Quantity of products packed in one carton	10pcs×10=100pcs
Gross weight : Approx	7.6Kg

14.HANDING PRECAUTIONS

14.1 PRECAUTIONS

Caution

(1) Do not make an impact on the glass, because it may break, causung possible dangers.

(2) When the glass breaks, do not touch it directly with hands.
(You may get glass splinters in your hands or cut your skin.)

(3) In the event that you injure yourself, receive first aid and consult a physician.

(4) Do not put the liquid crystal in your mouth.
(In the event that the liquid crystal panel breaks, the liquid crystal inside will seep out. Although its toxicity has not been verified, you should not put the panel in your mouth.)

(5) If the liquid crystal gets on your skin or clothing, wash it off thoroughly.
(In the event that the liquid crystal gets on your clothing or hand, wipe it off with alcohol, or carefully wash it off with soap and water. If it gets into your eyes, wash your eyes in clean running water for at least 15 minutes, then see a physician)

(6) When disposing of this product,follow the industrial waste diposal standards existing In the country or region concerned.

(7) Do not connect or disconnect this product while the set remains switched on.

(8) This product has been assembled to a high degree of accuracy. Do not attempt to dismantle or modify it.

Caution :

This mark is used to indicate a precaution or an instruction which, if not correctly observed, may result in bodily injury, or material damages alone.

14.2 HANDLING PRECAUTIONS

1)Wear finger sacks when handling the modules at the incoming inspection and/or the production lines, and keep the working area very clean.
Do not touch the surface of the polarizing film because it is vulnerable.

2) Wear a wrist-strap and use an ion blower to avoid electrostatic discharge when handling the modules, because the LCD panel and the driver ICs are valnerable to an electrostatic discharge.

3)Do not scratch or hit the module surface with a tool, and do not drop the module, because the LCD panel made of glass substrates is fragile and the polaizing film is vulnerable to frictions and mechanical impacts.
In case that the module was accidentally dropped, it must be regarded as defective, and do not use it any longer.

4)Do not use or store the module in a place where dew is expected.

5)Do not store the LCD under direct sunlight or at a place exposed to ultraviolet rays because it will cause the deterioration of the LCD.

6)Do not stain the cables or make them damaged, because these might cause contact defects and/or wrong effects on the reliability.

7)Do not bend or pull the FPC part or carry the module just by holding the FPC with fingers.

8)Since the protection film is stuck on the polarizing plate of a monitor's surface, please use it at the time of mounting, removing. Refer to the 14.5th clause for how to remove.
In addition, please understand that our company cannot take responsibility to faults, such as electric destruction produced on the occasion of protection film exfoliation.

14.3 OPERATING PRECAUTIONS

1)Do not expose the driver ICs on the module to strong lights during operation.
It may cause function failures, because the driver ICs have no light shield.

2)When driving the monitor, apply the input signal after the power voltage is supplied.
When turning off the power, turn off the input signal before or at the same timing of switching off the power.

3)Apply an optimum value of Vcom/c when using the module.

4)It causes a trouble when a cable is plugged in and out under the condition that a power supply voltage is input. Plug the cable in and out after cutting off the power supply voltage.

5)Do not operate in the strong magnetic field. It may break a module.

6)Do not indicate a fixed pattern for a long time. It has the possibility that an afterimage breaks out by character of the liquid crystal. Please use a screen saver, and do not indicate a fixed pattern.

14.4 SHIPPING CARTON BOX STORAGE CONDITIONS

Environment

- Temperature: 0 to 40 °C
- Relative humidity: 60% or less
  Shall have no dew if the temperature is low and the humidity is high.
- Atmosphere: Any poisonous gases and chemical substances such as acid or alkaline, which will erode electronic components and/or wiring materials, shall not be detected in a storage room.
- Period: Within approx. 3 months
- Unpacking: In order to prevent the TFT modules from being damaged by static electricity during the unpacking process, adjust the relative humidity of the working room to 50%RH or higher, and take effective measures such as static electricity grounding.
- Maximum allowable quantity of piling : 10

14.5 PRECAUTIONS AT PROTECTION FILM REMOVING PROCESS

When removing the protection film from the mointor screen, static electricity may be generated, causing a function destruction or absorbing dusts. To avoid them, the following environment and working methods are recommended.

A)Working environment

a)Keep the relative humidity at 50% to 70% and the temperature at 15 to 27°C

b)Workers shall wear conductive working clothes, conductive shoes, conductive finger sacks, and wrist-strap bands. The working floor shall also be conductive.

c)The working room shall be a clean room, preventing dusts from coming in. Setting an adhesive mat at the entrance of the room is recommeded.

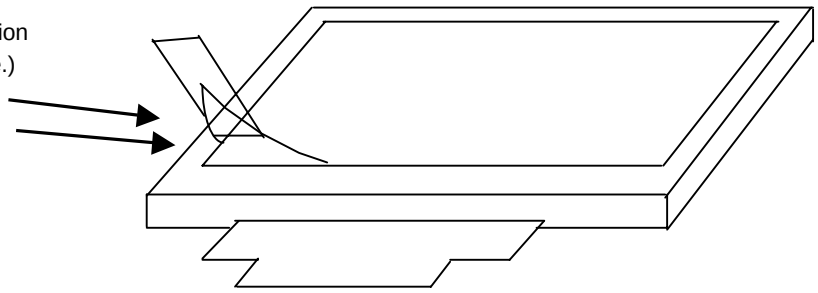
B)Working method

a)Place an ion blower at an optimal distance from the monitor and ,set an optimal wind direction.

b)Put an adhesive tape (Scotch tape, etc.) on the LCD protection film's corners near the ion blower to protect the polarizing film from damage.

c)Pull the adhesive tape slowly (taking more than 2 seconds to complete) towards the operator to remove the protection film.

Blower wind direction (Set an ion blower with its adequate value.)



14.6 QUALITY ASSURANCE

Casio shall be obliged to compensate for defective products by payment at the unit price of the product or substitutes in case that the products are used and stored under the conditions specified in this document, the defect causes are attributable to Casio, and such claims are notified to Casio within one year from the day of product delivery.
Casio shall not be obliged to guarantee the product quality in case that the products are used under conditions beyond the specifications or reorganized by Lite On Technology Corporation.

14.7 OTHERS

In case of revisions of specifications, ordinarily Casio will notify Lite On Technology Corporation. at least one month prior to the product delivery. But in an emergent case, procedures for revision will be separately determined by consultations between Lite On Technology Corporation and Casio.

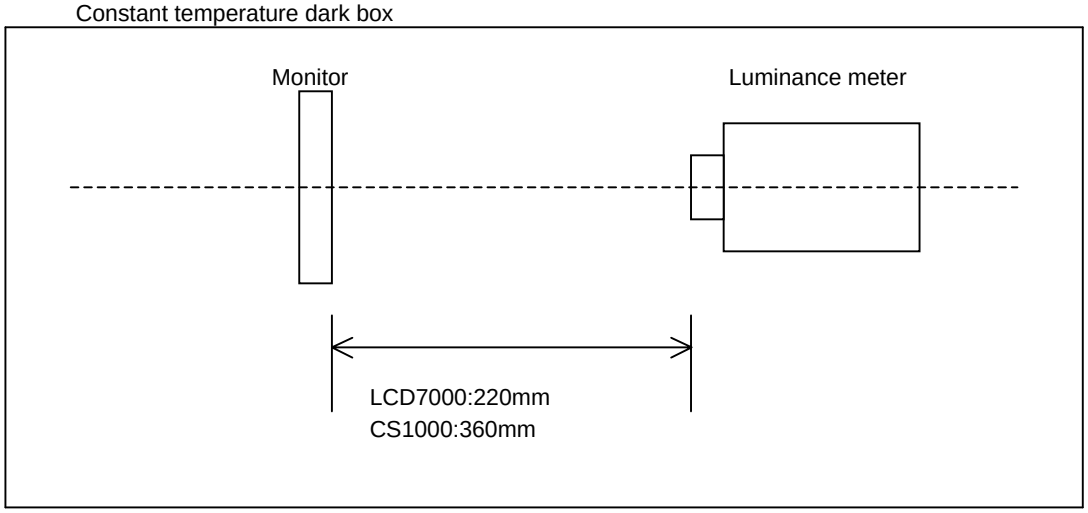
APPENDIX

Standard Measurement Method of Optical Characteristics for TFT-LCD Monitors.

1 Testing conditions

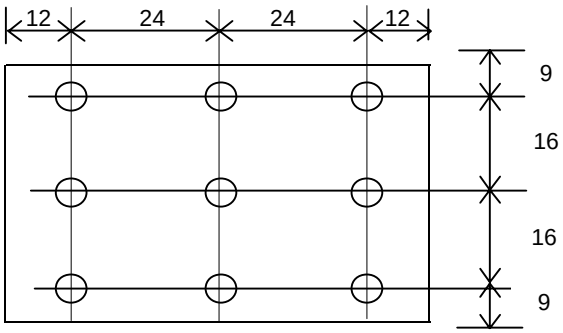
Measuring instrument: CS1000（Konika Minolta）、LCD7000（Otsuka Electronics）
Driving conditions: See “Standard measuring method for optical characteristics.”
Measuring temperature : Unless otherwise specified, the temperature is 25°C
Measuring system : See the diagram below. The luminance meter is positioned on the normal line on the measuring point.
Measuring points: In usually the center point of the screen

Constant temperature dark box



A measuring run should be started after allowing the back light to be lit for 30 minutes.

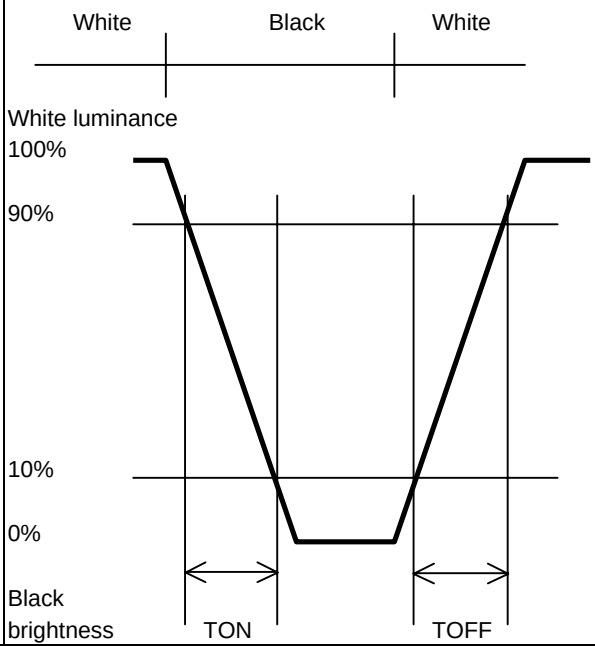
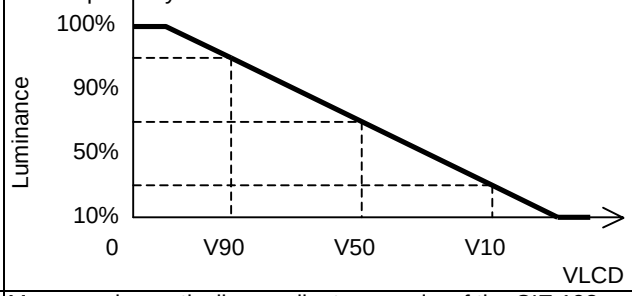
Measuring points: The center point of the screen
For obtaining the luminance distribution only, nine points shall be measured shown below.



Unit:mm

Backlight IL=20.0mA

2 Testing method

Note	Item	Testing method	Measuring equipment	remarks
1	Response time	Measure output signal waves with a luminance meter when the raster or window pattern is changed over from white to black and from black to white 	LCD7000	Black VLCD=5V White VLCD=1V T ON Rise time T OFF Fall time
2	Contrast ratio	Put the raster or window pattern on the display. Then measure the maximum luminance Y1 (VLCD = 1V) and the minimum luminance Y2 (VLCD = 5V) at the center of the display. Contrast ratio = Y1/Y2 Measurement spot diameter: 8mm ϕ	CS1000	
3	Viewing angle Horizontal θ Vertical ϕ	Change the viewing angles step by step in up, down, left, and right direction each, and measure contrast ratio to obtain respective angle where contrast ratio becomes 5.	LCD7000	
4	V-T threshold	Change the VLCD by 0.1V step and measure monitor luminances. VLCD, where the luminance is 90%, 50%, and 10% of the maximum value ,is defined as V90, V50, and V10 respectively. 	LCD7000	
5	White chromaticity balance	Measure chromatically coordinates x and y of the CIE 1931 calorimetric system under VLCD = 1V. Color matching function is at view of 2°.	CS1000	

Note	Item	Testing method	Measuring equipment	remarks
6	Max. contrast angle	Change the viewing angles step by step in up/down direction, and measure the contrast ratio at each steps to obtain angles where the contrast ratio becomes maximum.	LCD7000	
7	Image sticking	Confirm image stickings with eyes after displaying the window pattern (VLCD=1/5V)for 2 hours		Vcom/C is adjusted to optimum value.
8	Center luminance	Measure the luminance at the center of the screen.	CS1000	
9	Luminance distribution	(Luminance distribution) = 100 x B/A % A : max. luminance of the 9 points B : min. luminance of the 9 points	CS1000	