NEC

TFT COLOR LCD MODULE

Type: NL8060BC26-15
26cm (10.4 Type), SVGA
LVDS interface (1 port)

SPECIFICATIONS

(First Edition)

PRELIMINARY

This document is preliminary. All information in this document is subject to change without prior notice.

NEC Corporation
Display Device Operations Unit
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Checked		May. 26, 1998
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The devices listed in this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control systems and life support systems.

If customers intend to use NEC devices for above applications or they intend to use "Standard" quality grade NEC devices for applications not intended by NEC, please contact our sales people in advance.

Application examples recommended by NEC Corporation.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

1. DESCRIPTION

NL8060BC26-15 is a TFT(thin film transistor) active matrix color liquid crystal display(LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL8060BC26-15 has a built-in backlight with inverter.
The 26cm(10.4 Type) diagonal display area contains 800×600 pixels and can display 262144 colors simultaneously.

2. FEATURES

- High luminous(100 cd/cm^2 at IL= 3mArms)
- Low reflection
- Expanded screen size without increasing the frame area
- LVDS interface (adapted THC63LVDF63A, THine Microsystem, Inc.)
- Supply voltage: 3.3V
- Incorporated edge type backlight (One lamp, Inverter-less)

3. APPLICATIONS

- Engineering work station, Personal computer
- Display terminals for control system
- Monitors

4. STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.
RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.
Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

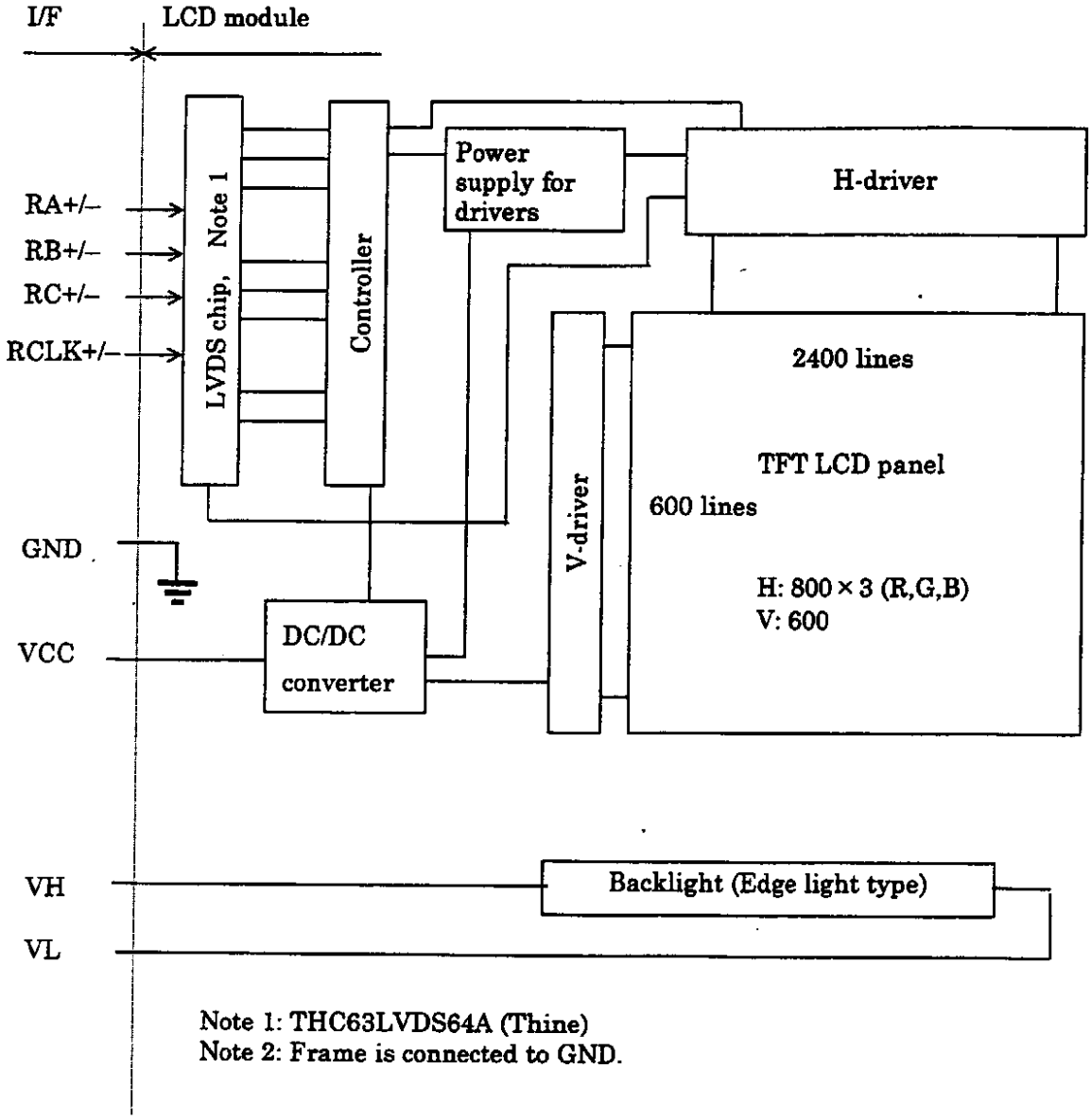
Display area	211.2(H) × 158.4(V)mm
Drive system	a-Si TFT active matrix
Display colors	262144 colors
Number of pixels	800 × 600
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.264(H) × 0.264(V)mm
Module size	237.8(H) × 170.0(V) × 5.8 typ.(D)mm
Weight	270g(typ.)
Contrast ratio	150:1(typ.)

Viewing angle (more than the contrast ratio of 10:1)
- Horizontal: 50° (typ. , left side, right side)
- Vertical: 20° (typ. , up side), 40° (typ., down side)

Designed viewing direction
- Wider viewing angle with contrast ratio: down side (6 o'clock)
- Wider viewing angle without image reversal: up side (12 o'clock)
- Optimum grayscale (γ =2.2): 5° (typ., down side)

Polarizer pencil-hardness	3H(min. at JIS-K5400)
Color gamut	40%(typ. At center, To NTSC)
Response time	TBDms(typ.), "white" to "black"
Luminance	100cd/m^2 (typ. at IL= 3.0mArms)
Signal system	LVDS interface (THC63LVDF64A, THine Microsystem, Inc.) RGB 6-bit signals, Synchronous signals(Hsync, Vsync), and Dot clock(CLK) are adapted for THC63LVDF63A (THine Microsystem, Inc.)
Supply voltage	3.3V (Logic, LCD driving)
Backlight	Edge light type: One cold cathode fluorescent lamp, Inverter-less
Power consumption	2.8 W (typ. at 100 cd/m^2)

6. OUTLINE OF CHARACTERISTICS (at room temperature)



Note 1: THC63LVDS64A (Thine)
Note 2: Frame is connected to GND.

7. GENERAL SPECIFICATIONS

Item	Specifications	Unit
Module size	237.8±0.5 (H) × 170.0±0.5 (V) × 6.0 max.(D)	mm
Display area	211.2 (H) × 158.4 (V)	mm
Number of pixels	800 (H) × 600 (V)	pixel
Dot pitch	0.088 (H) × 0.264 (V)	mm
Pixel pitch	0.264 (H) × 0.264 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	—
Display colors	262,144	color
Weight	300(max.)	g

8. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VCC	-0.3 to +4.0	V	Ta = 25℃
Logic input voltage	VI	-0.3 to VCC+0.3	V	
Lamp voltage	VL	1500	V	
Storage temperature	Tst	-20 to +60	℃	—
Operating temperature	Top	0 to +50	℃	Module surface*
Humidity (No condensation)		≦ 95% relative humidity		Ta≦40℃
		≦ 85% relative humidity		40℃<Ta≦50℃
		Absolute humidity shall not exceed Ta=50℃,85% relative humidity level.		Ta>50℃

* Measured at the display area

9. ELECTRICAL CHARACTERISTICS

(1) Logic/ LCD driving

Ta = 25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VCC	3.0	3.3	3.6	V	—
Ripple voltage	Vrp	—	—	100	mV	for VCC
LVDS signal input "L" voltage	ViL	-100	—	—	mV	VCM=1.2V VCM:Common mode voltage in LVDS driver
LVDS signal input "H" voltage	ViH	—	—	+100	mV	
Terminating resistor	Rt	—	100	—	Ω	—
Supply current	ICC	—	250 note 1	400	mA	VCC=3.3V

note 1: Checker flag pattern(in EIAJ ED-2522)

(2) Backlight

Ta = 25℃

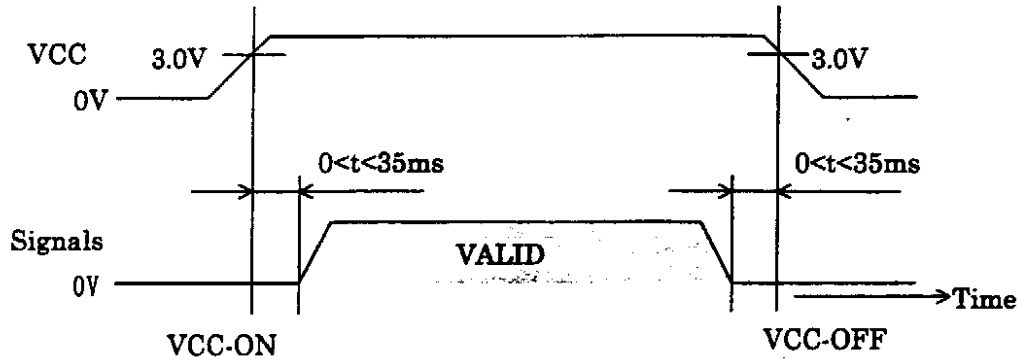
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Lamp current	IL	2.0	3.0	5.5	mArms	3.0mArms: 100cd/cm²(typ) 5.5mArms: 150cd/cm²(typ)
Lamp voltage	VL	—	650	—	Vrms	IL = 3.0mArms
Lamp turn on voltage	VS	—	—	900	Vrms	Ta = 0℃
		—	—	700		Ta = 25℃
Inverter out put voltage	—	1200	—	1500	Vrms	—
Oscillator frequency	Ft	50	—	95	KHz	—

note 1: Recommended value of "Ft"

- Ft is within the specification.
- $Ft = \frac{1}{4th} \times (2n-1)$ th: Hsync period, n: a natural number

If Ft is out of the recommended value, interface between Ft frequency and Hsync frequency may cause beat on the display.

10. SUPPLY VOLTAGE SEQUENCE



*1 The supply voltage for input signals should be the same as VCC.
*2 Apply VDDB within the LCD operation period. When the backlight turns on before LCD operation or the LCD operation turns off before the backlight turns off, the display may momentarily become white.
*3 When the power is off, please keep whole signals(Hsync, Vsync, CLK, DE, Data) low level or high impedance.

11. INTERFACE PIN CONNECTION

(1) Interface connector for signal and power

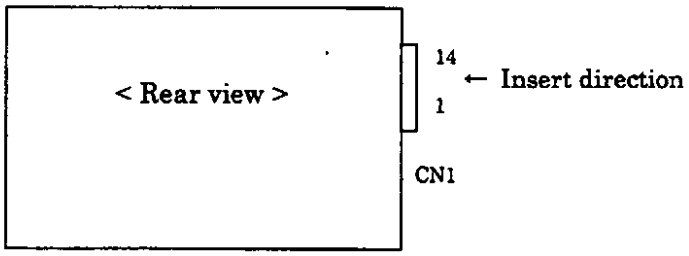
Part No. : 55063-1410
Adaptable socket : 51146-1400
Supplier : MOLEX-JAPAN CO., LTD.

CN1

Pin No.	Symbol	Signal type	Function
1	VCC	+3.3V power supply	Supply +3.3V±0.3%
2	VCC		
3	RA+	Pixel data etc.	LVDS differential data input
4	RA-		
5	GND	Ground	Note 1
6	RB+	Pixel data etc.	LVDS differential data input
7	RB-		
8	GND	Ground	Note 1
9	RC+	Pixel data etc.	LVDS differential data input
10	RC-		
11	GND	Ground	Note 1
12	RCLK+	Pixel clock	CLK for pixel data f=38.362MHz (typ.) (LVDS level)
13	RCLK-		
14	GND	Ground	Note 1

note 1: Signal ground for logic and LCD driving. GND should be connected to system ground. GND is connected to frame.
note 2: Please connect all terminals with cables of 100Ω twist pair.

CN1 :Figure from socket view



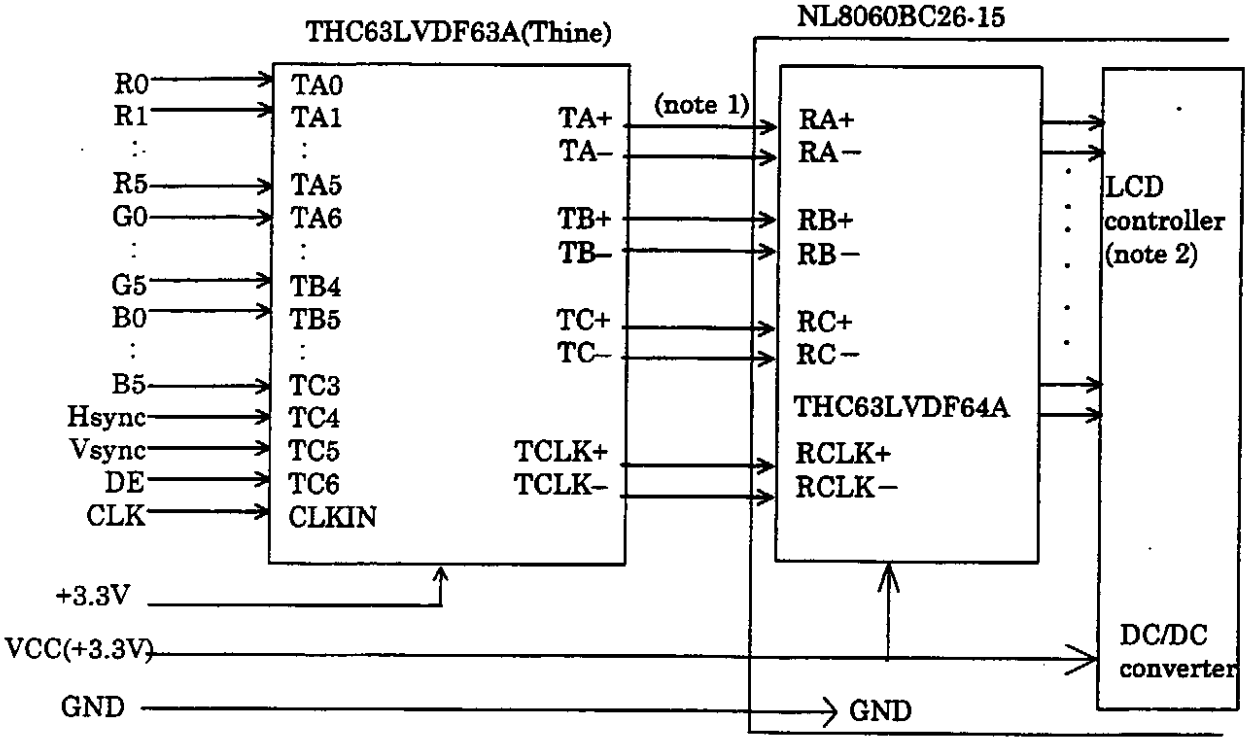
(2) Connector for backlight unit

Part No. : HV-2S-C1
Adaptable socket : HV-2P-HF
Supplier : Japan Aviation Electronics Industry Limited (JAE)

CN2

Pin No.	Symbol	Function
1	VH	High voltage terminal (The cable color is white)
2	VL	Low voltage terminal

12. METHOD OF CONNECTION FOR LVDS chip



note 1: 100Ω twist pair
note 2: These signals should be kept in the specified range of 14.INPUT SIGNAL TIMING.
note 3: R0, G0 and B0 are LSB. R5, G5 and B5 are MSB.

13. DISPLAY COLORS vs INPUT DATA SIGNALS

Display colors		Data signal(0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:						:						:		
	↓				:						:						:		
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

note: Colors are developed in combination with 6-bit signals (64 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 262,144 ($64 \times 64 \times 64$) colors.

14. INPUT SIGNAL TIMING

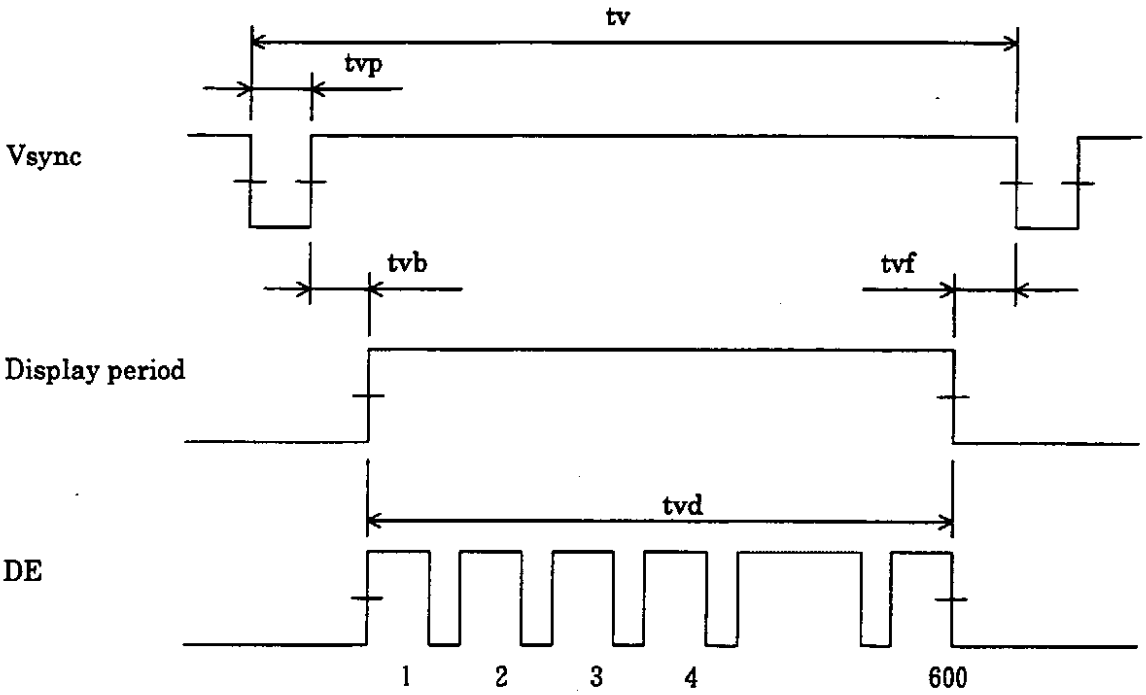
(1) Input signal specification for LCD controller

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	1/tc	34.0	38.362	42.0	MHz	26.067ns(typ.)
	Duty	tch/tc	0.4	0.5	0.6	—	note 1
	Rise, fall	tcrf	—	—	10	ns	note 1
Hsync	Period	th	—	26.693	—	ms	37.463kHz(typ.)
			—	1024	—	CLK	
	Display period	thd		800		CLK	—
	Front-porch	thf	4	24	—	CLK	—
	Pulse width	thp *	2	72	128	CLK	—
	Back-porch	thb *	13	128	509	CLK	—
	* thp + thb		15	200	511	CLK	—
	Hsync-CLK timing	ths	8	—	—	ns	note 1
	CLK-Hsync timing	thh	10	—	—	ns	note 1
	Rise, fall	thrf	—	—	10	ns	—
Vsync	Period	tv	16.1	16.683	17.2	ms	59.94Hz(typ.)
			—	625	—	H	
	Display period	tvd		600		H	—
	Front-porch	tvf	1	1	—	H	—
	Pulse width	tvp *	1	2		H	—
	Back-porch	tvb *	1	22		H	—
	* tvp + tvb		2	24	254	H	—
	Vsync-Hsync timing	tvs	15	—	—	ns	note 1
	Hsync-Vsync timing	tvh	1	—	—	CLK	note 1
	Rise, fall	tvrf	—	—	10	ns	note 1
DATA	DATA-CLK (Set up)	tds	8	—	—	ns	note 1
	CLK-DATA (Hold)	tdh	10	—	—	ns	note 1
	Rise, fall	tdrf	—	—	10	ns	note 1
DE	DE-CLK timing	tes	8	—	—	ns	—
	CLK-DE timing	teh	10	—	—	ns	
	Rise, fall	terf	—	—	10	ns	

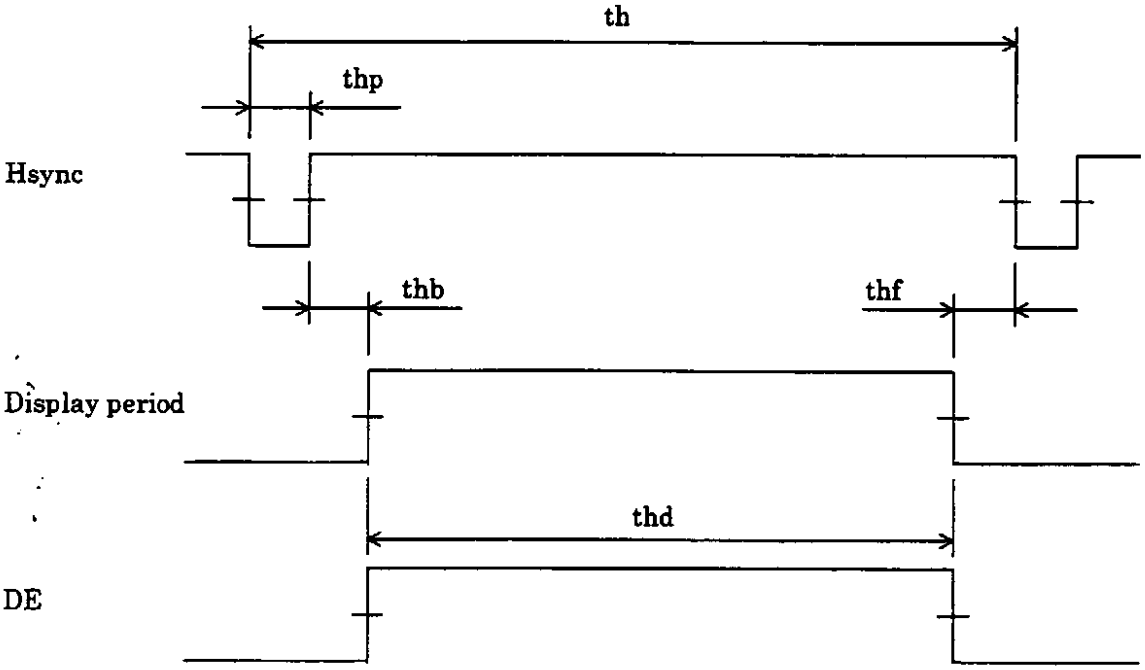
note 1: These values are in the output of THC63LVDS64A.
(Refer to 12. METHOD OF CONNECTION FOR LVDS chip)

(2) Definition of input signal timing for LCD controller

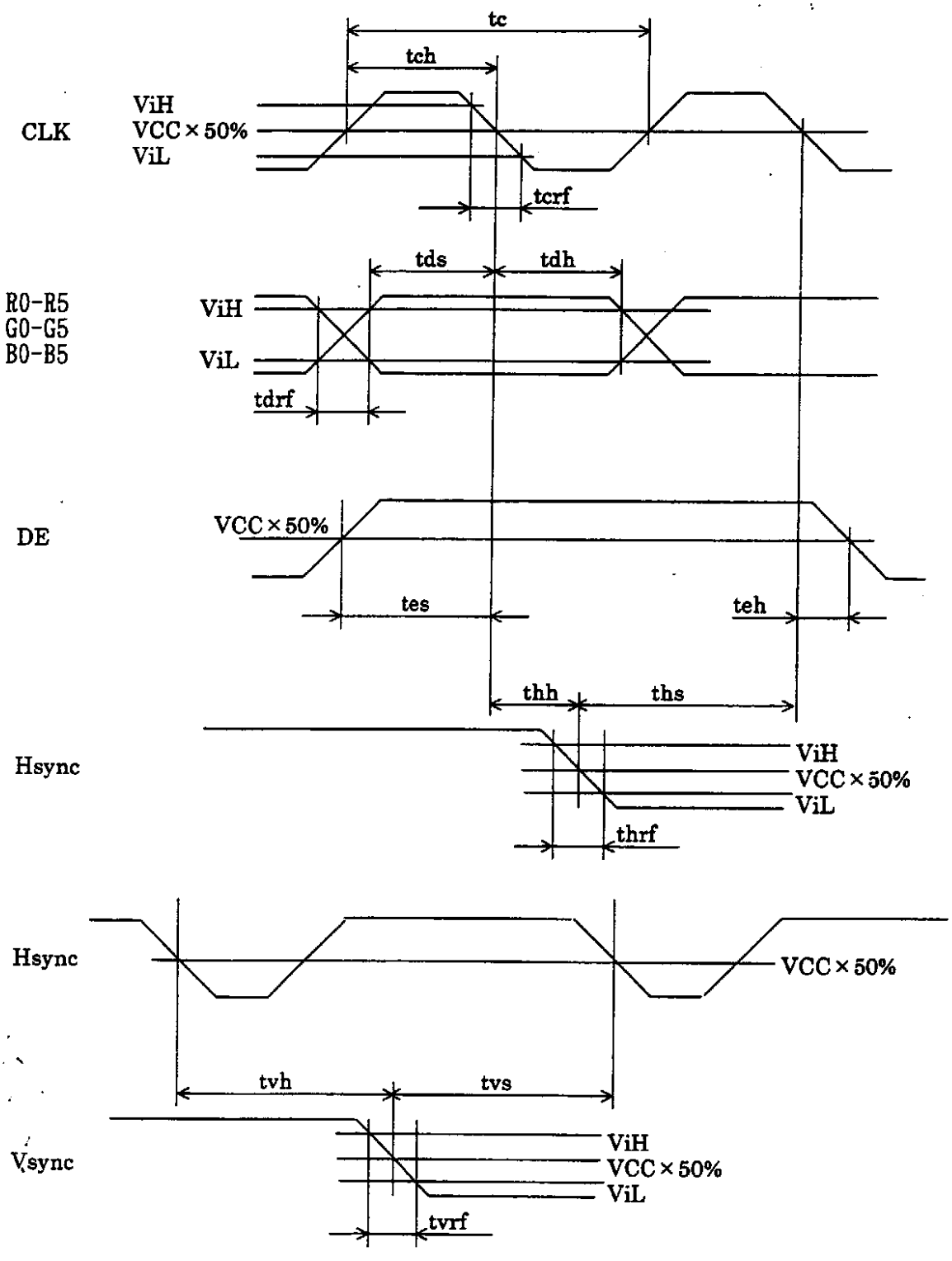
<Vertical>



<Horizontal>

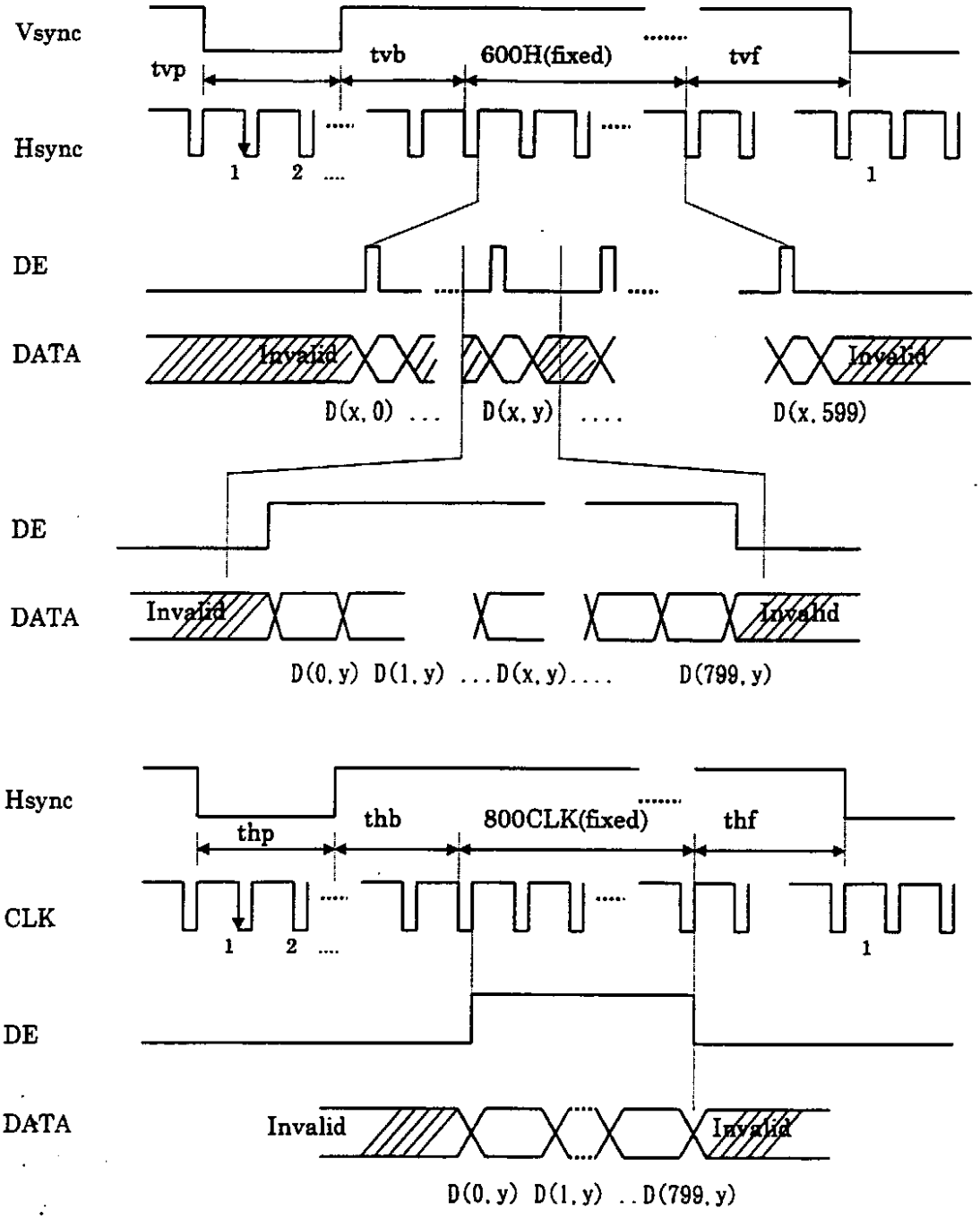


note 1: "Display period" do not exist as signals.
note 2: These values are in the output of THC63LVDS64A.
(Refer to 12. METHOD OF CONNECTION FOR LVDS chip)



ViH = VCC × 0.7(Min.)
ViL = VCC × 0.3(Max.)

(3) Input signal timig chart for LCD



note 1: These values are in the output of SN75LVDS86 or THC63LVDS64A.
(Refer to 12. METHOD OF CONNECTION FOR LVDS chip).

(4) Display position of input data

D(0, 0)	D(1, 0)	···	D(X, 0)	···	D(799, 0)
D(1, 0)	D(1, 1)	···	D(X, 1)	···	D(799, 1)
⋮	⋮	⋮	⋮	⋮	⋮
D(0, Y)	D(1, Y)	···	D(X, Y)	···	D(799, Y)
⋮	⋮	⋮	⋮	⋮	⋮
D(0,599)	D(1,599)	···	D(X,599)	···	D(799,599)

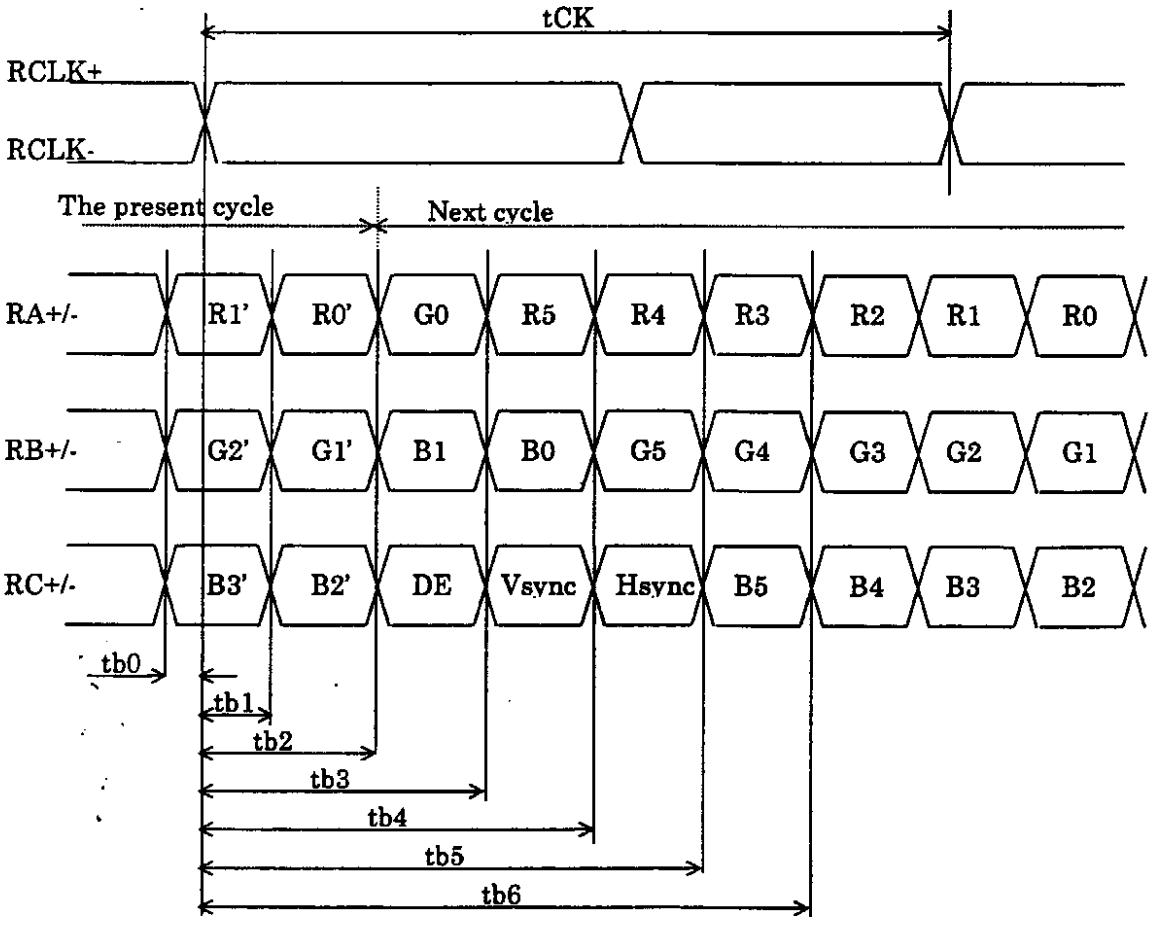
15. FOR LVDS RECEIVER

(1) Input signal specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
CLK Frequency	tCK	29.41	26.07	23.81	ns	–
Bit0 position	tb0	–	0	–	ns	–
Bit1 position	tb1	–	1/7tck	–	ns	–
Bit2 position	tb2	–	2/7tck	–	ns	–
Bit3 position	tb3	–	3/7tck	–	ns	–
Bit4 position	tb4	–	4/7tck	–	ns	–
Bit5 position	tb5	–	5/7tck	–	ns	–
Bit6 position	tb6	–	6/7tck	–	ns	–
–	SKRM	490	–	–	ps	–

note 1: See the specifications of LVDS manufactures for detailed design.

(2) Input signal timing chart



16. OPTICAL CHARACTERISTICS

Ta = 25 ℃ note 1

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio		CR	$\theta x = \pm 0^\circ, \theta y = \pm 0^\circ$	80	150	—	—	note 2
			Best contrast angle $\theta x = \pm 0^\circ, \theta y = -5^\circ$	—	300	—	—	note 2
Viewing angle range	Horizontal	$\theta x+$	CR>10, $\theta y = \pm 0^\circ$	30	50	—	deg.	note 3
		$\theta x-$	CR>10, $\theta y = \pm 0^\circ$	30	50	—	deg.	
	Vertical	$\theta y+$	CR>10, $\theta x = \pm 0^\circ$	10	20	—	deg.	
		$\theta y-$	CR>10, $\theta x = \pm 0^\circ$	20	40	—	deg.	
Color gamut		C	To NTSC	35	40	—	%	note 4
Response time		ton	"White" to "Black"	—	TBD	40	ms	note 5
		toff	"Black" to "White"	—	TBD	TBD	ms	
Luminance		Lu	"White"	70	100	—	cd/m^2	note 6
			"White", IL = 5.5mArms	—	150	—	cd/m^2	
Luminance uniformity		—	max. / min.	—	—	1.40	—	note 7

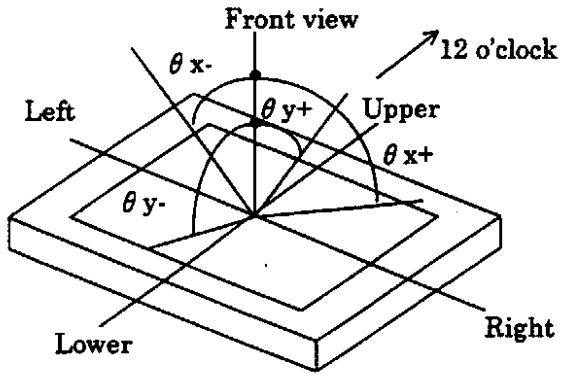
note 1: VCC = 3.3V, IL = 3.0mArms

note 2: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

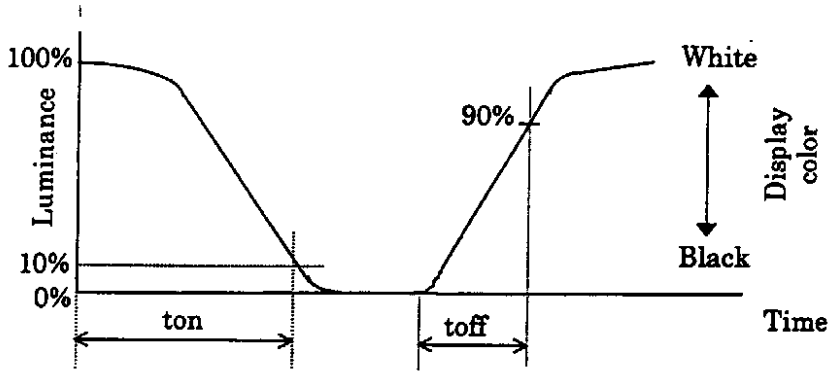
The luminance is measured in a darkroom.

note 3: Definitions of viewing angle are as follows.

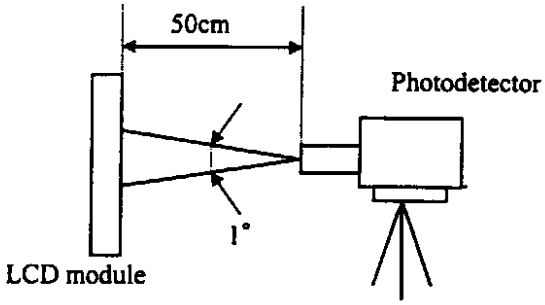


note 4: Viewing angle is $\theta x = \pm 0^\circ$, $\theta y = \pm 0^\circ$. At center.

note 5: Definition of response time is as follows.
Photodetector output signal is measured when the luminance changes "white" to "black" or "black" to "white".
Response time is the time between 100% (0%) and 10% (90%) of the photodetector output amplitude.



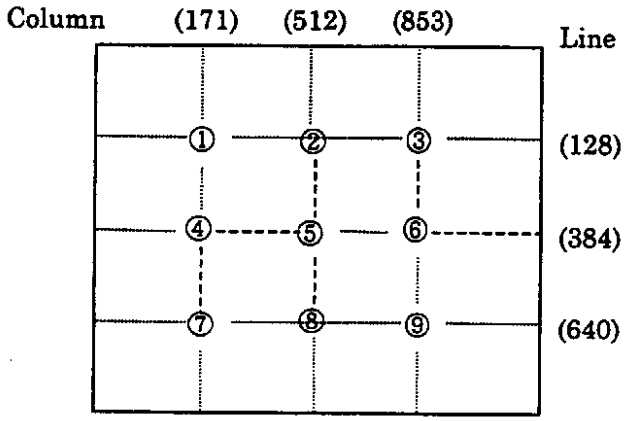
note 6: The luminance is measured after 20 minutes from the module works, with all pixels in "white".



note 7: The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity} = \frac{\text{Minimum Luminance}}{\text{Maximum Luminance}}$$

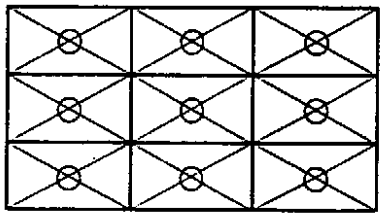
The luminance is measured at near the five points shown below.



17. RELIABILITY TEST

Test item	Test condition	Judgment
High temperature/humidity operation	50±2℃, 85% relative humidity 240 hours, Display data is black.	*1
Heat cycle (operation)	① 0℃±3℃···1 hour 55℃±3℃···1 hour ② 50 cycles , 4 hours/cycle ③ Display data is black.	*1
Thermal shock (non-operation)	① -20℃±3℃···30 minutes 60℃±3℃···30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 0.5G 1 minute/cycle, X,Y,Z direction ② 120 times each direction	*1, *2
Mechanical shock (non-operation)	① 30G, 15ms X,Y,Z direction ② 5 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10KV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: Display function is checked by the same condition as LCD module out-going inspection.
*2: Physical damage
*3: Discharge points are shown in the figure.



18. GENERAL CAITION

Because next figures and sentences are very important, please understand these contents as follows.

⚠ CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

This figure is a mark that you will get hurt when you make a mistake to operate.

CAUTIONS

(1) A caution when taking out the module

① Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges. Peel protection sheet out from the LCD panel surface as slowly as possible.

②  As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

④ Do not pull the interface connectors in or out while the LCD module is operating.

⑤ Put the module display side down on a flat horizontal plane.

⑥ Handle connectors and cables with care.

⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

⑧ The torque of mounting screw should never exceed 0.2 N·m (2 Kgf·cm).

⑨ Do not grab the TCP (Tape Carrier Package) as the transparent sheet on rear side is very thin. If pressure is added on TCPs, they may break.

(3) Cautions for the atmosphere

① Dew drop atmosphere should be avoided.

② Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer-packing pouch and under relatively low temperature atmosphere is recommended.

③ This module uses cold cathode fluorescent lamp. Therefore, The lifetime of lamp becomes short conspicuously at low temperature.

④ Do not operate the LCD module in a high magnetic field.

(4) A caution for the module characteristics

① Do not apply fixed pattern data signals to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

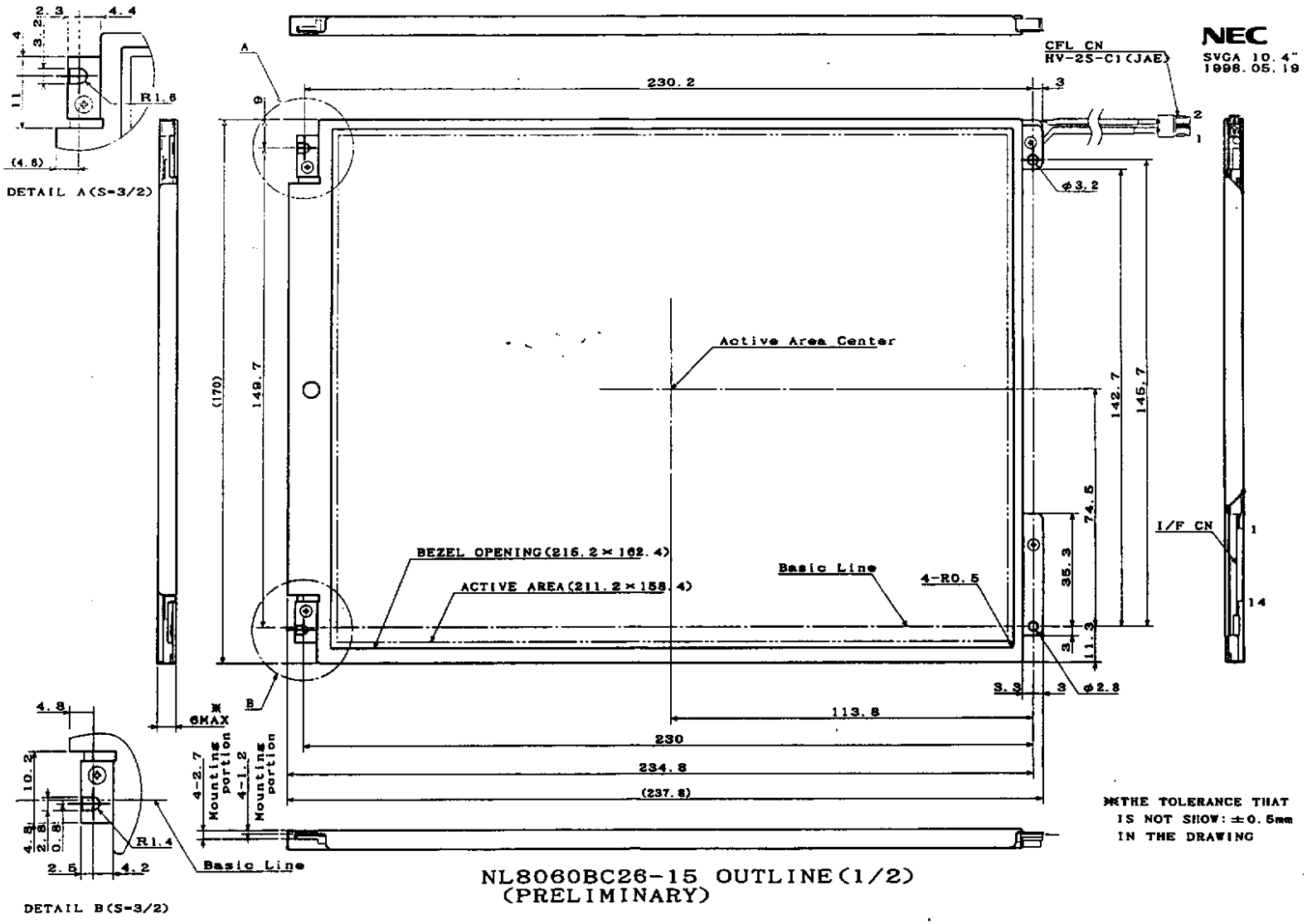
(5) Other cautions

① Do not disassemble and/or reassemble LCD module.
② Do not readjust variable resistors or switches etc.
③ When returning the module for repair or etc., please pack the module not to be broken. We recommend the original shipping packages.

Liquid Crystal Display has the following specific characteristics. These are not defects or malfunctions.

The ambient temperature may affect the display condition of LCD module.
The LCD module uses cold cathode tube for backlighting. Optical characteristics, like luminance or uniformity, will change during time.

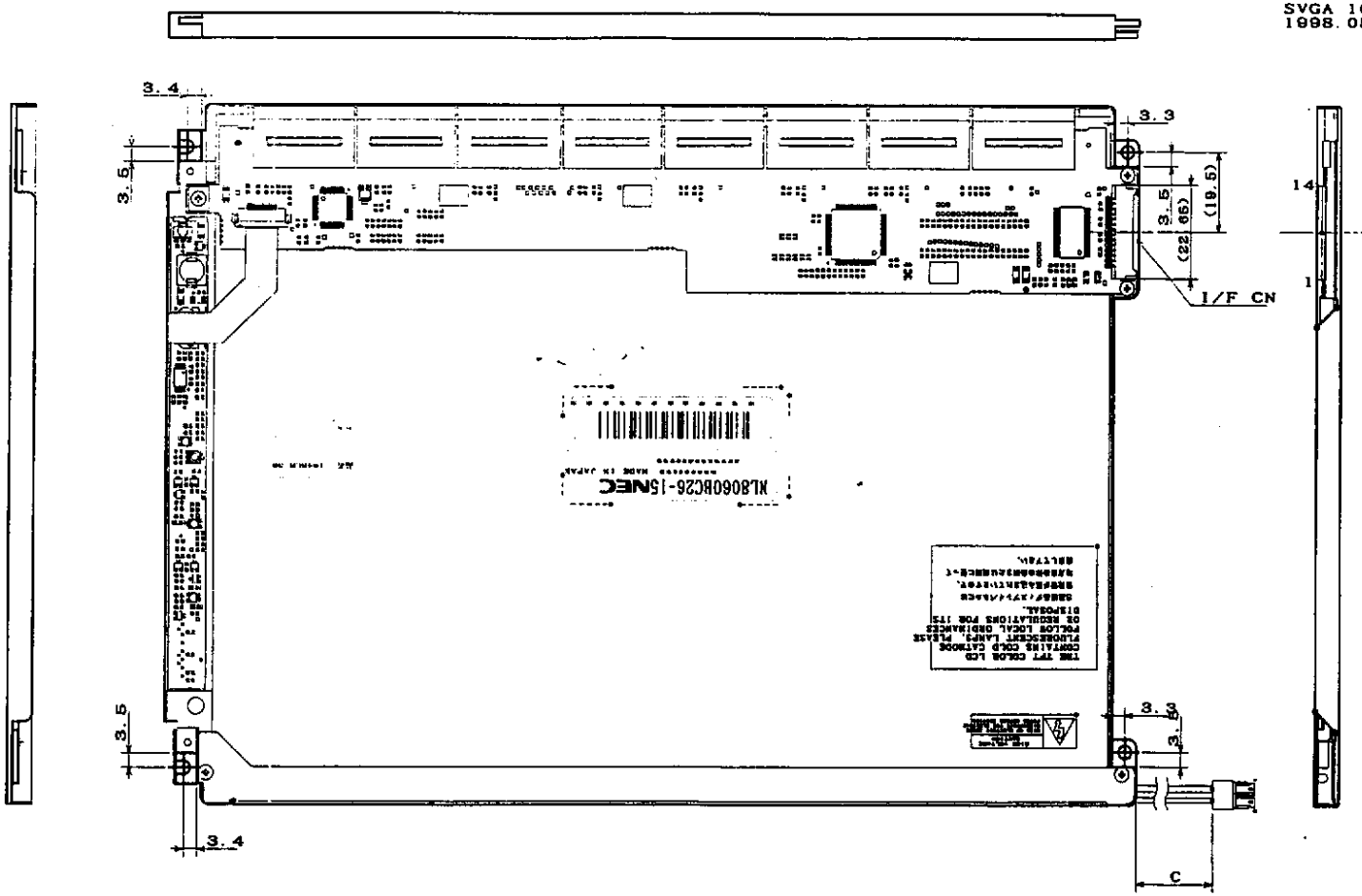
Uneven brightness and/or small spots may be noticed depending on different display patterns.



NL8060BC26-15 OUTLINE(1/2)
(PRELIMINARY)

NEC

SVGA 10.4"
1998.05.19



NL8060BC26-15 OUTLINE(2/2)
(PRELIMINARY)

DETAIL C
· Cable length (High Voltage Side) 17 ± 3
· Cable length (Low Voltage Side) 24 ± 3

※THE TOLERANCE THAT IS NOT SHOW: ± 0.5mm IN THE DRAWING

Rev.	prepared date	Revision contents	Approved	Checked	Prepared	Issued date
1	May. 26, 1998	DOD-H-6458			T. Kucanoga	–