NEC

TFT COLOR LCD MODULE
NL6448AC33-15

26 cm (10.4 type), 640×480 pixels Full colors, incorporated two-lamp/edge-light type backlight

DESCRIPTION

NL6448AC33-15 is a TFT (Thin Film Transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL6448AC33-5 has a built-in backlight.

The 26 cm diagonal display area contains 640 × 480 pixels and can display full colors simultaneously.

FEATURES

- ○ Full color (Analog RGB interface)
- ○ Multi scan fanction (VGA, PC9801, MAC, NTSC and PAL)
- ○ Reverse scan function
- ○ High luminous (200 cd/m^2) / Low reflection
- ○ Incorporated edge type backlight (Two lamps. Include Inverter)
- ○ Data enable function
- ○ Lamp holder replacable

APPLICATIONS

- ○ Personal computers (PC). Word processor
- ○ Display terminals for control system
- ○ Monitors for process controller

The information in this document is subject to change without notice.

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STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	211.2 (H) × 158.4 (V) mm
Drive system	a-Si TFT active matrix
Display colors	Full colors
Number of pixels	640 × 480
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.33 (H) × 0.33 (V) mm
Module size	251.0 (H) × 196.0 (V) × 18.0 typ. (D) mm
Weight	750 g (typ.)
Contrast ratio	150 : 1 (typ.)

Viewing angle (more than the contrast ratio of 10 : 1)

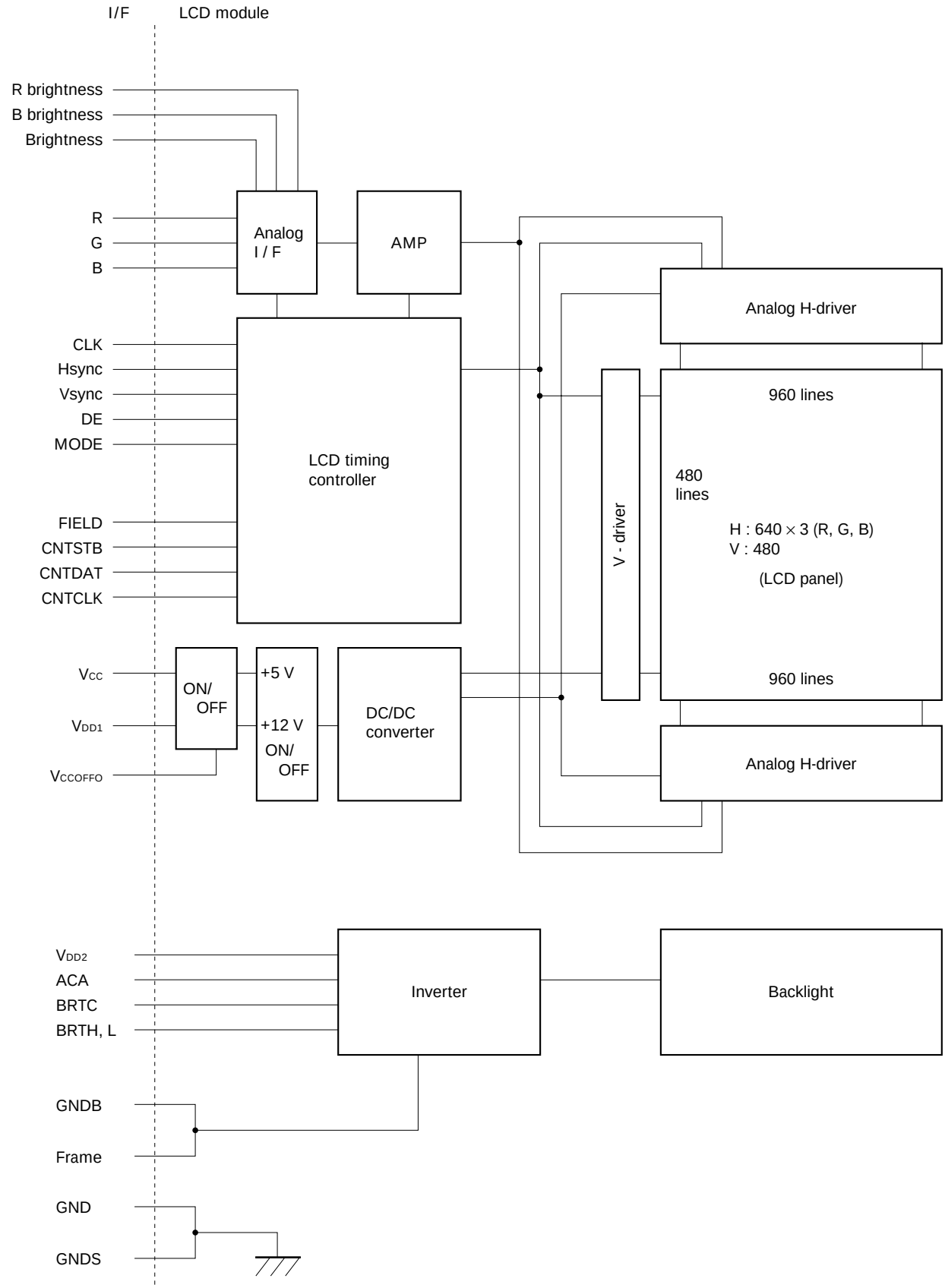
- Horizontal : 50° (typ. left side, right side)
- Vertical : 15° (typ. up side), 45° (typ. down side)

Designed viewing direction (Normal scanning)

- Wider viewing angle with contrast ratio : down side (6 o'clock)
- Wider viewing angle without image reversal : up side (12 o'clock)
- Optimum grayscale (γ = 2.2) : perpendicular

Color gamut	55% (typ. At center, To NTSC)
Response time	40 ms (max.), "white" to "black"
Luminance	200cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals (Hsync, Vsync), Dot clock (CLK)
Supply voltage	5.0 V, 12 V, 12 V
Backlight	Edge light type: Two fluorescent lamps (cold cathode type)
Power consumption	9.4 W (typ.)

BLOCK DIAGRAM



SPECIFICATIONS

1. GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	251.0±1.0 (H) × 196.0±1.0 (V) × 18.5 (D) (max.) (Inverter portion: 24.0 (D) (max.))	mm
Display area	211.2 (H) × 158.4 (V) 26 cm (10.4 type)	mm
Number of pixels	640 (H) × 480 (V)	dot
Dot pitch	0.11 (H) × 0.11 (V)	mm
Pixel pitch	0.33 (H) × 0.33 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	Full color	color
Weight	780 (max.)	g

note 1 :

2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD1}	0 to 15	V	Ta = 25°C
	V_{DD2}	0 to 15	V	
	V_{CC}	–0.3 to 6.0	V	
Logic signals input voltage Include brightness	V_{IN1}	–0.3 to VCC+0.3	V	
Analog RGB input voltage	V_{IN2}	–4.0 to 4.0	V	
Storage temp.	T_{ST}	–20 to 60	°C	–
Operating temp.	T_{OP}	0 to 50	°C	Module surface **note 1**
Humidity (No condensation)	R_H	≦95 % relative humidity	–	Ta≦40°C
		≦85 % relative humidity	–	40°C < Ta≦50°C
		Absolute humidity shall not exceed Ta = 50°C, 85% relative humidity level	–	50°C < Ta

note 1 : Measured at the display area

3. ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving

(Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	V_{DD1}	11.4	12.0	12.6	V	
	V_{CC}	4.75	5.0	5.25	V	
Logic input "L" voltage	V_{DIL}	0	–	0.8	V	
Logic input "H" voltage	V_{DIH}	2.2	–	V_{CC}	V	
Logic input "L" current 1	I_{IL1}	–1200	–	–	μA	CLK
Logic input "H" current 1	I_{IH1}	–	–	20	μA	**note1, note2**
Logic input "L" current 2	I_{IL2}	–1500	–	–	μA	VCCOFFO
Logic input "H" current 2	I_{IH2}	–	–	320	μA	**note1, note2**
Logic input "L" current 3	I_{IL3}	325	–	–	μA	VCCOFFO
Logic input "H" current 3	I_{IH3}	–	–	325	μA	**note1, note2**
Logic input "L" current 4	I_{IL4}	–20	–	–	μA	Hsync, Vsync DE, VUD, MODE CNTDAT, CNTSTB CNTCLK, FIELD
Logic input "H" current 4	I_{IH4}	–	–	325	μA	**note1, note2**
Logic input "L" current 5	I_{IL5}	–130	–	–	μA	R bright, Bbright Bright
Logic input "H" current 5	I_{IH5}	–	–	130	μA	**note1, note2**
Logic input "L" current 6	I_{IL6}	–90	–	–	μA	ACA
Logic input "H" current 6	I_{IH6}	–	–	10	μA	**note1, note2**
Logic input "L" current 7	I_{IL7}	–670	–	–	μA	BRTC
Logic input "H" current 7	I_{IH7}	–	–	80	μA	**note1, note2**
Video signal amplitude (max.) White-Black	V_{IRGB}	0	–	0.7	V_{p-p}	Zi = 75 Ω
Video dignal input range	V_{IdcRGB}	–2.5	–	2.5	V_{p-p}	**note1**
Supply current **note 3**	I_{DD1}	–	150	220	mA	**note1**
	I_{CC}	–	80	120	mA	**note1**

note 1 : IILx : V_I = GND, IIHx : V_I = V_{CC}

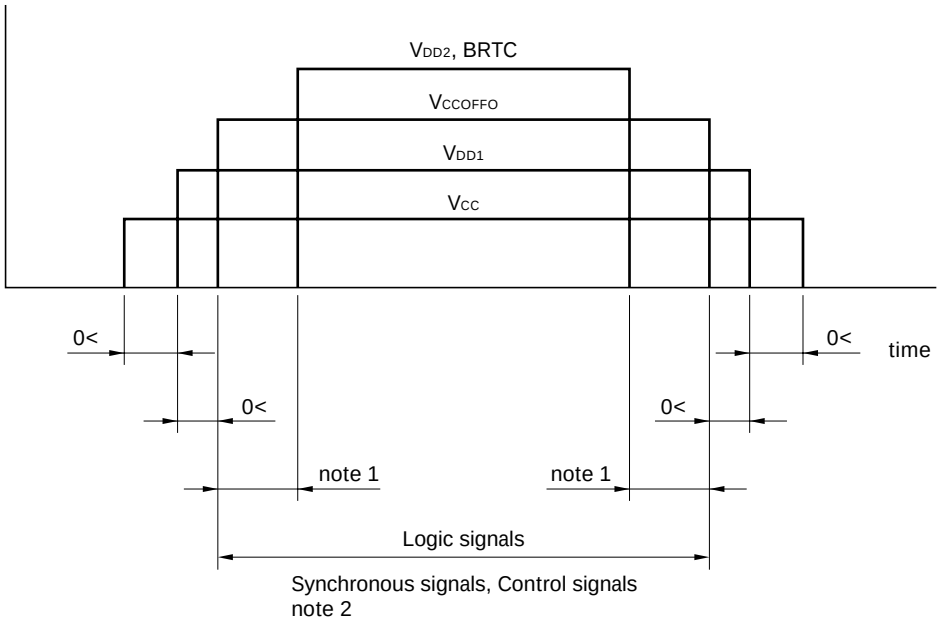
note 2 : Measured at the dot-checked pattern

(2) Back light

Ta = 25°C, Brightness : 100%

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	V_{DD2}	11.4	12.0	12.6	V	
Supply current	I_{DDB}	–	600	850	mA	VDD2 = 12.0 V Typical luminance
Logic input "L" voltage	V_{INL}	0	–	0.8	V	for BRTC, ACA terminal A base level : GNDB
Logic input "H" current	V_{INH}	2.2	–	5.5	V	
Logic input "L" current	I_{IL}	–1000	–	–	μA	for logic input terminal
Logic input "H" current	I_{IH}	–	–	1000	μA	for logic input terminal

4. SUPPLY VOLTAGE SEQUENCE



Caution

Wrong power sequence may damage to the module.

note 1 : BRTC (V_{DD2}) should operate after V_{CC}, V_{DD1} and V_{CCOFFO} input in the LCD module.
BRTC (V_{DD2}) had better be input the LCD module in more than 250 ms after V_{CCOFFO}, if you want to avoid an ununiformity display for a moment.

note 2 : Logic signals (Hsync, Vsync, CLK, DE, FIELD, MODE, CNTSEL, CNTDAT, CNTSTB, CNTCLK, CPSEL, CLAMP) should be "L"or "Open", when V_{CC} and V_{DD1} are not input.

note 3 : The ON / OFF switching of backlight should operate while Hsync, Vsync, CLK, DE (for DE mode) are supplied.
If the backlight power supply (V_{DD2}) is turn ON / OFF without logic signals, unstable data will be displayed.

note 4 : Analog RGB input are independent from this power supply sequence.

5. INTERFACE AND PIN CONNECTION

(1) Connector for logic signal and supply voltage

CN1 : IL–Z–10PL–SMTY

Adaptable socket : IL–Z-10S–S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

No.	Symbol	Function	No.	Symbol	Function
1	R	Red video signal	6	GNDS	Signal GND
2	GNDS	Signal GND	7	Hsync	Horizontal sync.
3	G	Green video signal	8	GNDS	Signal GND
4	GNDS	Signal GND	9	Vsync	Vertical sync.
5	B	Blue video signal	10	GNDS	Signal GND

note 1 : When V_{CCOFFO} is L or Open, V_{CC} and V_{DD1} are turned OFF.
When V_{CCOFFO} are H, V_{CC} and V_{DD1} are turned ON.

note 2 : The wire for the connector should use the shielded wire (AWG#28).

note 3 : Signal ground (GNDS) is separated from frame ground (front cover).

CN2 : IL–Z–13PL–SMTY

Adaptable socket : IL–Z–13S–S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

No.	Symbol	Function	No.	Symbol	Function
1	GND	Logic GND	8	V_{DD1}	Power supply
2	CLK	Dotclock	9	V_{DD1}	Power supply
3	GND	Logic GND	10	V_{CCOFFO}	ON/OFF for V_{CC},V_{DD1}
4	DE	Data enable	11	GND	Logic GND
5	VUD	Scanning select	12	V_{CC}	Power supply
6	GND	Logic GND	13	GND	Logic GND
7	MODE	Timing mode select			

note 1 : MODE
- L or Open = Fixed mode
- H = DE mode

note 2 : VUD
- L or Open = Normal scanning
  - Wider viewing angle without image reversal : Up side (12 o'clock)
  - Wider viewing angle with contrast ratio : Down side (6 o'clock)
- H = Reverse scanning
  - Wider viewing angle without image reversal : Down side (6 o'clock)
  - Wider viewing angle with contrast ratio : Up side (12 o'clock)

note 3 : Signal ground (GNDS) is separated from frame ground (front cover).

(2) Connector for display control

CN3 : IL–Z–11PL–SMTY

Adaptable socket : IL–Z-11S–S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

No.	Symbol	Function	No.	Symbol	Function
1	V_{DD2}	Supply voltage for back light (B / L)	7	ACA	Luminance select
2	V_{DD2}		8	BRTC	ON / OFF for B / L
3	V_{DD2}		9	BRTH	Luminance control
4	GNDB	B / L ground	10	BRTL	
5	GNDB		11	N. C.	– – –
6	GNDB				

note 1 : Backlight ground is connected with frame ground (front cover).

note 2 : N. C. (No connection) should be open.

CN4 : IL–Z–15PL–SMTY

Adaptable socket : IL–Z-15S–S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

No.	Symbol	Function	No.	Symbol	Function
1	GND	Logic GND	9	GND	Logic GND
2	CNTSEL	Control signal	10	FIELD	Field signal
3	CNTDAT	Control data	11	GND	Logic GND
4	CNTSTB	Latch pulse	12	N. C.	– – –
5	GND	Logic GND	13	R brightness	Brightness control for Red
6	CNTCLK	For control data	14	B brightness	Brightness control for Blue
7	N. C.	– – –	15	Brightness	Brightness control
8	N. C.	– – –			

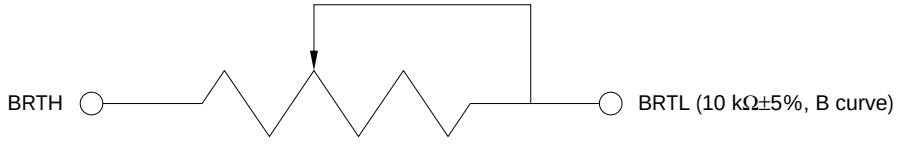
note 1 : Logic ground (GND) is separated from frame ground (front cover).

note 2 : N. C. (No connection) should be open.

(3) Detail of interface signal

Symbol	I/O	Logic	Description
R	I	Positive	Red video signal (0.7 Vp-p, 75 Ω)
G	I	Positive	Green video signal (0.7Vp-p, 75 Ω)
B	I	Positive	Blue video signal (0.7Vp-p, 75 Ω)
Hsync Vsync	I I	Negative Negative	Horizontal synchronous signal (TTL level) Vertical synchronous signal (TTL level)
CLK	I	Negative	Dot clock Timing signal for display data
DE	I	Positive	Data enable signal (TTL level) DE recognize video signals when MODE is "H" DE is controlled by MODE (Timing mode select)
FIELD	I	–	Field signal This signal judges the first field or the second field in NTSC / PAL signal input.
MODE	I	–	Timing mode select signal (TTL level) L or Open = Fixed mode H = DE mode
BRTH	I	–	Backlight luminance control Connect 10 K Ω variable resistor (∗1) or voltage control (∗2)
BRTL	I	–	
BRTC	I	Positive	Backlight ON/OFF control signal (TTL level) H or Open = Backlight ON L = Backlight OFF

note 1 : The variable resistor for luminance control should be 10 KΩ type, and zero point of the resistor corresponds to the minimum luminance.

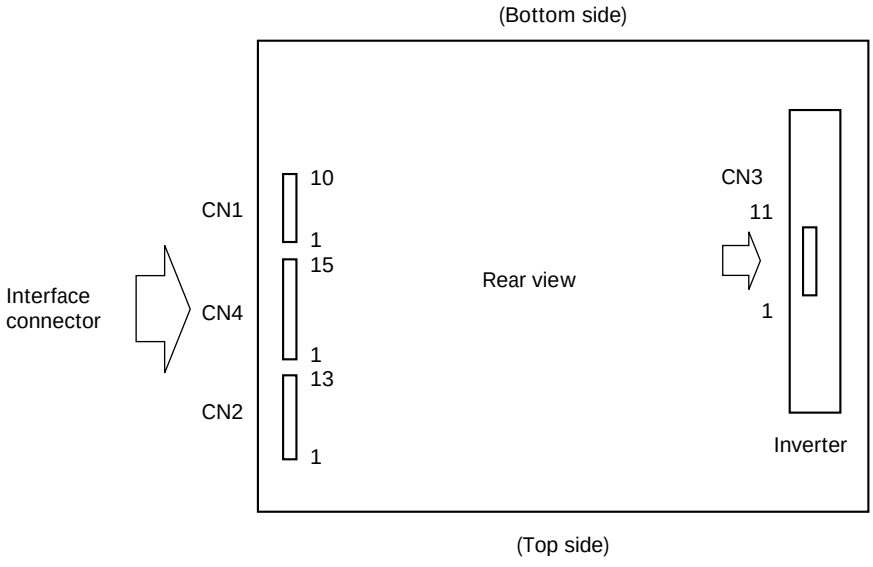


<Connection of the variable resistor to pins>

note 2 : In case of voltage control for brightness by BRTH / BRTL, at first, set BRTH to be "0" V And BRTL input voltage can control the brightness. When BRTL input voltage is "1 V" the luminance become maximum. And when its voltage is "0 V", the luminance becomes minimum.

Symbol	I/O	Logic	Description
ACA	I	Positive	Luminance select signal H or Open = Normal luminance L = Low luminance (1 / 2 of normal luminance)
V_{CCOFFO}	I	–	V_{CC} and V_{DD1} ON / OFF control signal (TTL level) H or Open = Power ON in LCD module. L = Power off in LCD module.
V_{CC}	–	–	Power supply voltage for Logic VCC = +5 V ± 5 %
V_{DD1}	–	–	Power supply voltage for LCD driving V_{DD1} = +12 V ± 5 %
GND	–	–	Logic ground for V_{CC} and V_{DD1}
GNDS	–	–	Signal ground for video, Hsync and Vsync GNDS should be separated from GND in order to avoid disturbing noise.
GNDB	–	–	Backlight ground
CNTSEL	I	–	Display control signal in case of serial communication. H or Open = Internal control (default) L = External control External control is set in CNTDAT, CNTCLK and CNTSTB.
CNTDAT	I	Positive	Display control data (serial data) (TTL level)
CNTCLK	I	Positive	CLK for display control data (TTL level)
CNTSTB	I	Positive	Latch pulse for display control data (TTL level)
Brightness	I	–	Input voltage for the tone of black (Refer to BRIGHTNESS CONTROL)
R Brightness	I	–	Input voltage for the tone of black in red (Refer to BRIGHTNESS CONTROL)
B Brightness	I	–	Input voltage for the tone of black in blue (Refer to BRIGHTNESS CONTROL)

(4) Interface pin connection



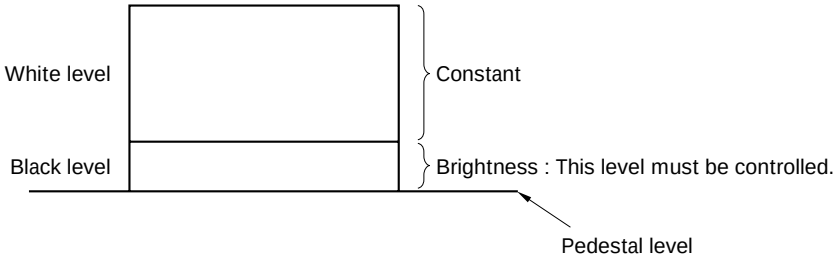
6. BRIGHTNESS CONTROL

The brightness control can adjust the tone of black. This function is used for making the white balance of each color by users. When the balance is adjusted, each voltage should not be changed. The brightness terminals should be opened in case of not using them.

Brightness controls the total level of black for R, G and B.

R/G brightness controls the black level of each color.

R/G brightness controls the differetiation of black level which is determined by Brightness.



Input voltage Unit : Volt

Sign	Min.	Typ.	Max.
Brightness	2.2	3.2	4.2
R brightness	–	3.0	–
B brightness	–	3.0	–

Control range

R brightness	–0.1 V≦ (Brightness – R brightness) ≦ 0.4 V
B brightness	–0.1 V≦ (Brightness – B brightness) ≦ 0.4 V

7. CONTROL DATA

Using the serial data, following functions can be utilized as follows.

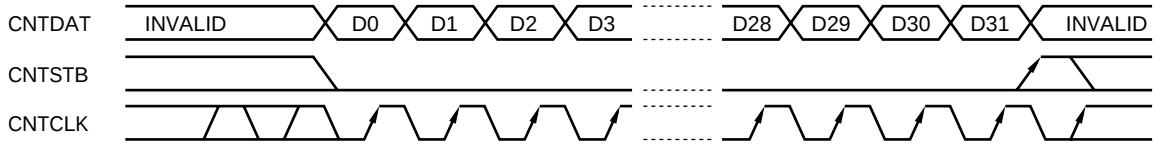
(1) The set of display mode : Table 1.
(2) The display-position adjustment(Horizontal) : Table 2.
(3) The display-position adjustment(Vertical) : Table 3.
(4) CLK•DELAY : Table 4.
(5) Under-scan mode : Table 5 and 6.
(6) Masking mode : Table 7.

CNTSEL = “L” : Above functions are effective.
CNTSEL = “H” or “Open” : Internal fixed value (default) is effective

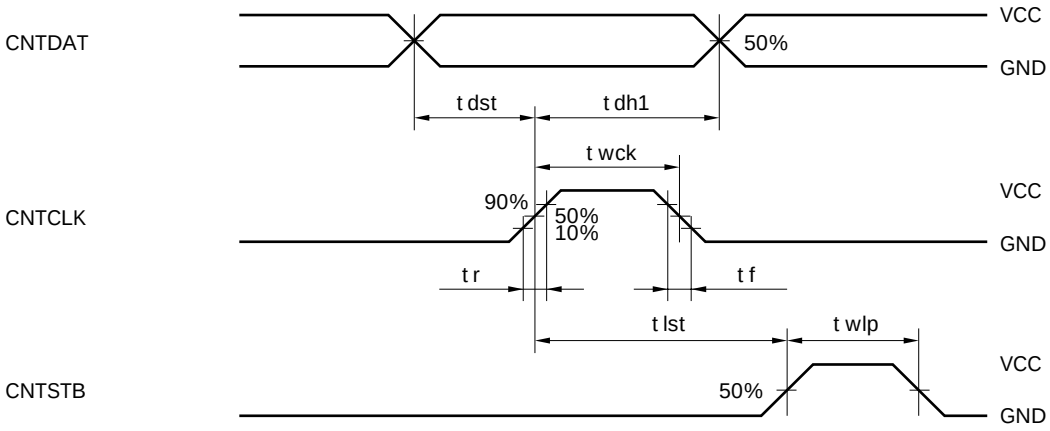
After serial data are transferred into the module, it is latched by CNTSTB. The above functions are effective after the data is latched.

Please keep CNTSTB to be "L" during transferring data. The serial data can be changed at any time, however, the display may be interrupted. We recommend that the backlight is turned-off by RBTC signal during changing the serial data.

Serial communication timing and waveform



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse width	twck	50	–	ns	CNTCLK
CLK frequency	fclk	–	5	MHz	
DATA setup-time	tdst	50	–	ns	CNTDAT
DATA hold-time	tdhl	50	–	ns	
Latch-pulse width	twlp	50	–	ns	CNTSTB
Latch setup-time	tlst	50	–	ns	
Rise/Fall time	tr, tf	–	50	ns	CNT×××



CNTDAT composition

Data	Data name	Function	
D0	USC0	Line position for single-scan	see table 6
D1	USC1	Line position for single-scan	
D2	USC2	Line position for single-scan	
D3	MOD0	Display mode selection	see table 1
D4	MOD1	Display mode selection	
D5	MOD2	Display mode selection	
D6	MOD3	Display mode selection	
D7	USCAN	Under-scan selection	see table 5 and 6
D8	HD0	Horizontal display position (LSB)	see table 3
D9	HD1	Horizontal display position	
D10	HD2	Horizontal display position	
D11	HD3	Horizontal display position	
D12	HD4	Horizontal display position	
D13	HD5	Horizontal display position	
D14	HD6	Horizontal display position	
D15	HD7	Horizontal display position (MSB)	
D16	VD0	Vertical display position (LSB)	see table 2
D17	VD1	Vertical display position	
D18	VD2	Vertical display position	
D19	VD3	Vertical display position	
D20	VD4	Vertical display position	
D21	VD5	Vertical display position (MSB)	
D22	MSK0	Masking mode selection	see table 7
D23	MSK1	Masking mode selection	
D24	–	–	Input data should be “H” or “L”
D25	–		
D26	–		
D27	DELY0	CLK delay (LSB)	see table 4
D28	DELY1	CLK delay	
D29	DELY2	CLK delay	
D30	DELY3	CLK delay	
D31	DELY4	CLK delay (MSB)	

LSB : Least Significant Bit
MSB : Most Significant Bit

Table 1 Display mode selection (MOD0 to 3 : 4 bit)

MOD3	MOD2	MOD1	MOD0	Display mode	Mode No.	Remark
0	0	0	0	VGA (640 × 480)	0	640 × 480
0	0	0	1	VGA (640 × 400)	1	640 × 400
0	0	1	0	PC9801 (640 × 480)	2	640 × 480
0	0	1	1	PC9801 (640 × 400)	3	640 × 400
0	1	0	0	MAC	4	640 × 480
0	1	0	1	NTSC	5	–
0	1	1	0	PAL	6	–
0	1	1	1	Invalidity	7 to 15	Same as mode 0
1	X	X	X			

Table 2 Vertical display position (VD0 to VD5 : 6 bit)

VD5	VD4	VD3	VD2	VD1	VD0	Vertical display position ∗**1**		
						Mode 0, 2, 4	Mode 5, 6	Mode 1, 3
0	0	0	0	0	0	Prohibit		
0	0	0	0	0	1			
0	0	0	0	1	0			
0	0	0	0	1	1			
0	0	0	1	0	0	4		
•	•	•	•	•	•	•		
•	•	•	•	•	•	•		
•	•	•	•	•	•	•		
1	0	0	1	1	1	39		
1	0	1	0	0	0	40		
1	0	1	0	0	1	41		Prohibit
•	•	•	•	•	•	•		
•	•	•	•	•	•	•		
1	1	1	1	1	0	62		
1	1	1	1	1	1	63		

note 1 : This is vertical line number from Vsync-fall to effective VIDEO signal (tvp + tvb).

Table 3 Horizontal display position (HD0 to HD7 : 8 bit)

HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal display position ∗**1**
0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	1	
0	0	0	0	0	0	1	0	
•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	
0	0	0	1	1	1	0	0	
0	0	0	1	1	1	0	1	29
0	0	0	1	1	1	1	0	30
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

note 1 : This is horizontal line number from Hsync-fall to effective VIDEO signal (thp + thb).

Table 4 Clock (CLK) delay (DELAY0 to DELAY5 : 5 bit)

DELAY5	DELAY3	DELAY2	DELAY1	DELAY0	Delay value [ns]	
					Mode 1, 2, 3, 4	Mode 5, 6
0	0	0	0	0	(0)	(0)
0	0	0	0	1	(1.5)	(2.0)
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	1	1	0	(45.0)	(60.0)
1	1	1	1	1	(46.5)	(62.0)

note 1 : Delay value is approximate.

Table 5 Under-scan selection

USCAN	Function
1	Under-scan ON
0	Under-scan OFF

note 1 : Under-scan is effective in display mode No.5 or 6.
note 2 : A line of single-scan is every sixth line in NTSC mode.
(Vertical magnification : 11/6)
note 3 : Six lines of single-scan is every thirteen line in PAL mode.
(Vertical magnification : 20/13)
note 4 : Single-scan position of NTSC mode is mentioned in table 6.

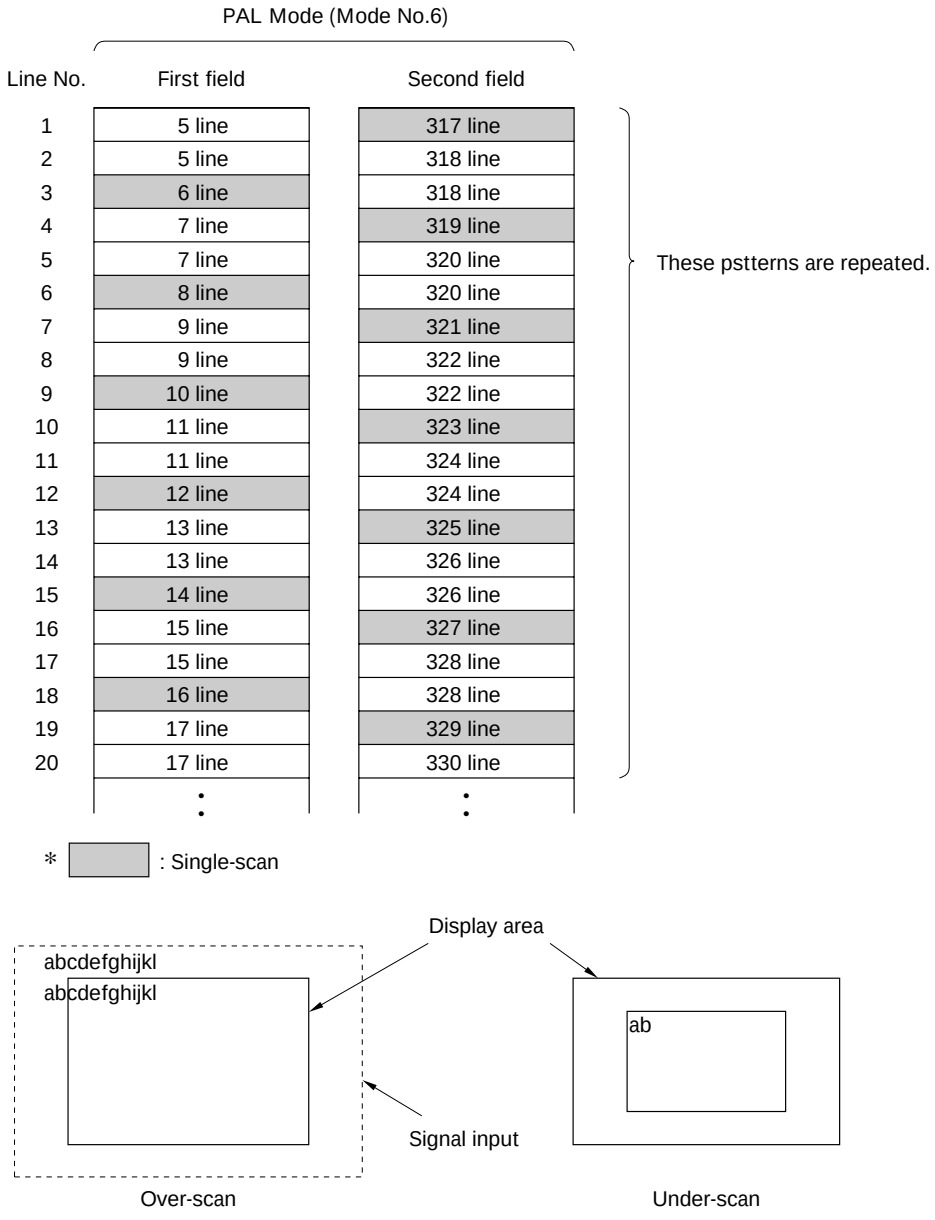


Table 6 Single-scan position (NTSC mode (Mode No. 5) in Under-scan)

Line No.	USC [2, 1, 0]									
	[0, 0, 0]		[0, 0, 1]		[0, 1, 0]		[0, 1, 1]		[1, 0, 0]	
	1'st	2'nd	1'st	2'nd	1'st	2'nd	1'st	2'nd	1'st	2'nd
1	8	8	8	8	8	8	8	8	8	8
2	8	9	8	9	8	9	8	9	8	9
3	9	9	9	9	9	9	9	9	9	9
4	9	10	9	10	9	10	9	10	10	10
5	10	10	10	10	10	10	10	10	10	11
6	10	11	10	11	10	11	11	11	11	11
7	11	11	11	11	11	11	11	12	11	12
8	11	12	11	12	12	12	12	12	12	12
9	12	12	12	12	12	13	12	13	12	13
10	12	13	13	13	13	13	13	13	13	13
11	13	13	13	14	13	14	13	14	13	14
12	14	14	14	14	14	14	14	14	14	14
13	14	15	14	15	14	15	14	15	14	15
14	15	15	15	15	15	15	15	15	15	15
15	15	16	15	16	15	16	15	16	16	16
16	16	16	16	16	16	16	16	16	16	17
17	16	17	16	17	16	17	17	17	17	17
18	17	17	17	17	17	17	17	18	17	18
19	17	18	17	18	18	18	18	18	18	18
20	18	18	18	18	18	19	18	19	18	19
21	18	19	19	19	19	19	19	19	19	19
22	19	19	19	20	19	20	19	20	19	20
23	20	20	20	20	20	20	20	20	20	20
24	20	21	20	21	20	21	20	21	20	21
25	21	21	21	21	21	21	21	21	21	21

∗ ▭ : Single-scan

note 1: The position of single-scan is able to be changed by USC [2, 1, 0]

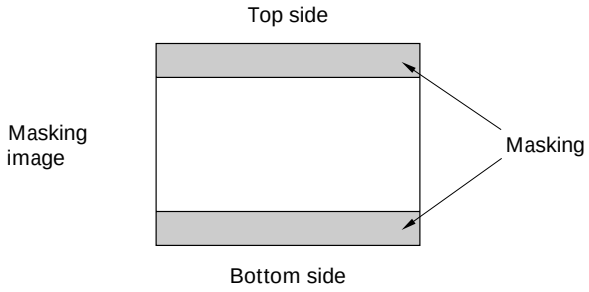
Table 7 Masking mode (Top and bottom side)

MSK1	MSK0	Mode selection (Top and bottom side)
0	0	Without masking
0	1	Each side : 40 lines
1	0	Each side : 12 lines

note 1 : Though the display position can be changed with HD (Horizontal display position) or VD (Vertical display position), the masking position can not change.

note 2 : Masking mode is effective in the Mode No.5 or 6. (Refer to table 1)

note 3 : Masking mode is not effective in under-scan.



8. INPUT SIGNAL TIMING (a)

(1) VGA–640 × 480 pixels (Mode No.0)

CNTSEL = "H" or "OPEN" (Internal control : Standard mode)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	39.722 ns	25.175 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	31.778 μs	31.469 kHz	800CLK
	Display period	thd	25.422 μs	—	640CLK
	Front-porch	thf	0.636 μs	—	16CLK
	Pulse-width	thp	3.813 μs	—	96CLK
	Back-porch	thb	1.907 μs	—	48CLK
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	16.683 ms	59.94 Hz	525H
	Display period	tvd	15.253 ms	—	480H
	Front-porch	tvf	0.350 ms	—	11H
	Pulse-width	tvp	0.063 ms	—	2H
	Back-porch	tvb	1.017 ms	—	32H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

(2) VGA–640 × 400 pixels (Mode No.1)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	39.722 ns	25.175 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	31.778 μs	31.469 kHz	800CLK
	Display period	thd	25.422 μs	—	640CLK
	Front-porch	thf	0.636 μs	—	16CLK
	Pulse-width	thp	3.813 μs	—	96CLK
	Back-porch	thb	1.907 μs	—	48CLK
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	14.268 ms	70.09 Hz	449H
	Display period	tvd	12.711 ms	—	400H
	Front-porch	tvf	0.381 ms	—	12H
	Pulse-width	tvp	0.063 ms	—	2H
	Back-porch	tvb	1.112 ms	—	35H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

(3) PC9801–640 × 480 pixels (Mode No.2)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	39.722 ns	25.175 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	31.778 μs	31.469 kHz	800CLK
	Display period	thd	25.422 μs	—	640CLK
	Front-porch	thf	0.636 μs	—	16CLK
	Pulse-width	thp	3.813 μs	—	96CLK
	Back-porch	thb	1.907 μs	—	48CLK
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	16.683 ms	59.94 Hz	525H
	Display period	tvd	15.253 ms	—	480H
	Front-porch	tvf	0.191 ms	—	6H
	Pulse-width	tvp	0.063 ms	—	2H
	Back-porch	tvb	1.176 ms	—	37H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

(4) PC9801–640 × 400 pixels (Mode No.3)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	47.5 ns	21.0526 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	40.28 μs	24.83 kHz	848CLK
	Display period	thd	30.4 μs	—	640CLK
	Front-porch	thf	3.04 μs	—	64CLK
	Pulse-width	thp	3.04 μs	—	64CLK
	Back-porch	thb	3.08 μs	—	80CLK
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	17.723 ms	56.42 Hz	440H
	Display period	tvd	16.112 ms	—	400H
	Front-porch	tvf	0.282 ms	—	7H
	Pulse-width	tvp	0.322 ms	—	8H
	Back-porch	tvb	1.007 ms	—	25H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

(5) MAC (Mode No.4)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	33.069 ns	30.240 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	28.571 μs	35.000 kHz	864CLK
	Display period	thd	21.164 μs	—	640CLK
	Front-porch	thf	2.116 μs	—	64CLK
	Pulse-width	thp	2.116 μs	—	64CLK
	Back-porch	thb	3.175 μs	—	96CLK
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	15.000 ms	66.667 Hz	525H
	Display period	tvd	13.714 ms	—	480H
	Front-porch	tvf	0.086 ms	—	3H
	Pulse-width	tvp	0.086 ms	—	3H
	Back-porch	tvb	1.114 ms	—	39H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

(6) NTSC (Mode No.5)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	79.443 ns	12.5875 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	63.556 μs	15.734 kHz	800CLK
	Display period	thd	50.844 μs	—	640CLK
	Pulse-width	thp	4.7 μs	—	(59CLK)
	thp + thb	–	9.7 μs	—	(122CLK)
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	16.683 ms	59.94 Hz	262.5H
	Display period	tvd	15.253 ms	—	240H
	Pulse-width	tvp	0.191 ms	—	3H
	thp + thb	–	1.080 ms	—	17H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—
FIELD	Period	tf	33.367 ms	29.97 Hz	—
	Vsync-Field timing	tfh	1 Hsync (Min.)	—	—
	Field-Vsync timing	tfs	1 Hsync (Min.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

Display line of MTSC

(Vertical Display Position = 17)

LCD-line No.	(a) First field	(b) Second field
1	21 line	284 line
2	21 line	285 line
3	22 line	285 line
4	22 line	286 line
5	23 line	286 line
. . .	. . .	. . .
478	259 line	523 line
479	260 line	523 line
480	260 line	524 line

(7) PAL (Mode No.6)

Parameter		Symbol	Time	Frequency	Remark
CLK	Frequency	l / tc	79.443 ns	12.5875 MHz	—
	Duty	tch / tc	0.4 to 0.6	—	—
	Rise / Fall	tcrf	10 ns (Max.)	—	—
Hsync	Period	th	64.0 μs	15.625 kHz	805CLK
	Display period	thd	50.8 μs	—	640CLK
	Pulse-width	thp	4.7 μs	—	(59CLK)
	thp + thb	–	9.7 μs	—	(122CLK)
	Hsync-Vsync timing	thvh	1 CLK (Min.)	—	—
	Vsync-Hsync timing	thvs	8 ns (Min.)	—	—
	Rise / Fall	thrf	10 ns (Max.)	—	—
Vsync	Period	tv	16.683 ms	50.00 Hz	312.5H
	Display period	tvd	15.253 ms	—	287H
	Pulse-width	tvp	0.191 ms	—	3H
	thp + thb	–	1.208 ms	—	27H
Analog RGB Signal	RGB setup timing	trgbs	10 ns (Min.)	—	**note 1**
	RGB hold timing	trgbh	10 ns (Min.)	—	
DE	DE-CLK timing	tes	8 ns (Min.)	—	—
	CLK-DE timing	teh	8 ns (Min.)	—	—
	Rise / Fall	terf	10 ns (Max.)	—	—
FIELD	Period	tf	33.367 ms	29.97 Hz	—
	Vsync-Field timing	tfh	1 Hsync (Min.)	—	—
	Field-Vsync timing	tfs	1 Hsync (Min.)	—	—

note 1 : Except for display period (thd, tvd), analog RGB signal should be black level.

Display line of PAL

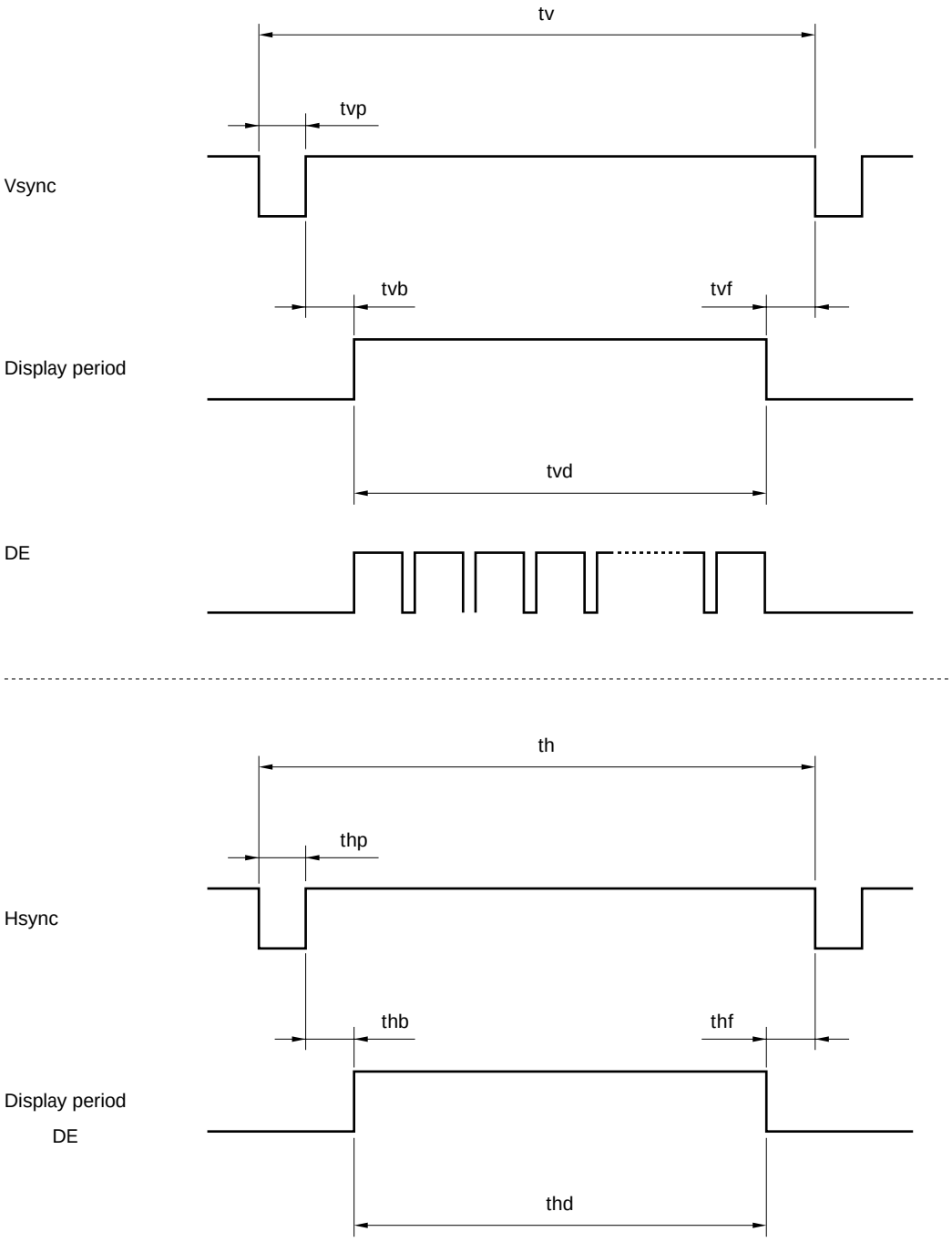
(Vertical Display Position = 27)

LCD-line No.	(a) First field	(b) Second field
1	28 line	340 line
2	28 line	341 line
3	29 line	341 line
4	29 line	342 line
5	30 line	342 line
6	31 line	343 line
7	31 line	344 line
8	32 line	344 line
9	32 line	345 line
10	33 line	345 line
11	33 line	346 line
12	34 line	346 line
13	35 line	347 line
14	35 line	348 line
15	36 line	348 line
. . .	. . .	. . .
478	306 line	618 line
479	306 line	619 line
480	307 line	619 line

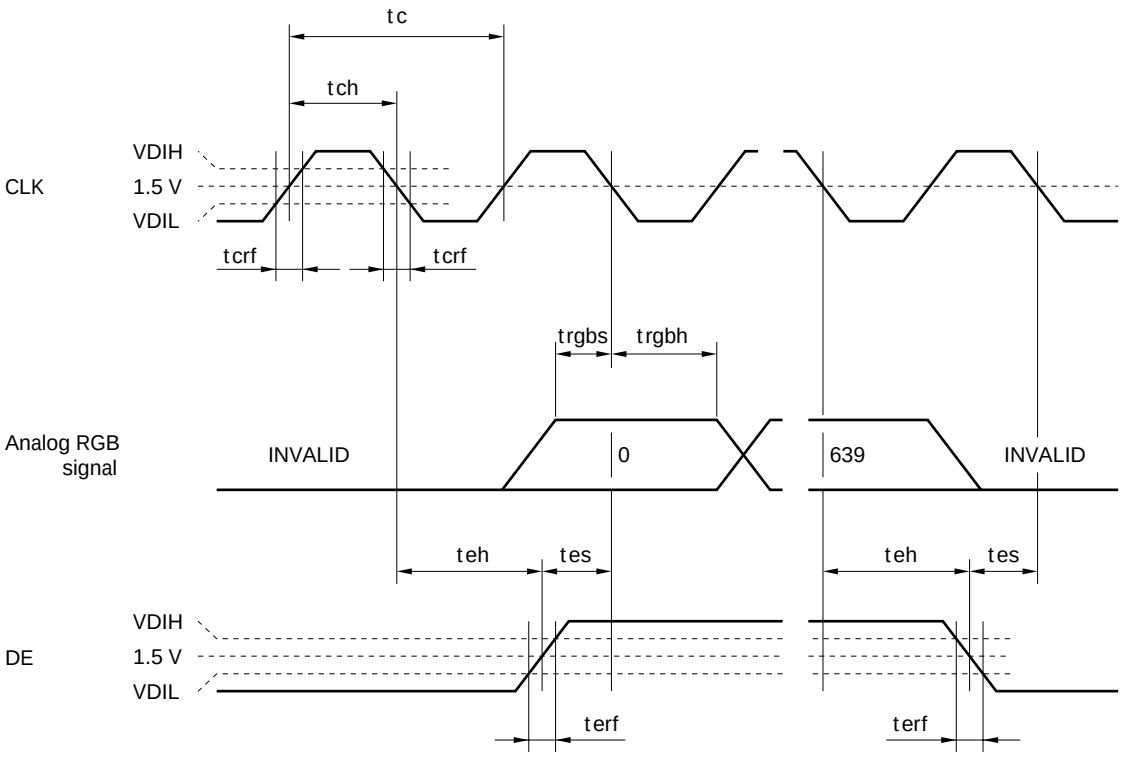
* ☐ : Single-scan

note : Single-scan is repeated every third line or every fourth line.

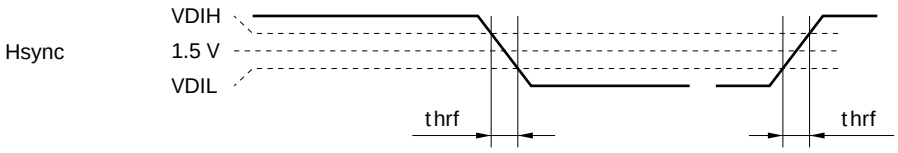
9. INPUT SIGNAL TIMING (b)



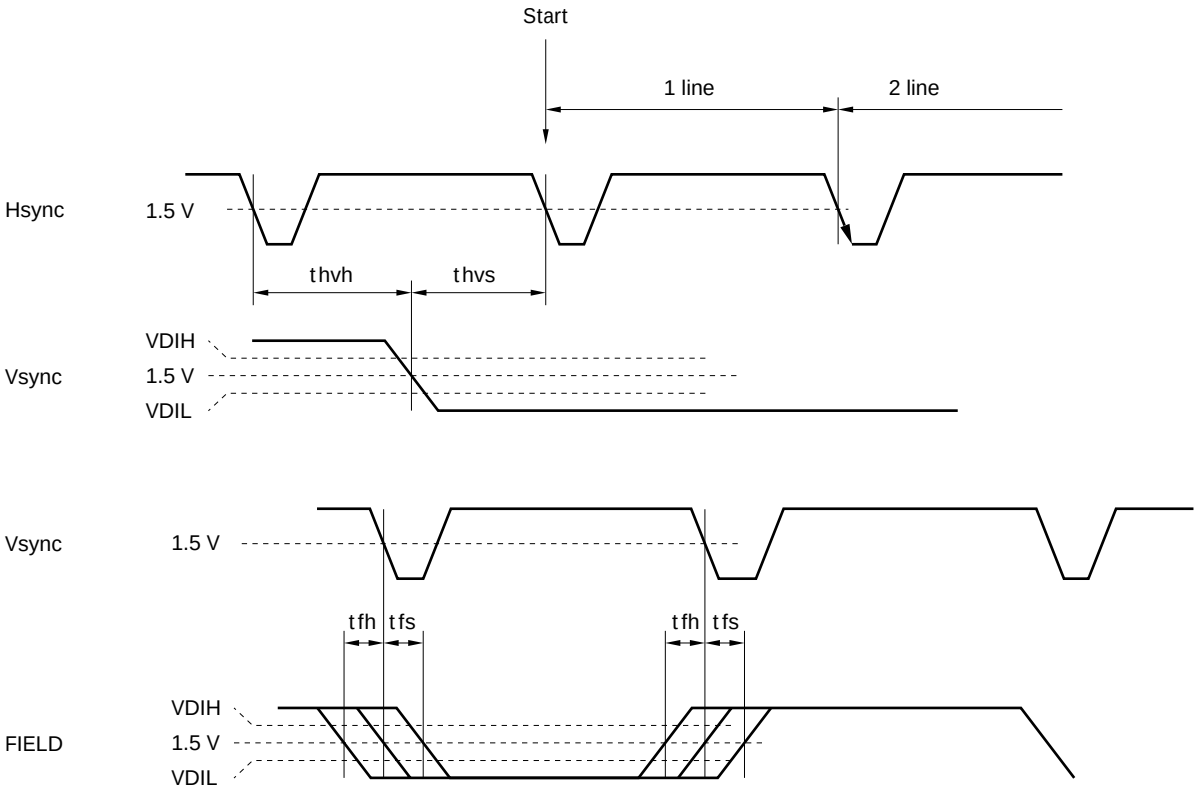
Display period: These do not exist signals.



note: Analog RGB signal should be black level in INVALID.



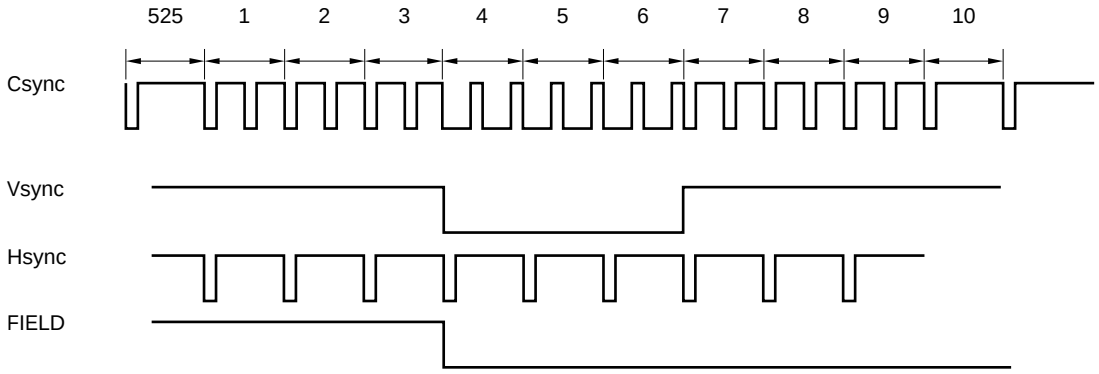
VDIH = 2.2 V to V_{CC}
VDIL = 0 to 0.8 V



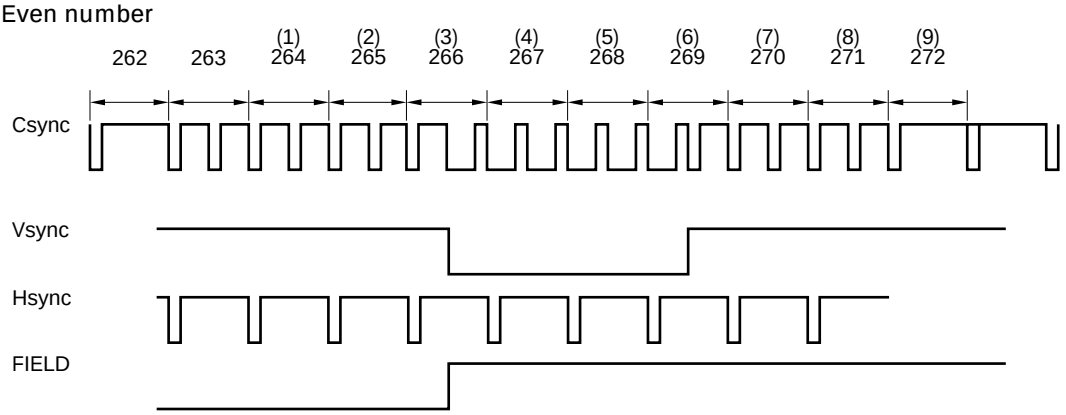
VDIH = 2.2 V to V_{CC}
VDIL = 0 to 0.8 V

10. DEFINITION OF LINE NUMBERS IN NTSC MODE

(1) Odd number field

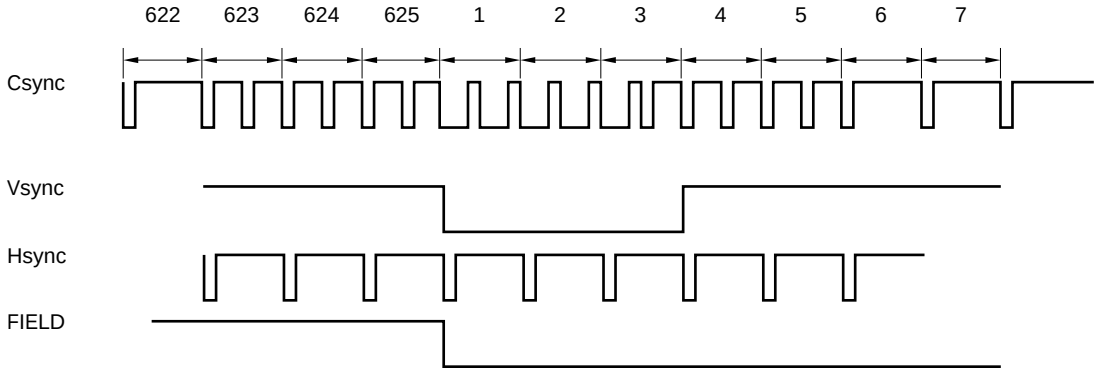


(2) Even number

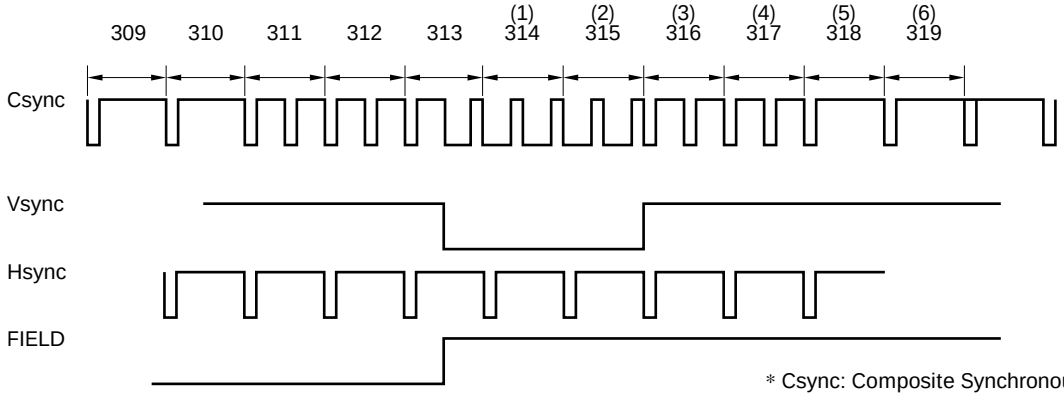


11. DEFINITION OF LINE NUMBERS IN PAL MODE

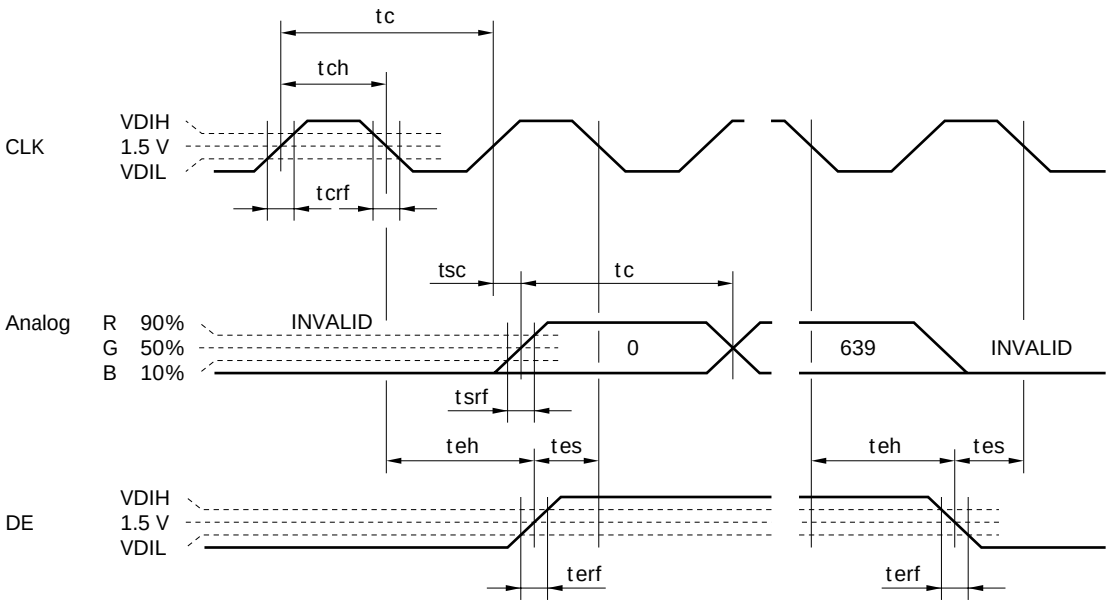
(1) Odd number field

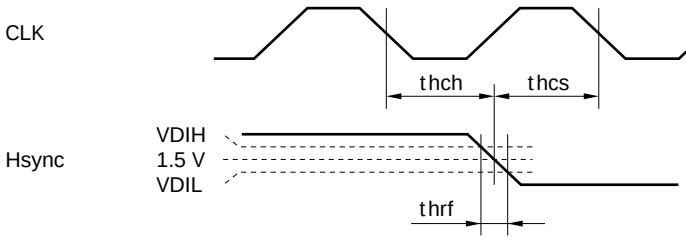


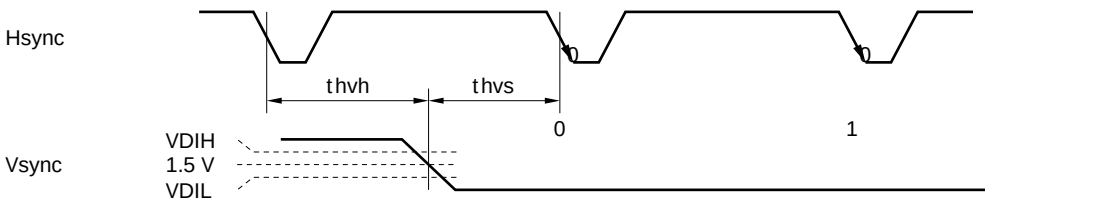
(2) Even number field

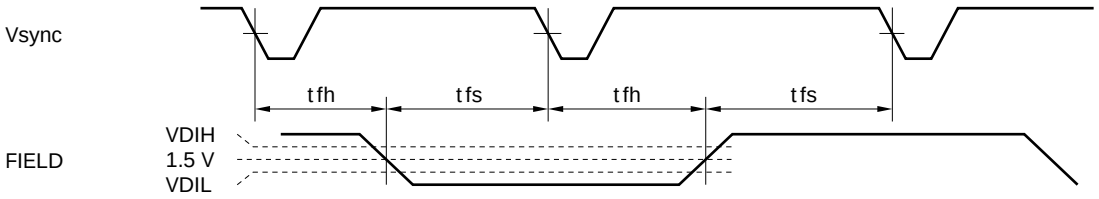


* Csync: Composite Synchronous Signal







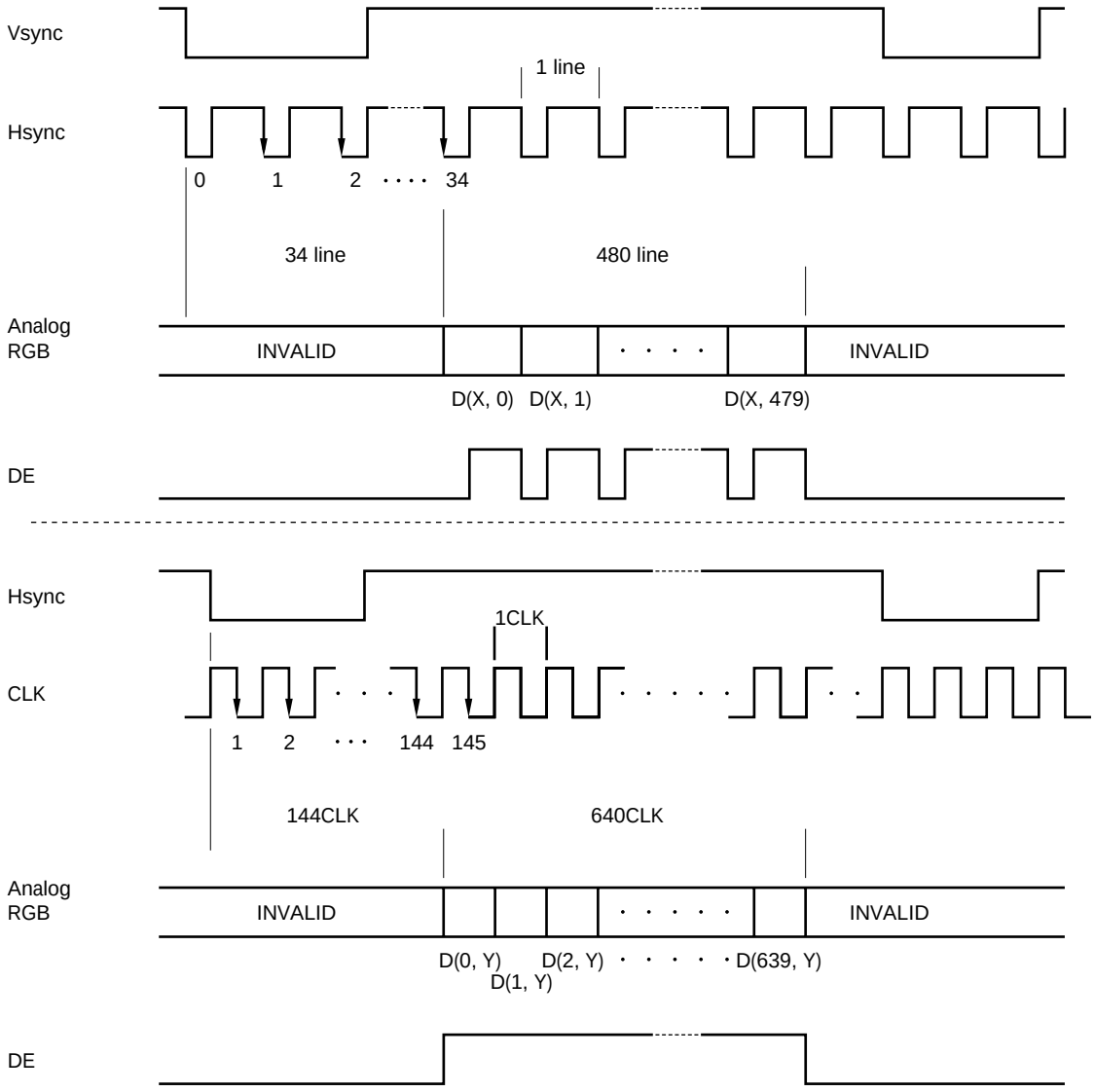


note: Analog RGB signal should be black level in INVALID.

VDIH = 2.2 V to V_{CC}
VDIL = 0 to 0.8 V

12. INPUT SIGNAL AND DISPLAY POSITION (VGA-640 × 480 pixels: Default)

Mode No.0 (Refer to Table 1)



note: Analog RGB signal should be black level in INVALID

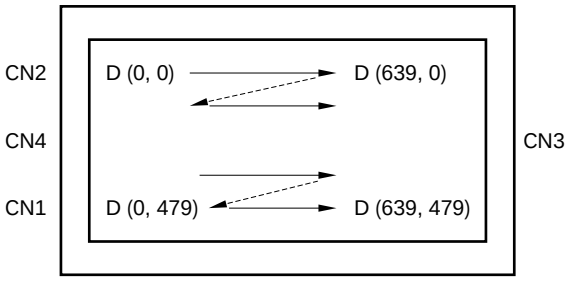
Display (Normal scanning) D (X, Y)

D (0, 0)	D (1, 0)	D (2, 0)	· · · · · ·	D (639, 0)
D (0, 1)	D (1, 1)			
D (0, 2)				
· · · ·				· · · ·
D (0, 479)	D (1, 479)	D (2, 479)	· · · · · ·	D (639, 479)

Display (Reverse scanning) D (X, Y)

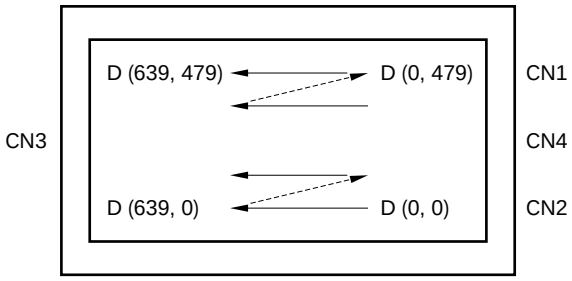
D (639, 479)	D (638, 479)	D (637, 479)	· · · · · ·	D (0, 479)
D (639, 478)	D (638, 478)			
D (639, 477)				
· · · ·				· · · ·
D (639, 0)	D (638, 0)	D (637, 0)	· · · · · ·	D (0, 0)

Normal scanning



Wider viewing angle without image reversal: Up side view

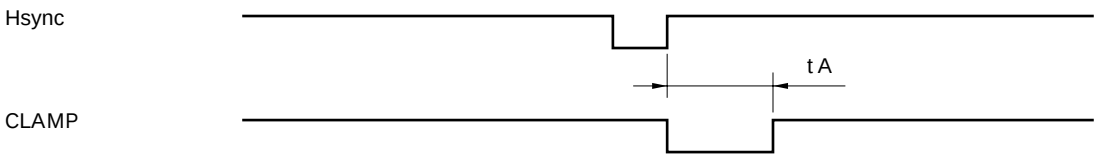
Reverse scanning



Wider viewing angle without image reversal: Down side view

13. CLAMP PULSE

CLAMP pulse define the black level of analog RGB signals.



MOD3	MOD2	MOD1	MOD0	Mode	t A [CLK]
0	0	0	0	VGA (480)	18
0	0	0	1	VGA (400)	18
0	0	1	0	PC98 (480)	18
0	0	1	1	PC98 (400)	15
0	1	0	0	MAC	18
0	1	0	1	NTSC	10
0	1	1	0	PAL	10

note: The black level of analog RGB signal in CLAMP is basis. And noise signals should not be input because of avoiding the display ununiformity.

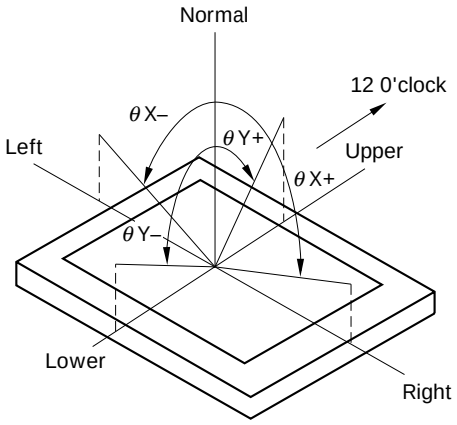
14. OPTICAL CHARACTERISTICS

Ta = 25°C **note 1**

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ x+	CR>10, θ y = ±0°	40	50	–	deg.	note 2
		θ x–	CR>10, θ y = ±0°	40	50	–	deg.	
	Vertical	θ x+	CR>10, θ x = ±0°	10	15	–	deg.	
		θ x–	CR>10, θ x = ±0°	40	45	–	deg.	
Contrast ratio		CR	note 3	80	150	–	–	note 4
Response time		tpd	white to black	–	15	40	ms	note 5
Color gamut		C	at center, to NTSC	40	55	–	%	–
Luminance		Lu	note 3	150	200	–	cd / m²	note 6
Brightness uniformity		–	max. / min.	–	–	1.25	–	note 7

note 1 : V_{CC} = 5.0 V, V_{DD1} = 12.0 V, V_{DD2} = 12.0 V

note 2 : Definitions of viewing angle are as follows.



note 3 : Viewing angle is θ x = ±0°, θ y = ±0°. At center.

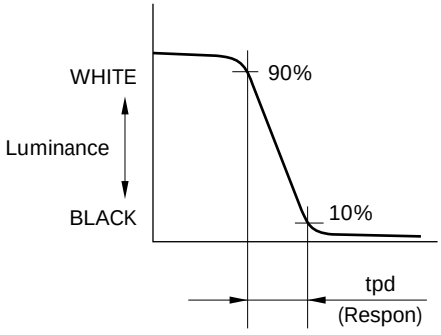
note 4 : The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness (Luminance) with all pixels in “white”}}{\text{Brightness with all pixels in “black”}}$$

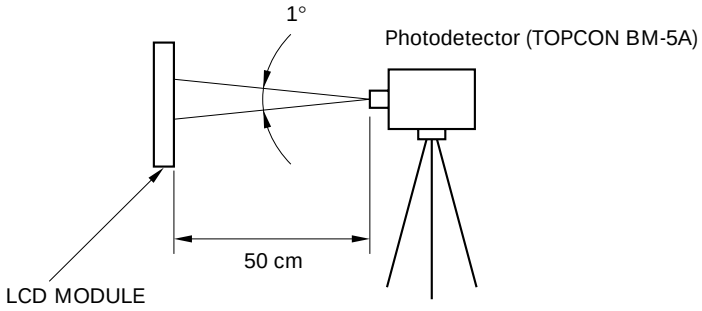
The brightness is measured in darkroom.

note 5 : Definition of response time is as follows.

Photodetector output signal is measured when the brightness changes "white" to “black”. Response time is the time between 10% and 90% of the photodetector output amplitude.



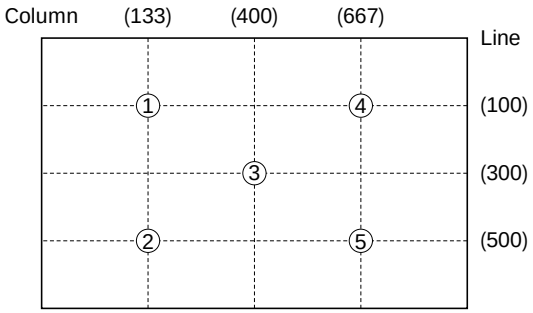
note 6 : The luminance is measured after 20 minutes from the module works, with all pixels in "white".



note 7 : The brightness uniformity is calculated by using following formula.

$$\text{Brightness uniformity} = \frac{\text{Maximum Brightness}}{\text{Minimum Brightness}}$$

The brightness is measured at near the five points shown below.



Next figures and sentence are very Important, please understand these contents as follows.

CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you wlll get an electric shock when you make a mistake to operate.
	This figure is a mark that the LCD module will give out smoke or eatch fire when you make a mistake to operate.
	This figure Is a mark that you will get hurt when you make a mlstake to operate

CAUTION

Do not touch an Inverter --on which is stuck a caution label-- while the LCD module is under the operatlon, because of dangerous high voltage.

(1) Caution when taking out the module

<1> Pick the pouch only, in taking out module from a carrier box.

(2) Caution for handling the module

<1> As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatlc discharges.

<2> As the LCD panel and backllght element are made from fragjle glass material, Impulse and pressure to the LCD module should be avoided.

<3> As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

<4> Do not pull the interface connectors in or out while the LCD module is operating.

<5> Put the module display side down on a flat horizontal plane.

<6> Handle connectors and cables with care.

<7> When the module is operating, do not lose CLK, Hsync, or Vsync slgnal. If any one of these signals is lost, the LCD panel would be damaged.

<8> Obey the supply voltage sequence. If wrong sequence is applied, the module wouldbe damaged.

<9> The torque to nrounting screw should never exceed 0.294 N•m (3 Kgf•cm).

(3) Caution for the atmosphere

<1> Dew drop atmosphere should be avoided.

<2> Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packlng pouch and under relatively low temperature atmosphere Is recommended.

<3> This module uses cold cathod fluorescent lamp. Therefore, The life time of lamp becomes short conspicuously at low temperature.

<4>  Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

<1> Do not apply fixed pattern data signal to the LCD module at product agjng. Applying fixed pattern for a long time may cause image sticking.

(5)Other cautions

<1> Do not disassemble and/or reassemble LCD module.

<2> Do not readjust variable resistor or switch etc.

<3> When returning the module for repair or etc, please pack the module not to be broken. We recommend to the original shipping packages.

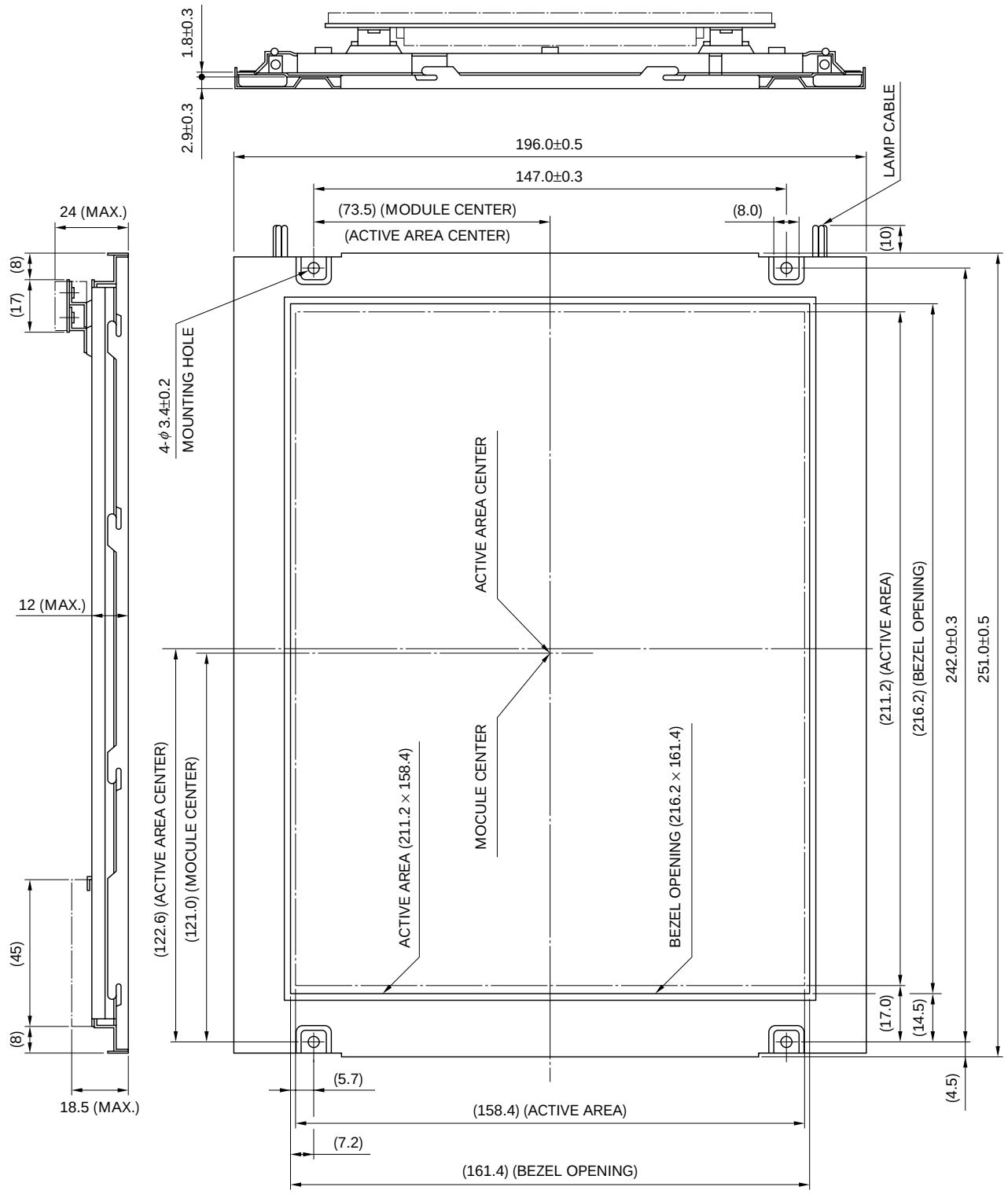
<4> Turn off the power supply to avoid electrical shock while backlight lamp is replaced, and the backlight replace manual.

Liquid Crystal Dlsplay has the following specific characteristics. There are not defects or malfunctions.

The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tube for backlightlng. Optical characteristics, like luminance or uniformity, will change during time.

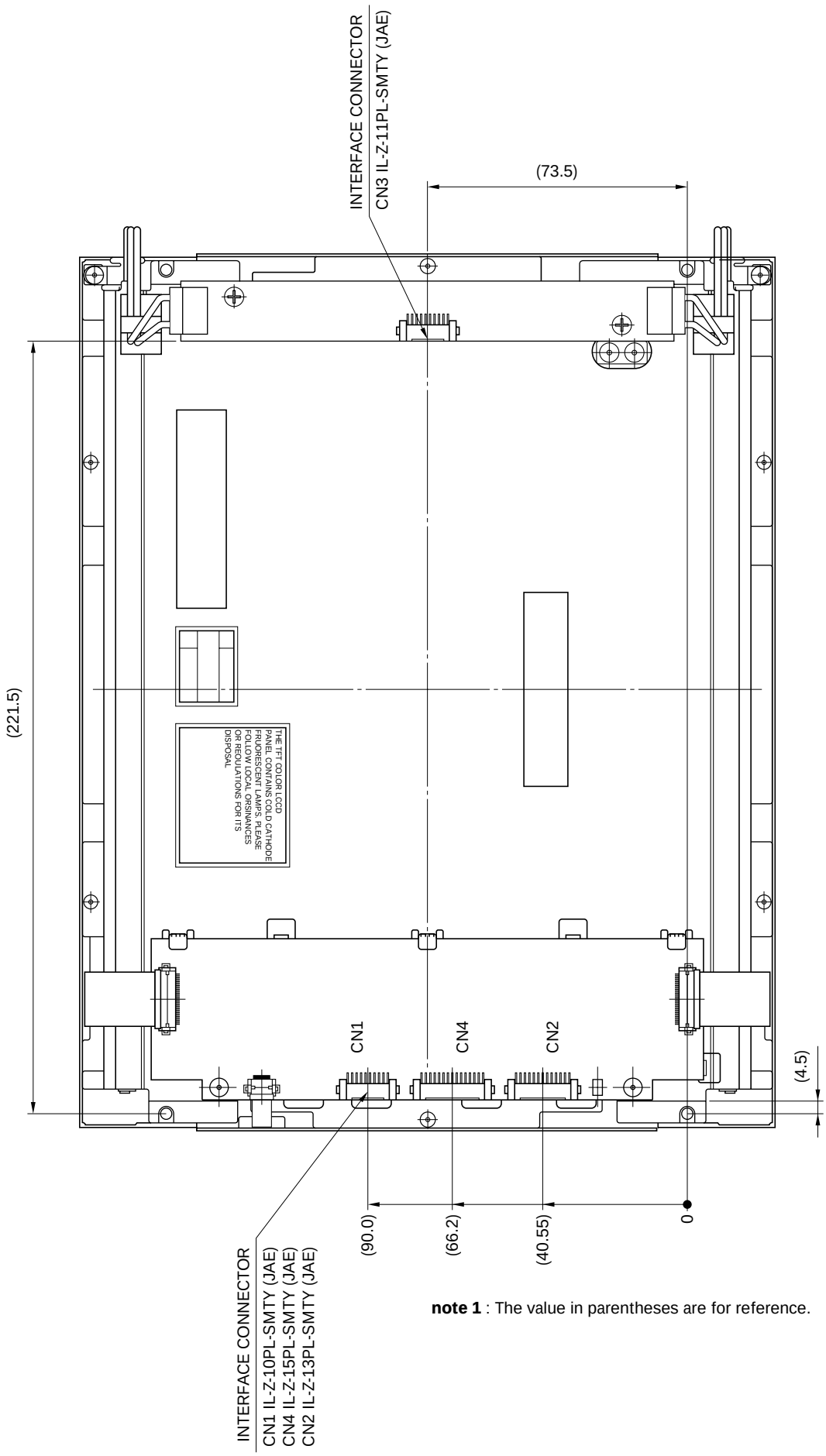
Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING (Unit in mm)



∗ **note 1** : The value in parentheses are for reference.

note 2 : The tarque to mounting screw should never exceed 0.29 NËm (3kgfËcm)



note 1 : The value in parentheses are for reference.