NEC

TFT COLOR LCD MODULE

NL6448AC33-10

26 cm (10.4 type), 640×480 pixels 4096 colors, incorporated one lamp/edge-light type backlight

DESCRIPTION

NL6448AC33-10 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) module comprising amorphous silicon TFT attached to each signal electrode, a driving circuit, and a backlight.

The 26 cm diagonal display area contains 640 × 480 pixels and can display 4096 colors simultaneously.

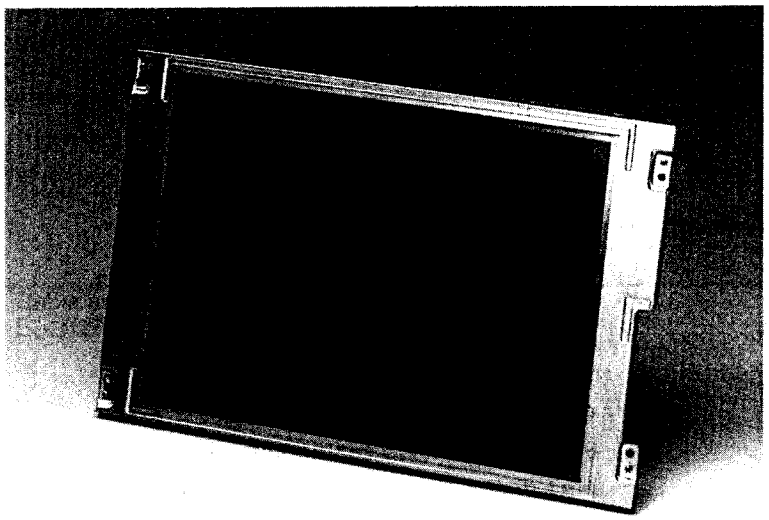
By utilizing one lamp/edge-light type backlight, a very thin profile design and low power consumption have been achieved.

FEATURES

- High contrast ratio, wide color gamut
- High-speed response
- Incorporated edge light type backlight and Inverter
- Data enable function

APPLICATIONS

- Notebook personal computer (PC), word processor
- Display terminals for control system
- New media
- Control board for NC machine
- Monitors for process controller



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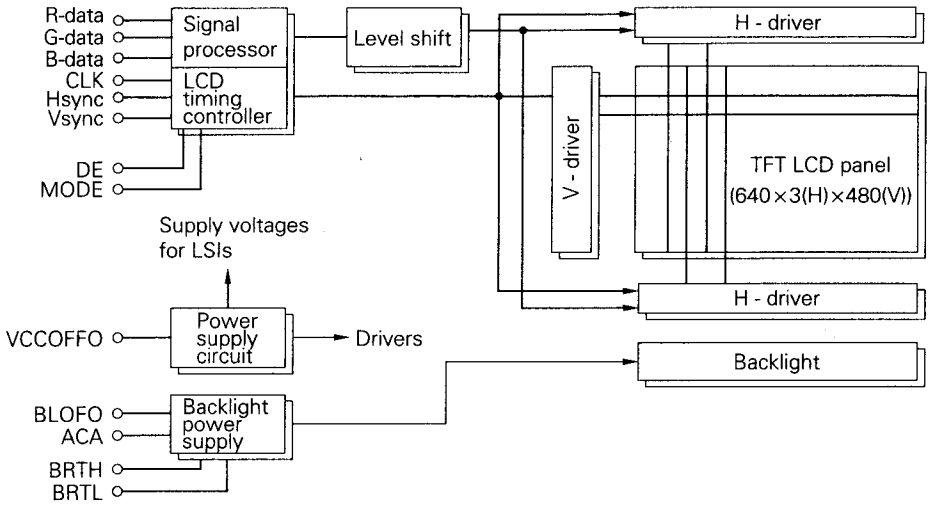
STRUCTURE AND FUNCTIONS

A TFT color LCD module comprises a TFT LCD panel, LSIs for driving liquid crystal, and the backlight. The TFT LCD panel is composed of a TFT array glass substrate superimposed on a color filter glass substrate with liquid crystal filled in the narrow gap between two substrates. The backlight apparatus is located on the backside of the LCD panel.

RGB (Red, Green, Blue) data signals are sent to LCD panel drivers after modulation into suitable forms for active matrix addressing through signal processor.

Each of the liquid crystal cells acts as an electro-optical switch that controls the light transmission from the backlight by a signal applied to a signal electrode through the TFT switch.

BLOCK DIAGRAM



OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	211.2(H) × 158.4(V) mm
Drive system	a-Si TFT active matrix
Display colors	4096 colors
Number of pixels	640 × 480 pixels
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.33(H) × 0.33(V) mm
Module size	270±1(H) × 183±1(V) × 13.0(D) mm
Weight	700 g (typ.)
Contrast ratio	150 : 1 (typ.)
Viewing angle (more than the contrast ratio of 10 : 1)	
	Horizontal : 45° (typ. left side, right side)
	Vertical : 25° (typ. up side), 25° (typ. down side)
Designed viewing direction	12 o'clock (upper direction)
Color gamut	55 % (typ. center, to NTSC)
Response time	40 msec. (max.), "white" to "black"
Luminance	90 cd / m² (typ. AC adapter mode), 55 cd / m² (typ. battery mode)
Signal system	4-bit digital signals for each of RGB primary colors, synchronous signals (Hsync, Vsync), dot clock (CLK)
Supply voltages	5 V (Logic, LCD driving), 5.2 to 20 V (Backlight)
Backlight	A fluorescent lamp with inverter (cold cathode type)
Power consumption	4.8 W (typ. AC adapter mode), 3.7 W (typ. battery mode)

GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	270.0 ±1(H) × 183.0 ± 1(V) × 13.0 max.(D)	mm
Display area	211.2(H) × 158.4(V) (diagonal size 10.4 typ.)	mm
Number of pixels	640(H) × 480(V)	pixel
Dot pitch	0.11(H) × 0.33(V)	mm
Pixel pitch	0.33(H) × 0.33(V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	
Display colors	4 096	color
Weight	720 (max.)	g

An inverter is incorporated within the module. (A luminance control variable resistor is extra)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks	
Supply voltage	V_{DD}	0 to 21.0	V	Ta = 25 °C	
	V_{CC}	−0.3 to 6.5	V		
Input voltage	V_I	−0.3 to V_{CC} +0.3	V		
Storage temp.	T_{ST}	−20 to 60	°C		
Operating temp.	T_{OP}	0 to 50	°C	Module surface*	
Humidity		≦ 95 % relative humidity		Ta = 40 °C	no condensation
		≦ 85 % relative humidity		Ta = 50 °C	
		absolute humidity shall not exceed Ta=50 °C, 85 % relative humidity level		Ta > 50 °C	

* measured at center of display area

ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving

Ta = 25 °C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{cc}	4.75	5.0	5.25	V	
Logic input "L"	V_{IL}	0	–	0.8	V	TTL
Logic input "H"	V_{IH}	2.2	–	V_{cc}	V	TTL
Supply current	I_{cc}	–	*200	350	mA	V_{cc} = 5.0 V

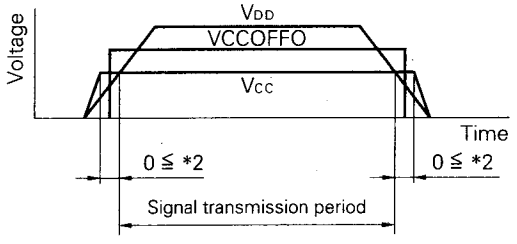
* at dot-checkered pattern

(2) Backlight

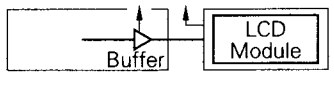
Ta = 25 °C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note	
Supply voltage	V_{DD}	5.2	–	20.0	V	backlight power supply	
Power consumption	P_{DD}	–	3.8	–	W	V_{DD} = 12 V	AC adapter mode (ACA = L)
		–	–	5.9	W	–	
		–	2.7	–	W	V_{DD} = 7.2 V	AC adapter mode (ACA = H)
		–	–	4.2	W	–	

SUPPLY VOLTAGE SEQUENCE



*1 The supply voltage of the external driver for input signals should be the same as Vcc.



*2 Apply V_{DD} within the LCD operation period. When the backlight turns on before LCD operation or the LCD operation turns off before the backlight turns off, the display may momentarily become white.

*3 When a battery is used as V_{DD}, the backlight must be controlled by BLOFFO (backlight ON/OFF signal).

*3 In the case of VCCOFFO = low level, please keep whole data and synchronous signals low level or high impedance.

INTERFACE PIN CONNECTION

(1) Interface signals, power supply

Connector : IL-Z-R10PL-SMTY + IL-Z-R13PL-SMTY + IL-Z-R11PL-SMTY (JAE)

(CN1:No.1 to 10) (CN2:No.11 to 23) (CN3:No.24 to 34)

Pin No.	Symbol	Function
1	CLK	Dot clock
2	GND	Signal ground
3	GND	Signal ground
4	Hsync	Horizontal sync.
5	Vsync	Vertical sync.
6	GND	Signal ground
7	R_0	Red data (LSB)
8	R_1	Red data
9	R_2	Red data
10	R_3	Red data (MSB)
11	GND	Signal ground
12	G_0	Green data (LSB)
13	G_1	Green data
14	G_2	Green data
15	G_3	Green data (MSB)
16	GND	Signal ground
17	B_0	Blue data (LSB)

Pin No.	Symbol	Function
18	B_1	Blue data
19	B_2	Blue data
20	B_3	Blue data (MSB)
21	GND	Signal ground
22	ACA	Brightness mode select
23	BLOFFO	Backlight ON/OFF signal
24	GND	Signal ground
25	V_{CC}	Logic power supply
26	V_{DD}	Backlight power supply
27	V_{DD}	Backlight power supply
28	N.C.	
29	GNDB	Backlight ground
30	GNDB	Backlight ground
31	DE	Data enable
32	MODE	Timing mode select
33	VCCOFFO	V_{CC} ON/OFF signal
34	GND	Signal ground

(2) External variable resistor

1) Connector for luminance control (on the left side) : IL-Z-R2PL-SMTY (JAE)

(CN4 : No.1 to 2)

Pin No.	Symbol	Function
1	BRTH	luminance control input

Pin No.	Symbol	Function
2	BRTL	luminance control input

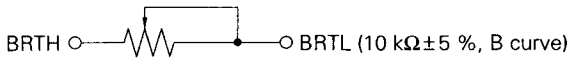
2) Connector for luminance control (on the right back) : LZ-5P-SL-SMT (JAE)

(CN5 : No.1 to 5)

Pin No.	Symbol	Function
1	BRTH	luminance control input
3	BRTL	luminance control input
5	N.C.	

Pin No.	Symbol	Function
2	BRTH	luminance control input
4	BRTL	luminance control input

Note 1 : The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor should correspond to the minimum of luminance.

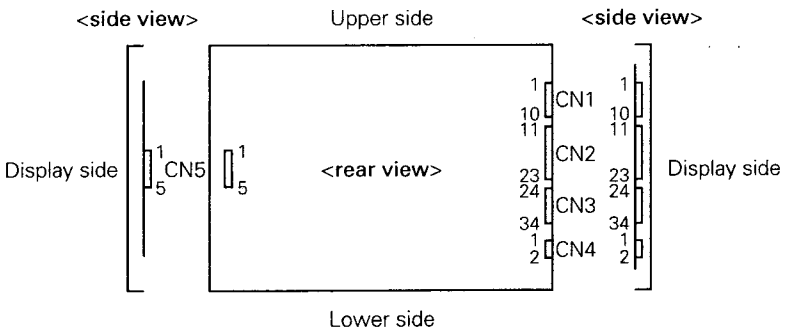


<a way of connecting variable resistor to pins>

Note 2 : The pins for BRTH and BRTL of luminance control connector on the left side (CN4) and the right side (CN5) are connected each other in the module.
Then, any one pair of the pins are available for luminance control variable resistor.

CAUTION

Connect the variable resistor of fixed resistor (10 kΩ or less) to the pin of BRTH and BRTL.
If the resistor (10 kΩ or less) is not connected, the life of fluorescent lamp would be short.



(3) PIN DESCRIPTION

Symbol	Function	Description
R0 – R3 G0 – G3 B0 – B3	Display data	4-bit digital signals for each of RGB primary colors.
Hsync	Horizontal sync.	Horizontal synchronous signal.
Vsync	Vertical sync.	Vertical synchronous signal.
CLK	Dot clock	Timing signal for display data. Module strobes the display data at the falling edge of CLK.
DE	Data enable	The signal that defines the graphic data that is to be displayed on the screen. When MODE = L, the function of this pin is ignored. (Keep DE high or low) When MODE = H, the period of DE = H is the display period of the module.
MODE	Timing mode select	MODE = H : DE mode (data enable function is active) MODE = L : fixed timing mode (data enable function is ignored)
VCCOFFO	V_{CC} ON / OFF signal	VCCOFFO = H : Power on inside of the module. VCCOFFO = L : Power off inside of the module.
ACA	Brightness mode select	ACA = H : battery mode (low luminance) ACA = L : AC ada[ter mode (high luminance)
BLOFFO	Backlight ON/OFF signal	BLOFFO = H : backlight on BLOFFO = L : backlight off
BRTH BRTL	Backlight brightness control	Connect a variable resistor (10 kΩ ± 5 %, B curve) between BRTH and BRTL.
V_{CC} V_{DD}	+5.0 V (± 5 %) +5.2 V to + 20.0 V	Power supply for logic and LCD driving. Power supply for backlight
GND GNDB	Logic ground *) Backlight ground	Ground for V_{CC} Ground for backlight *) GND is separated from GNDB in the module.

DISPLAY COLORS vs. INPUT DATA SIGNALS

	Display	Data signal (0 : Low level, 1 : High level)											
		R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	1	1	1	1
	Red	1	1	1	1	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	0	0	0	0	1	1	1	1
	Green	0	0	0	0	1	1	1	1	0	0	0	0
	Cyan	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	1	0	0	0	0	0	0	0	0
	Dark	0	0	1	0	0	0	0	0	0	0	0	0
	↑ ↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Bright	1	1	0	1	0	0	0	0	0	0	0	0
		1	1	1	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0
	↑ ↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Bright	0	0	0	0	1	1	0	1	0	0	0	0
		0	0	0	0	1	1	1	0	0	0	0	0
	Green	0	0	0	0	1	1	1	1	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1
	Dark	0	0	0	0	0	0	0	0	0	0	1	0
	↑ ↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Bright	0	0	0	0	0	0	0	0	1	1	0	1
		0	0	0	0	0	0	0	0	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	1	1	1	1

Note : Colors are developed in combination with 4 bit signal (16 steps in grayscale) of each primary red, green, and blue color.
This process can result in up to 4096 (16 × 16 × 16) colors.

FIXED TIMING MODE SPECIFICATIONS

(1) Input signal specifications (fixed timing mode)

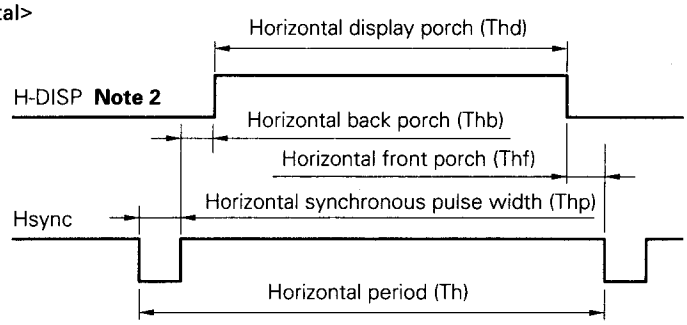
MODE (Pin No.32) = Low

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	1 / Tc	21.0	25.175	29.0	MHz	39.722 ns (Typ.)
	Tch / Tc	0.4	0.5	0.6	—	
	Tcrf			10	ns	
Hsync	Th	30.0	31.778	33.6	μs	31.468 kHz (typ.)
			800		CLK	
	Thd		25.422 640		μs CLK	
	Thf		0.636 16		μs CLK	
	Thp	10	3.813 96		μs CLK	Thp + Thb = 144 CLK
	Thb		1.907 48	134	μs CLK	
	Thch	12			ns	
	Thcs	8			ns	
	Tvh	15			ns	
	Tvs	15			ns	
	Thrf			10	ns	
Vsync	Tv	16.1	16.683	17.2	ms	59.94 Hz (typ.)
			525		H	
	Tvd		15.253 480		ms H	
	Tvf		0.381 12		ms H	
	Tvp	1	0.063 2		ms H	Tvp + Tvb = 33 H
	Tvb		0.985 31	32	ms H	
	Tvrf			10	ns	
DATA R0–R3 G0–G3 B0–B3	Tds	8			ns	
	Tdh	12			ns	
	Tdrf			10	ns	

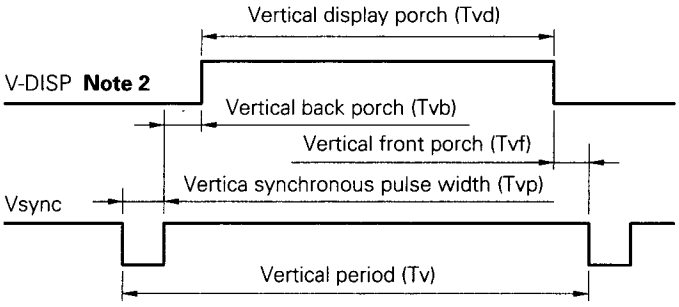
All of parameters should be kept in the specified range.

(2) Definition of input signal timing (fixed timing mode) Note 1

<Horizontal>

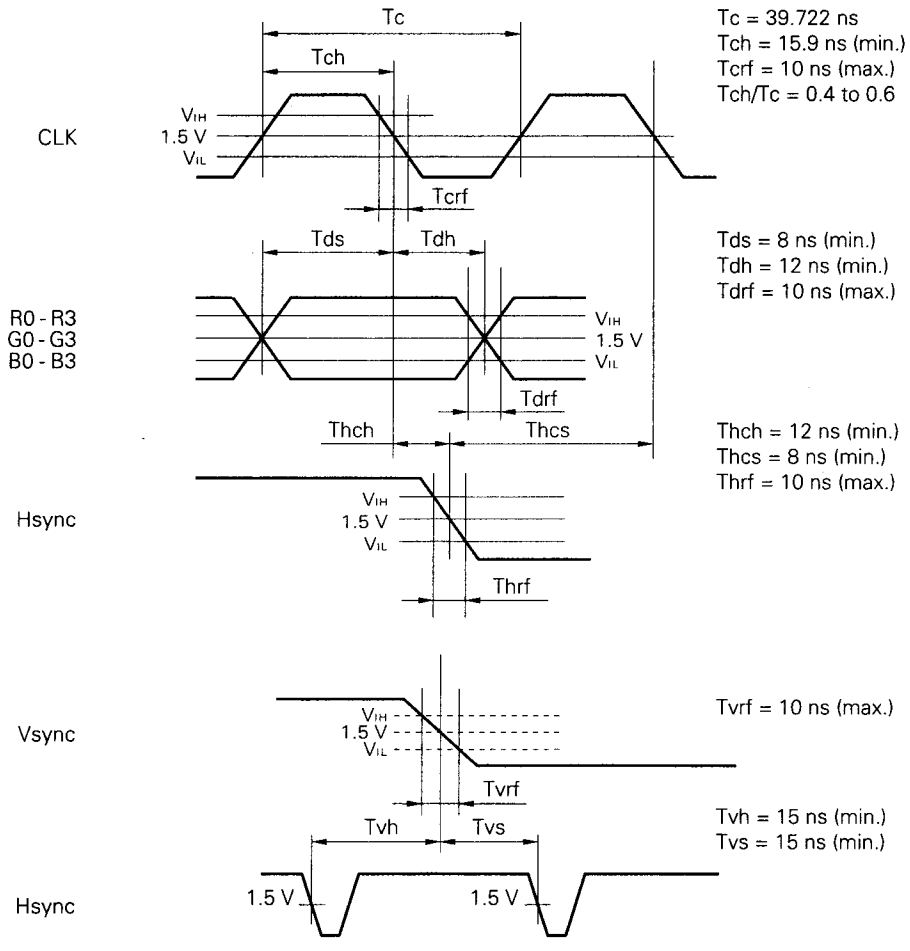


<Vertical>

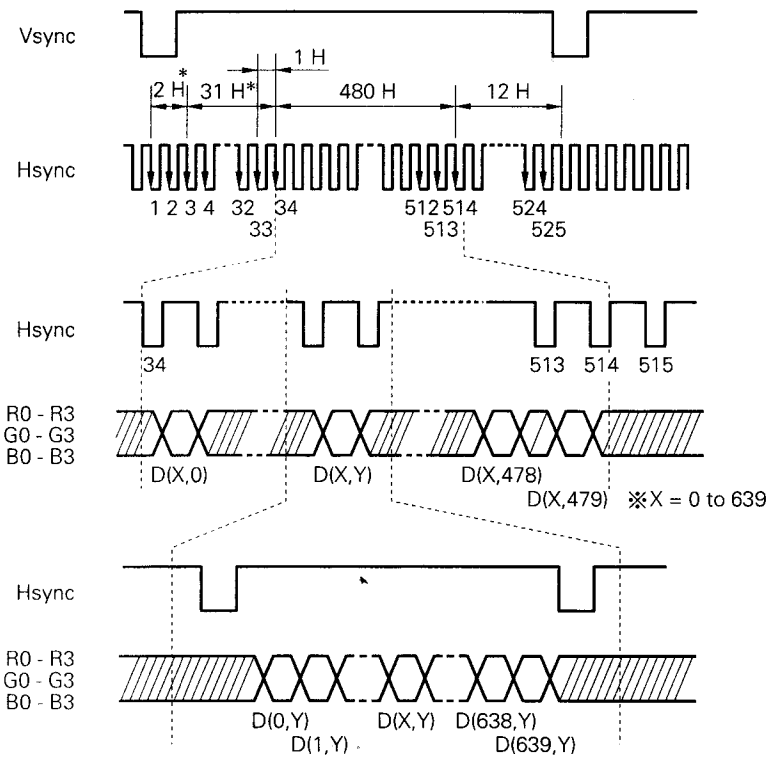


Note 1 : Regarding how ro conut H/CLK, refer to the input signal timing chart (fixed timing mode). Thp + Thb and Tvp + Tvb are fixed. The display position will be wrong, when different values are selected.

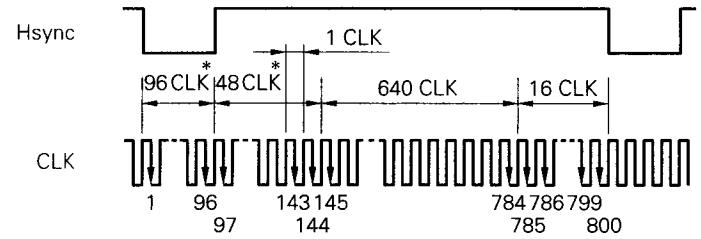
Note 2 : These do not exist as signals.



(3) Input signal timing chart (fixed timing mode)



*) Tvp (min.) is 1H.
*) Tvp + Tvb = 33H (Fixed).



*) Thp (min.) is 10 CLK.
*) Thp + Thb = 144 CLK (Fixed).

Display position of input data

D (0, 0)	D (1, 0)	---	D (X, 0)	---	D (638, 0)	D (639, 0)
D (0, 1)	D (1, 1)	---	D (X, 1)	---	D (638, 1)	D (639, 1)
-+-	-+-	-+-		-+-		
D (0, Y)	D (1, Y)	---	D (X, Y)	---	D (638, Y)	D (639, Y)
		-+-		-+-		
D (0, 478)	D (1, 478)	---	D (X, 478)	---	D (638, 478)	D (639, 478)
D (0, 479)	D (1, 479)	---	D (X, 479)	---	D (638, 479)	D (639, 479)

DE MODE SPEDIFICATIONS

(1) Input signal specifications (DE mode)

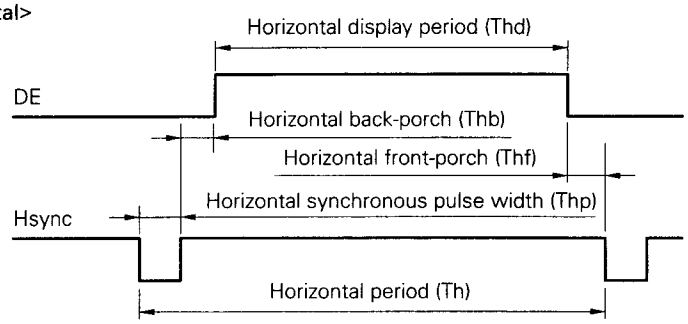
MODE (Pin No.32) = High

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	1 / Tc	21.0	25.175	29.0	MHz	39.722 ns (typ.)
	Tch / Tc	0.4	0.5	0.6	—	
	Tcrf			10	ns	
Hsync	Th	30.0	31.778	33.6	μs	31.468 kHz (typ.)
			800		CLK	
	Thd		25.422		μs	
			640		CLK	
	Thf	0	0.636		μs	
		0	16		CLK	
	Thp		3.813		μs	
		10	96		CLK	
	Thb		1.907		μs	
		4	48		CLK	
	Thch	12			ns	
	Thcs	8			ns	
	Tvh	15			ns	
	Tvs	15			ns	
	Thrf			10	ns	
Vsync	Tv	16.1	16.683	17.2	ms	59.94 Hz (typ.)
			525		H	
	Tvd		15.253		ms	
			480		H	
	Tvf	0	0.381		ms	
		0	12		H	
	Tvp		0.063		ms	
		1	2		H	
	Tvb		0.985		ms	
		4	31		H	
	Tvrf			10	ns	
DATA R0–R3 G0–G3 B0–B3	Tds	8			ns	
	Tdh	12			ns	
	Tdrf			10	ns	
DE	Tes	8			ns	
	Teh	12			ns	
	Terf			10	ns	

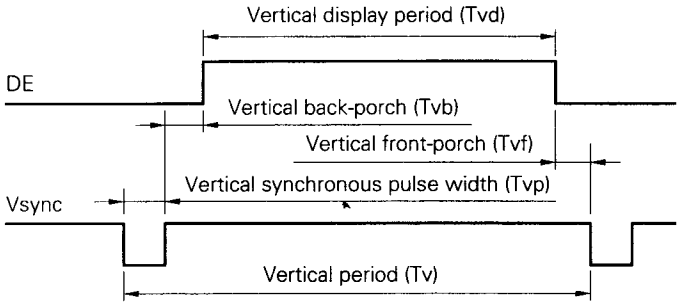
All of parameters should be kept in the specified range.

(2) Definition of input signal timing (DE mode) Note

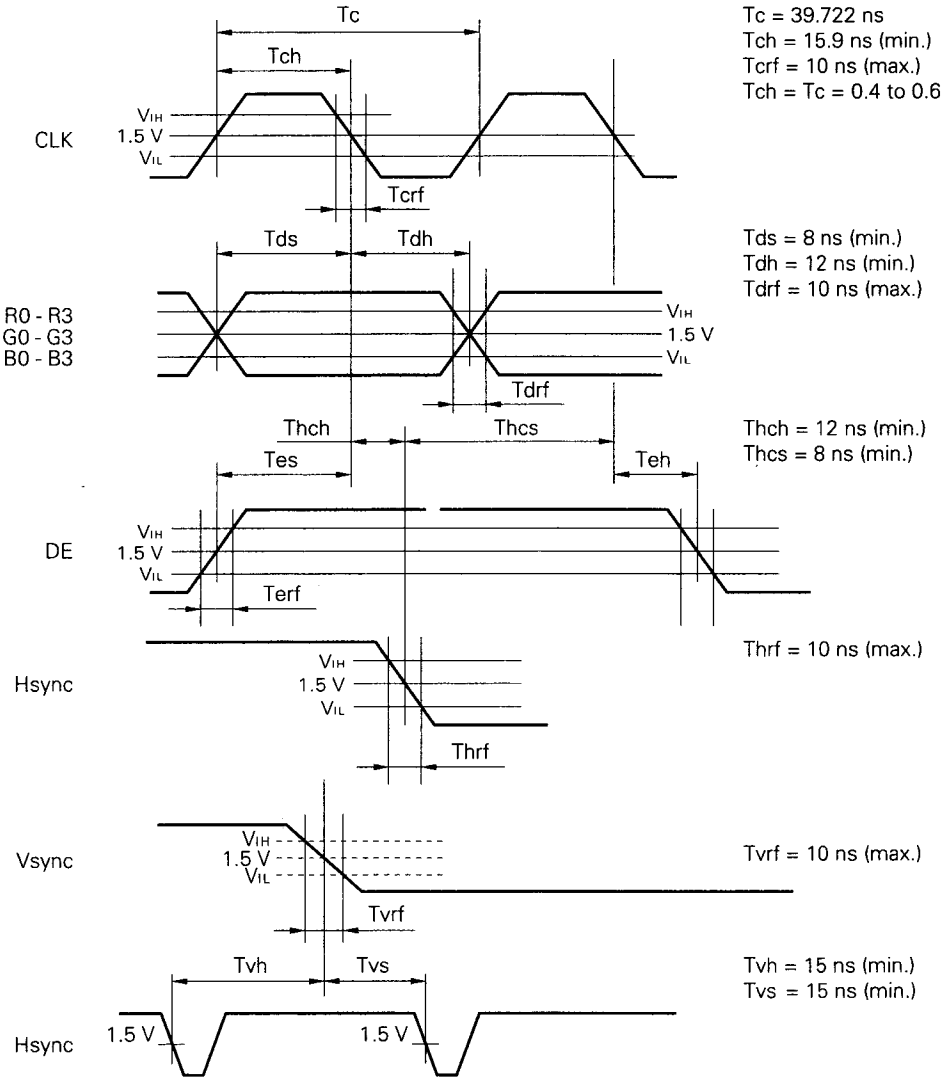
<Horizontal>



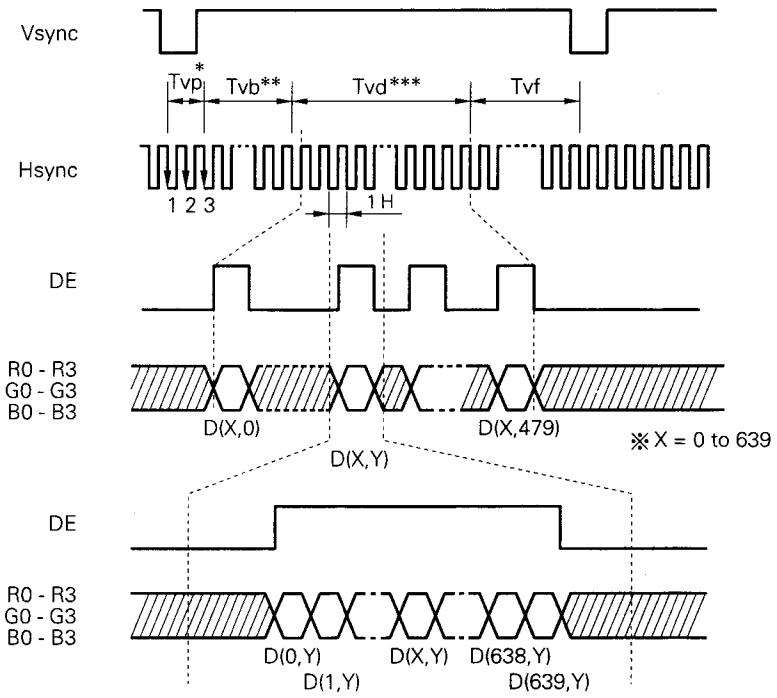
<Vertical>



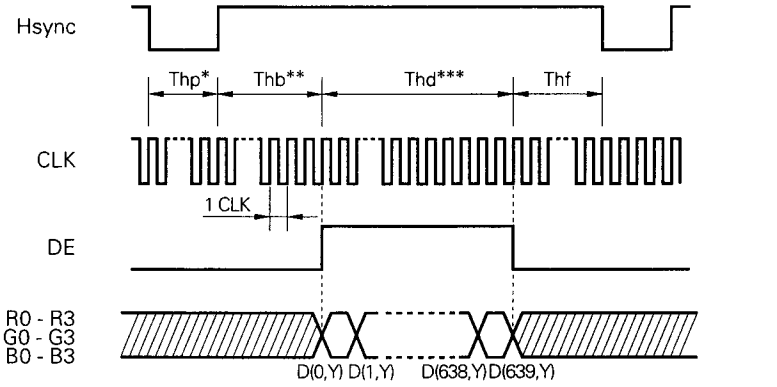
Note 1 : Regarding how ro count H/CLK, refer to the input signal timing chart (DE mode).



(3) Input signal timing chart (DE mode)



*) Tvp (min.) is 1H.
**) Tvb (min.) is 4H.
***) Tvd (Typ.) is 480H.



*) Thp (min.) is 10 CLK.
**) Thb (min.) is 4 CLK.
***) Thd (typ.) is 640 CLK.

Display position of input data

D (0, 0)	D (1, 0)	- - -	D (X, 0)	- - -	D (638, 0)	D (639, 0)
D (0, 1)	D (1, 1)	- - -	D (X, 1)	- - -	D (638, 1)	D (639, 1)
- + -	- + -	- + -		- + -		
D (0, Y)	D (1, Y)	- - -	D (X, Y)	- - -	D (638, Y)	D (639, Y)
		- + -		- + -		
D (0, 478)	D (1, 478)	- - -	D (X, 478)	- - -	D (638, 478)	D (639, 478)
D (0, 479)	D (1, 479)	- - -	D (X, 479)	- - -	D (638, 479)	D (639, 479)

GENERAL CAUTION

WARNING

Do not touch an inverter circuit -- a warning label is stuck on -- while the LCD module is operating, because of dangerous high voltage.

(1) Caution for taking out the module
   1) Pick the pouch only, when taking out module from a carrier box.

(2) Cautions for handling the module
   1) As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges. Peel protection sheet out from the LCD panel surface as slowly as possible.
   2) As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
   3) As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
   4) Do not pull the interface connectors in or out while the LCD module is operating.
   5) Put the module display side down on a flat horizontal plane.
   6) Handle connectors and cables with care.

(3) Cautions for the operation
   1) When the module is operating, do not lose DOTCLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.
   2) Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.
   3) Connect the variable resistor or fixed resistor (10 kΩ or less) to the pin of BRTH and BRTL. If the resistor is not connected, the life of fluorescent lamp would be short.

(4) Cautions for the atmosphere
   1) Dew drop atmosphere should be avoided.
   2) Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Caution for the module characteristics
   1) Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
   1) Do not disassemble and/or reassemble LCD module.
   2) Do not readjust variable resistor or switch etc.
   3) When returning the module for repair or etc., please pack the module not to be broken. We recommend to use our shipping package.

Liquid Crystal Display has the following specific characteristics. These are not defects or malfunctions.
The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tubes for backlighting. Optical characteristics, like luminance or uniformity, will change during time.
Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING (Unit in mm)