NEC NEC LCD Technologies, Ltd.

TFT COLOR LCD MODULE

NL3224BC35-20

13.9cm (5.5 Type)
QVGA

DATA SHEET
DOD-PD-0300 (8th edition)

This DATA SHEET is updated document from DATA SHEET DOD-PD-0076(7).

All information is subject to change without notice. Please confirm the sales representative before starting to design your system.

INTRODUCTION

No part of this document shall be copied in any form or by any means without the prior written consent of NEC LCD Technologies, Ltd. (hereinafter called "NEC").

NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a product described herein or any other liability arising from use of such application. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or of others.

While NEC has been making continuous effort to enhance the reliability of its products, the possibility of failures cannot be eliminated entirely. To minimize risks of damage to property or injury to person arising from a failure in an NEC product, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.

NEC products are classified into the following three quality grades:
  "Standard", "Special", "Specific"

The *"Specific"* quality grade applies only to applications developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a product depend on its quality grade, as indicated below. Customers must check the quality grade of each application before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is *"Standard"* unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for *"Standard"* quality grade, they should contact NEC sales representative in advance.

CONTENTS

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Color LCD module NL3224BC35-20 is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing circuit, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATION   ☆
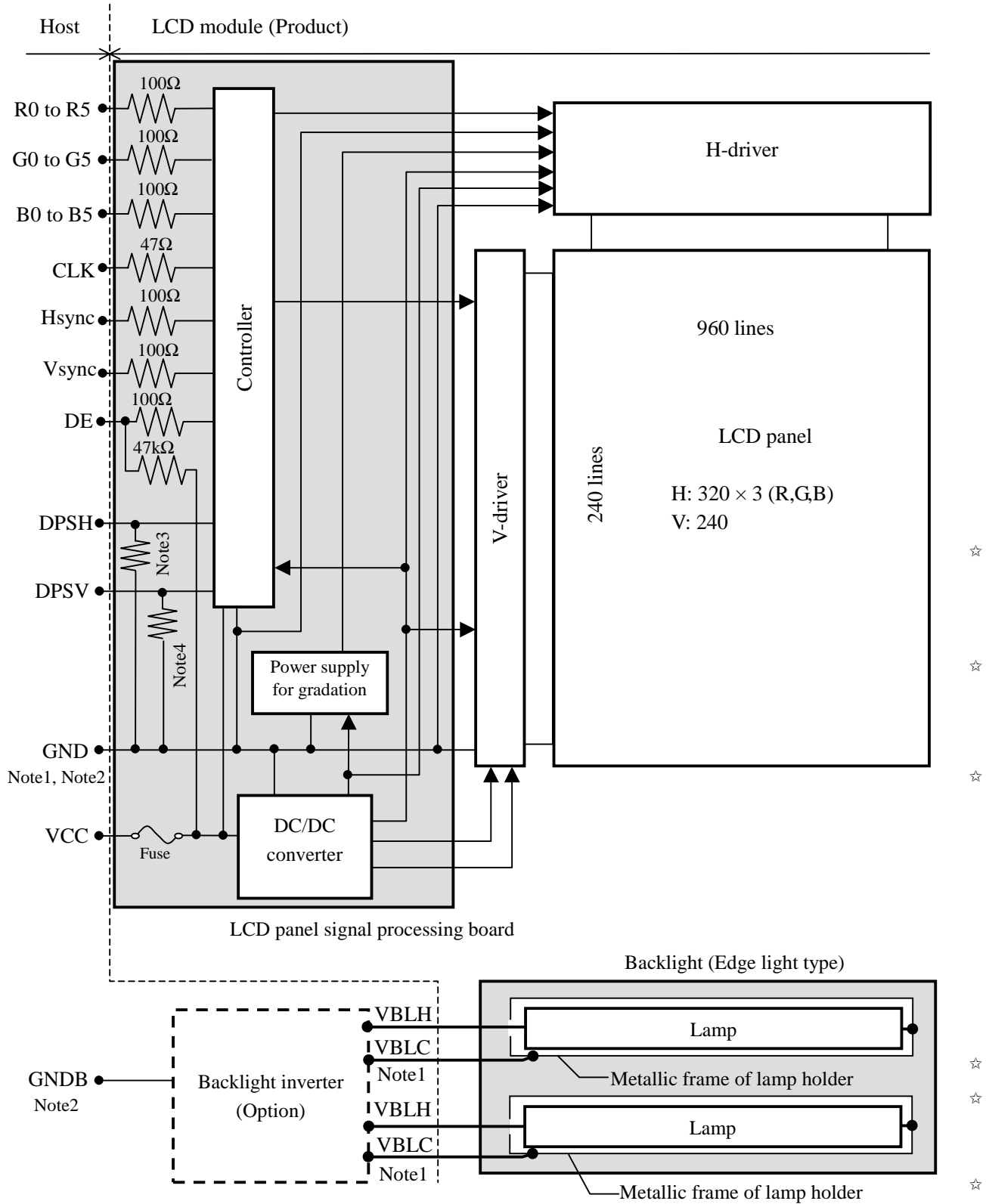
- For industrial use

1.3 FEATURES

- High luminance
- Wide color gamut
- Wide viewing angle
- Low reflection
- 6-bit digital RGB signals
- Reversible-scan direction
- Edge light type (without inverter)
- Replaceable lamp for backlightt
- Acquisition product for UL1950 3rd edition/CSA C22.2 No.950-95 (File number: E170632)

2. GENERAL SPECIFICATIONS

Display area	111.4 (H) × 83.5 (V) mm
Diagonal size of display	13.9 cm (5.5 inches)
Drive system	a-Si TFT active matrix
Display color	262,144 colors
Pixel	320 (H) × 240 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.1160 (H) × 0.3480 (V) mm
Pixel pitch	0.3480 (H) × 0.3480 (V) mm
Module size	134.0 (W) × 104.5 (H) × 12.5 (D) mm (typ.)
Weight	210 g (typ.)
Contrast ratio	400:1 (typ.)
Viewing angle	*At the contrast ratio ≥10:1* ☆ • Horizontal: Right side 65° (typ.), Left side 65° (typ.) • Vertical: Up side 40° (typ.), Down side 65° (typ.)
Designed viewing direction	*At DPSH, DPSV= Open: Normal scan* ☆ • Viewing direction without image reversal: down side (6 o'clock) • Viewing direction with contrast peak: down side 0° to 5° (6 o'clock) • Viewing angle with optimum grayscale (γ=2.2): normal axis
Polarizer surface	Antiglare treatment
Polarizer pencil-hardness	3H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 50 % (typ.) [against NTSC color space]
Response time	*Ton (white 90% → black 10%)* 5 ms (typ.)
Luminance	*At IBL= 5.0mArms / lamp* 400 cd/m^2 (typ.)
Signal system	6-bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE), Horizontal synchronous signal (Hsync), Vertical synchronous signal (Vsync)
Power supply voltage	LCD panel signal processing board: 3.3V or 5.0V
Backlight	Edge light type: 2 cold cathode fluorescent lamps ⎡ Replaceable parts ⎣ • Lamp holder set: Type No. 55LHS11 ⎤⎦ ⎡ Recommended inverter (Option) ⎣ • Inverter: Type No. 55PW131 ⎤⎦
Power consumption	*At IBL= 5.0mArms / lamp and checkered flag pattern* ☆ 4.1 W (typ., Power dissipation of the inverter does not include.)

3. BLOCK DIAGRAM

Host | LCD module (Product)

R0 to R5 — 100Ω
G0 to G5 — 100Ω
B0 to B5 — 100Ω
CLK — 47Ω
Hsync — 100Ω
Vsync — 100Ω
DE — 100Ω
— 47kΩ
DPSH
DPSV — Note3, Note4
GND — Note1, Note2
VCC — Fuse

Controller

Power supply for gradation

DC/DC converter

LCD panel signal processing board

H-driver

V-driver

240 lines / 960 lines

LCD panel

H: 320 × 3 (R,G,B)
V: 240

Backlight (Edge light type)

VBLH
VBLC — Note1
Lamp
Metallic frame of lamp holder

VBLH
VBLC — Note1
Lamp
Metallic frame of lamp holder

GNDB — Note2
Backlight inverter (Option)

Note1: Connections between GND (Signal ground), shield plate and VBLC (Lamp low voltage terminal) in ☆
the LCD module

Front shield plate - Rear shield plate	Not connected
GND - Front shield plate and Rear shield plate	Not connected
VBLC - Front shield plate and Rear shield plate	Not connected
GND - VBLC	Not connected

Front shield plate

Rear shield plate
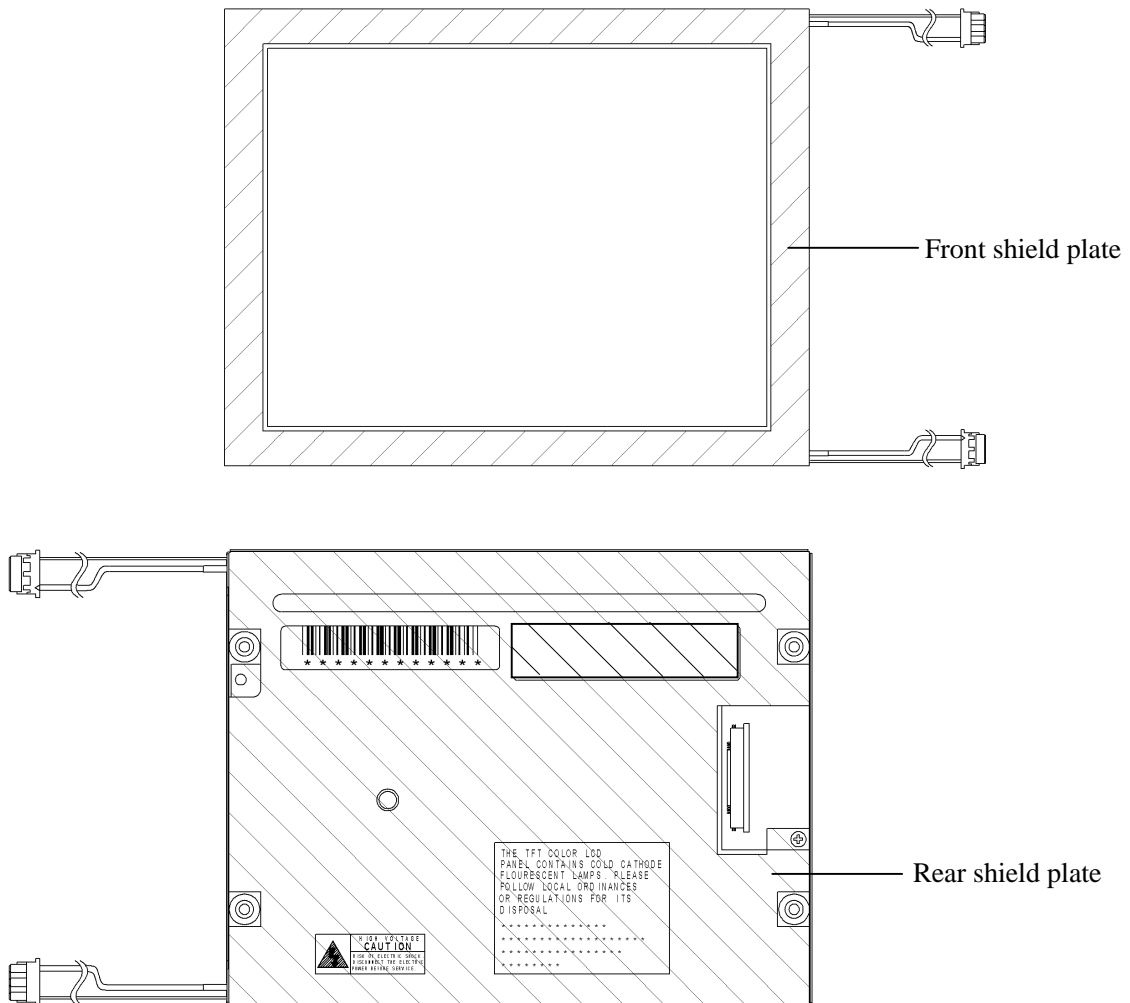
Note2: GND and GNDB must be connected to customer equipment's ground, and it is recommended that ☆
these grounds are connected together in customer equipment.

Note3: Pull-down resistance of DPSH pin ☆

Power supply voltage VCC	Pull-down resistance of DPSH pin (kΩ)		
	min.	typ.	max.
at 3.3V	8.2	13.0	18.3
at 5.0V	6.0	10.0	15.0

Note4: Pull-down resistance of DPSV pin ☆

Power supply voltage VCC	Pull-down resistance of DPSV pin (kΩ)		
	min.	typ.	max.
at 3.3V	13.0	18.3	23.0
at 5.0V	10.0	15.0	20.0

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	134.0 ± 0.5 (W) $\times$ 104.5 ± 0.5 (H) $\times$ 12.5 ± 0.5 (D)	Note1	mm
Display area	111.4 (H) $\times$ 83.5 (V)	Note1	mm
Weight	210 (typ.), 220 (max.)		g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VCC	-0.3 to +6.5	V	Ta = 25°C
	Lamp voltage	VBLH	1,500	Vrms	
Input voltage for signals	Display signals Note1	VD	-0.3 to VCC+0.3	V	
	Function signal Note2	VF	-0.3 to VCC+0.3	V	
Storage temperature		Tst	-30 to +80	°C	-
Operating temperature	Front surface	TopF	-10 to +70	°C	
	Rear surface	TopR	-10 to +75	°C	
Relative humidity Note3		RH	≤ 95	%	Ta ≤ 40°C
			≤ 85	%	$40 < $ Ta ≤ 50°C
			≤ 70	%	$50 < $ Ta ≤ 55°C
			≤ 60	%	$55 < $ Ta ≤ 60°C
			≤ 50	%	$60 < $ Ta ≤ 65°C
			≤ 42	%	$65 < $ Ta ≤ 70°C
Absolute humidity Note3		AH	≤ 83 Note4	g/m^3	Ta > 70°C

Note1: Display signals are CLK, Hsync, Vsync, DE and DATA (R0 to R5, G0 to G5, B0 to B5).
Note2: Function signals are DPSH and DPSV.
Note3: No condensation
Note4: Ta = 70°C, RH = 42%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

| Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
Power supply voltage		VCC	3.0	3.3	3.6	V	at VCC = 3.3V	☆
			4.75	5.0	5.25	V	at VCC = 5.0V	
Power supply current		ICC	-	180 Note1	250	mA	at VCC = 3.3V	
			-	120 Note1	165	mA	at VCC = 5.0V	
Logic input voltage for display signals	Low	VDLL	0	-	0.3VCC	V		
	High	VDLH	0.7VCC	-	VCC	V	-	
Input voltage for DPSH, DPSV and RSVD signals	Low	VFDL	0	-	0.9	V		☆
	High	VFDH	0.7VCC	-	VCC	V		

Note1: Checkered flag pattern [by EIAJ ED-2522]

4.3.2 Working for backlight lamp

Parameter	Symbol	Ta	min.	typ.	max.	Unit	Remarks
Lamp starting voltage	VS	-10°C	780	-	-	Vrms	Note1
		25°C	550	-	-	Vrms	
Lamp voltage	VBLH	25°C	-	350	-	Vrms	Note1, Note2
Lamp current	IBL	25°C	4.5	5.0	5.5	mArms	Note2
Lamp oscillation frequency	FO	25°C	39	43	47	kHz	Note3

Note1: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note2: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).

$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\ \%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\ \%$$
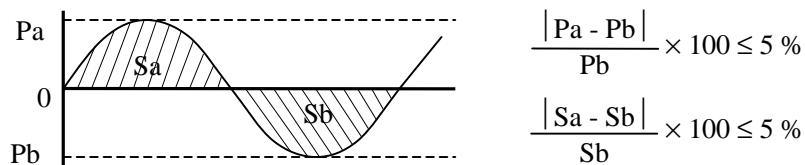
Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note3: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle (See "**4.9.3 Timing characteristics**".)
n: Natural number (1, 2, 3 ········)

Note4: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VCC	3.3 V	≤ 100	mVp-p
	5.0 V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VCC	ICP-S1.8	ROHM Co., Ltd.	1.8A	4.0A	Note1
			50V		

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board
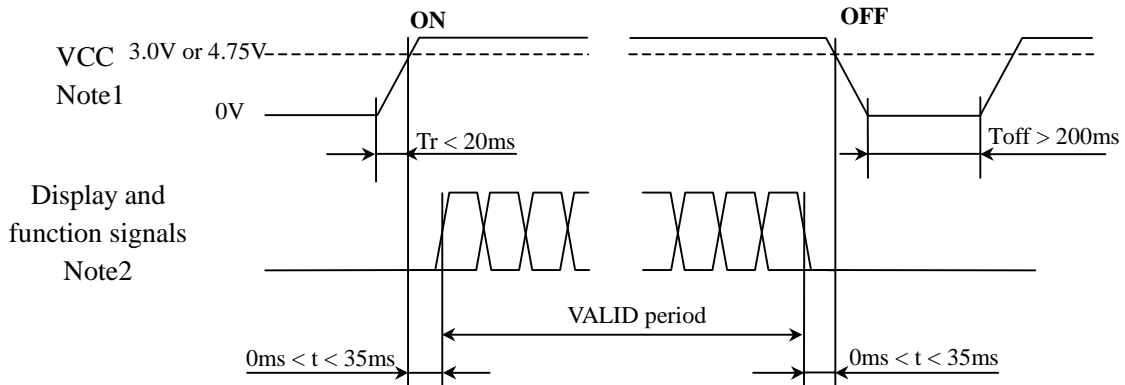
Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 3.0V in "VCC = 3.3V" or 4.75V in "VCC = 5.0V", a protection circuit may work, and then this product may not work.

Note2: Display signals (CLK, Hsync, Vsync, DE, R0 to R5, G0 to G5, B0 to B5) and function signal (DPSH, DPSV) must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VCC.

4.4.2 Sequence for backlight inverter (Option)
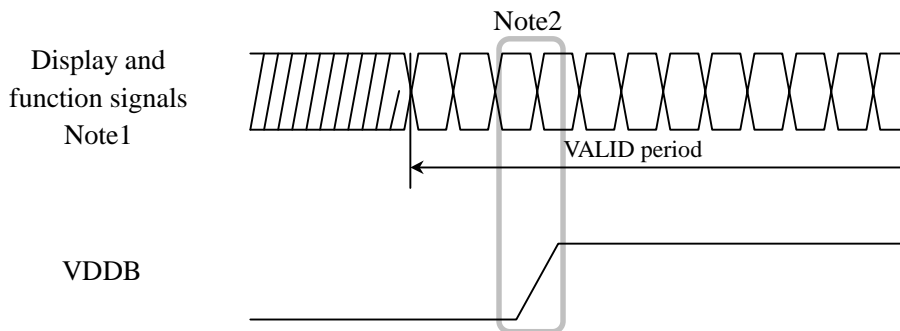
Note1: These are the display and function signals for LCD panel signal processing board.

Note2: The backlight inverter voltage (VDDB) should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

CN1 socket (LCD module side)　　: 08-6210-033-340-800 (Kyocera Elco Corp.)

Pin No.	Symbol	Signal	Remarks		
1	GND	Ground	-		
2	CLK	Dot clock			
3	Hsync	Horizontal synchronous signal			
4	Vsync	Vertical synchronous signal			
5	GND	Ground			
6	R0	Red data (LSB)	Least significant bit		
7	R1	Red data	-		
8	R2	Red data			
9	R3	Red data			
10	R4	Red data			
11	R5	Red data (MSB)	Most significant bit		
12	GND	Ground	-		
13	G0	Green data (LSB)	Least significant bit		
14	G1	Green data	-		
15	G2	Green data			
16	G3	Green data			
17	G4	Green data			
18	G5	Green data (MSB)	Most significant bit		
19	GND	Ground	-		
20	B0	Blue data (LSB)	Least significant bit		
21	B1	Blue data	-		
22	B2	Blue data			
23	B3	Blue data			
24	B4	Blue data			
25	B5	Blue data (MSB)	Most significant bit		
26	GND	Ground	-		
27	DE	Selection of DE / Fixed mode	Data enable signal: High or Open:	DE mode Fixed mode	
28	VCC	Power supply	-		
29	VCC	Power supply			
30	DPSH	Selection of scan direction (Horizontal)	Low or Open: High:	Normal scan Reverse scan	Note1
31	DPSV	Selection of scan direction (Vertical)			
32	RSVD	-	Keep this terminal Low or Open.		
33	GND	Ground	-		

Note1: See "**4.8 SCANNING DIRECTIONS**".

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. If customer connects wrongly, customer will be hurt and the module will be broken.

CN2 plug   : BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)

Adaptable socket   : SM03 (4.0) B-BHS-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Pink cable
2	N.C.	-	Keep this pin open.
3	VBLC	Low voltage (Cold)	White cable

CN3 plug   : BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)

Adaptable socket   : SM03 (4.0) B-BHS-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Pink cable
2	N.C.	-	Keep this pin open.
3	VBLC	Low voltage (Cold)	White cable

4.5.3 Positions of plugs and a socket
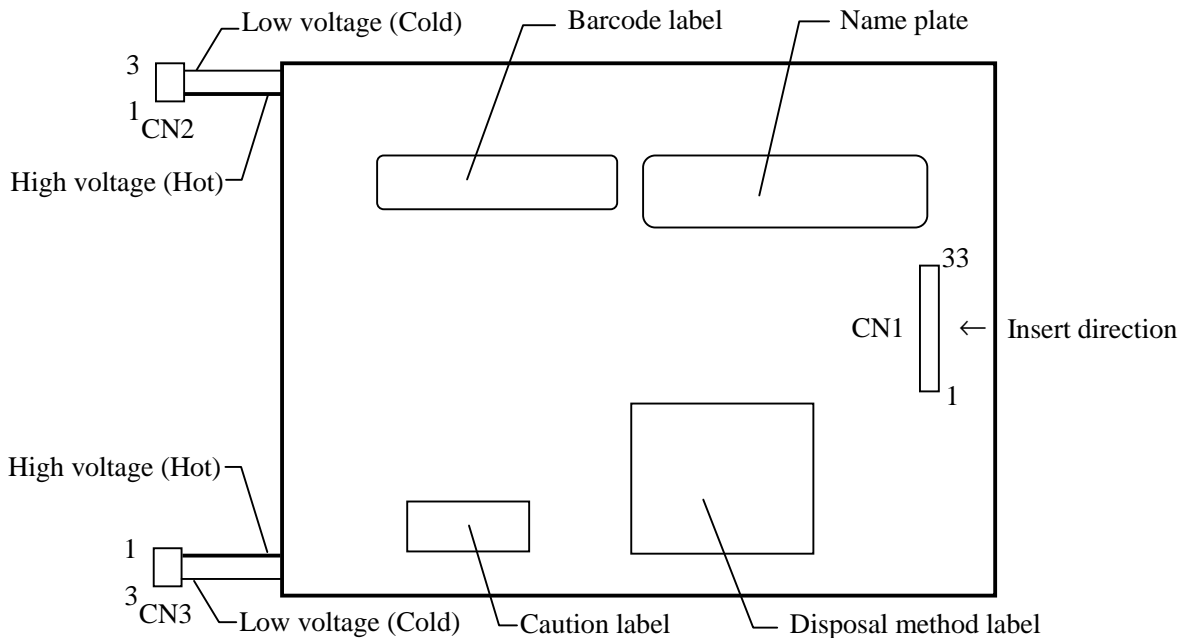
4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 262,144 colors in 64 gray scales. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																	
		R 5	R 4	R 3	R 2	R 1	R 0	G 5	G 4	G 3	G 2	G 1	G 0	B 5	B 4	B 3	B 2	B 1	B 0
Basic color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑			:						:						:			
	↓			:						:						:			
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑			:						:						:			
	↓			:						:						:			
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑			:						:						:			
	↓			:						:						:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

4.7 DISPLAY POSITIONS

The following table is the coordinates per pixel (See "**4.8 SCANNING DIRECTIONS**".).

C (0, 0)

R	G	B

C(0, 0)	C(1, 0)	• • •	C(X, 0)	• • •	C(318, 0)	C(319, 0)
C(0, 1)	C(1, 1)	• • •	C(X, 1)	• • •	C(318, 1)	C(319, 1)
• • •	• • •	• • • •	• • •	• • • •	• • •	• • • •
C(0, Y)	C(1, Y)	• • •	C(X, Y)	• • •	C(318, Y)	C(319, Y)
• • •	• • •	• • • •	• • •	• • • •	• • •	• • •
C(0, 238)	C(1, 238)	• • •	C(X, 238)	• • •	C(318, 238)	C(319, 238)
C(0, 239)	C(1, 239)	• • •	C(X, 239)	• • •	C(318, 239)	C(319, 239)

4.8 SCANNING DIRECTIONS

The following figures are seen from a front view. Also the arrow shows the direction of scan.
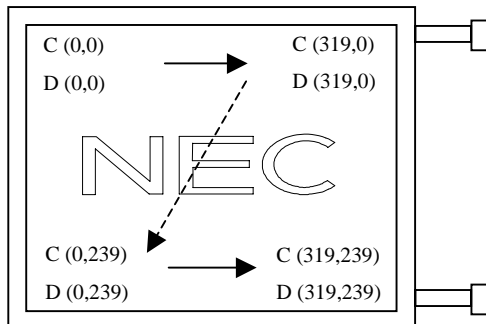
Figure1. DPSH= Low or Open (Normal scan)
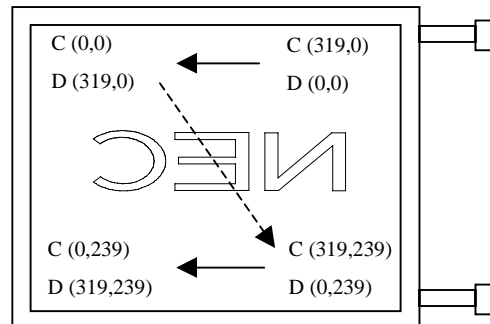   DPSV= Low or Open (Normal scan)

Figure2. DPSH= High (Reverse scan)
          DPSV= Low or Open (Normal scan)
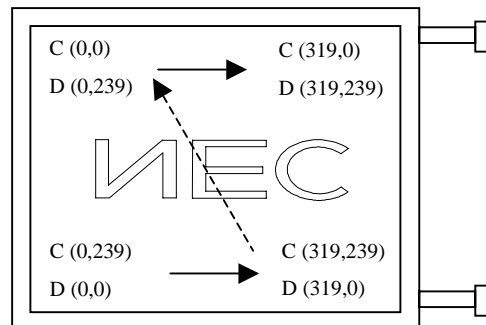
Figure3. DPSH= Low or Open (Normal scan)
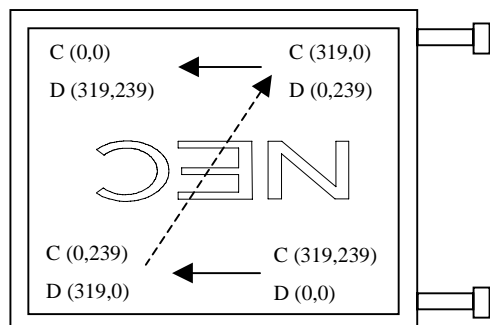   DPSV= High (Reverse scan)

Figure4. DPSH= High (Reverse scan)
          DPSV= High (Reverse scan)
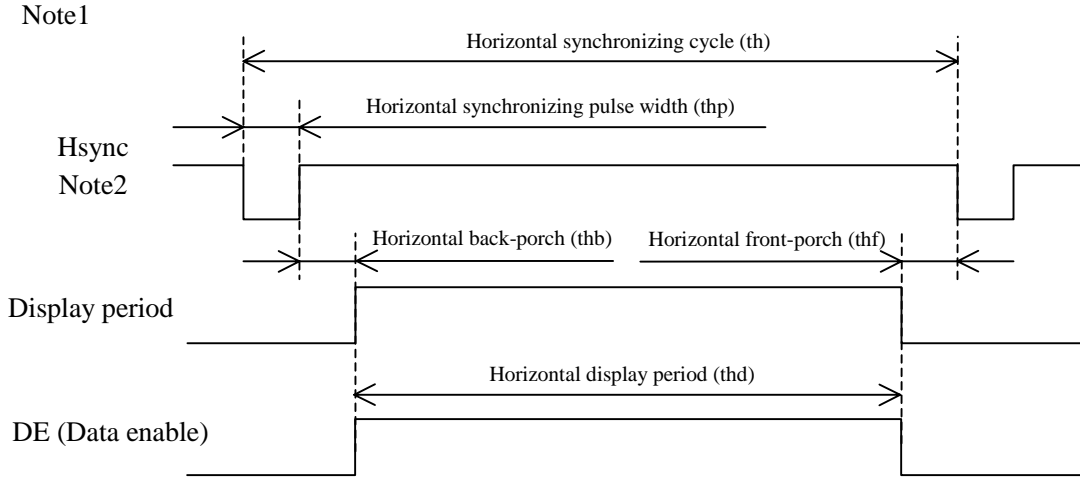
Note1: Meaning of C (X, Y) and D (X, Y)

   C (X, Y): The coordinates of the display position (See "**4.7 DISPLAY POSITIONS**".)

   D (X, Y): The data number of input signal for LCD panel signal processing board
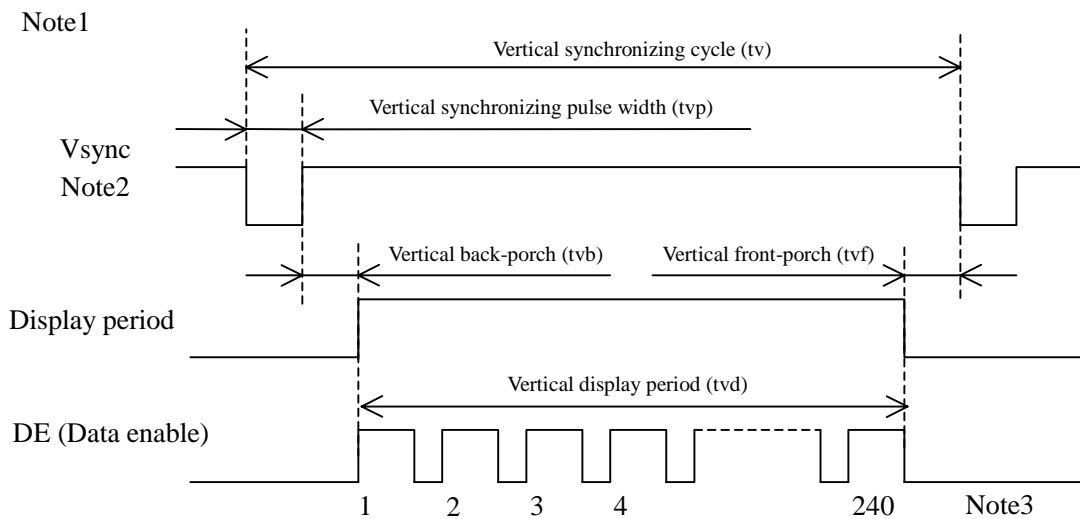
4.9 INPUT SIGNAL TIMINGS

4.9.1 Outline of input signal timings

- Horizontal signal
  Note1

Horizontal synchronizing cycle (th)

Horizontal synchronizing pulse width (thp)

Hsync
Note2

Horizontal back-porch (thb)   Horizontal front-porch (thf)

Display period

Horizontal display period (thd)

DE (Data enable)

- Vertical signal
  Note1

Vertical synchronizing cycle (tv)

Vertical synchronizing pulse width (tvp)

Vsync
Note2

Vertical back-porch (tvb)   Vertical front-porch (tvf)

Display period

Vertical display period (tvd)

DE (Data enable)

1   2   3   4   240   Note3

Note1: This diagram indicates virtual signal for set up to timing.
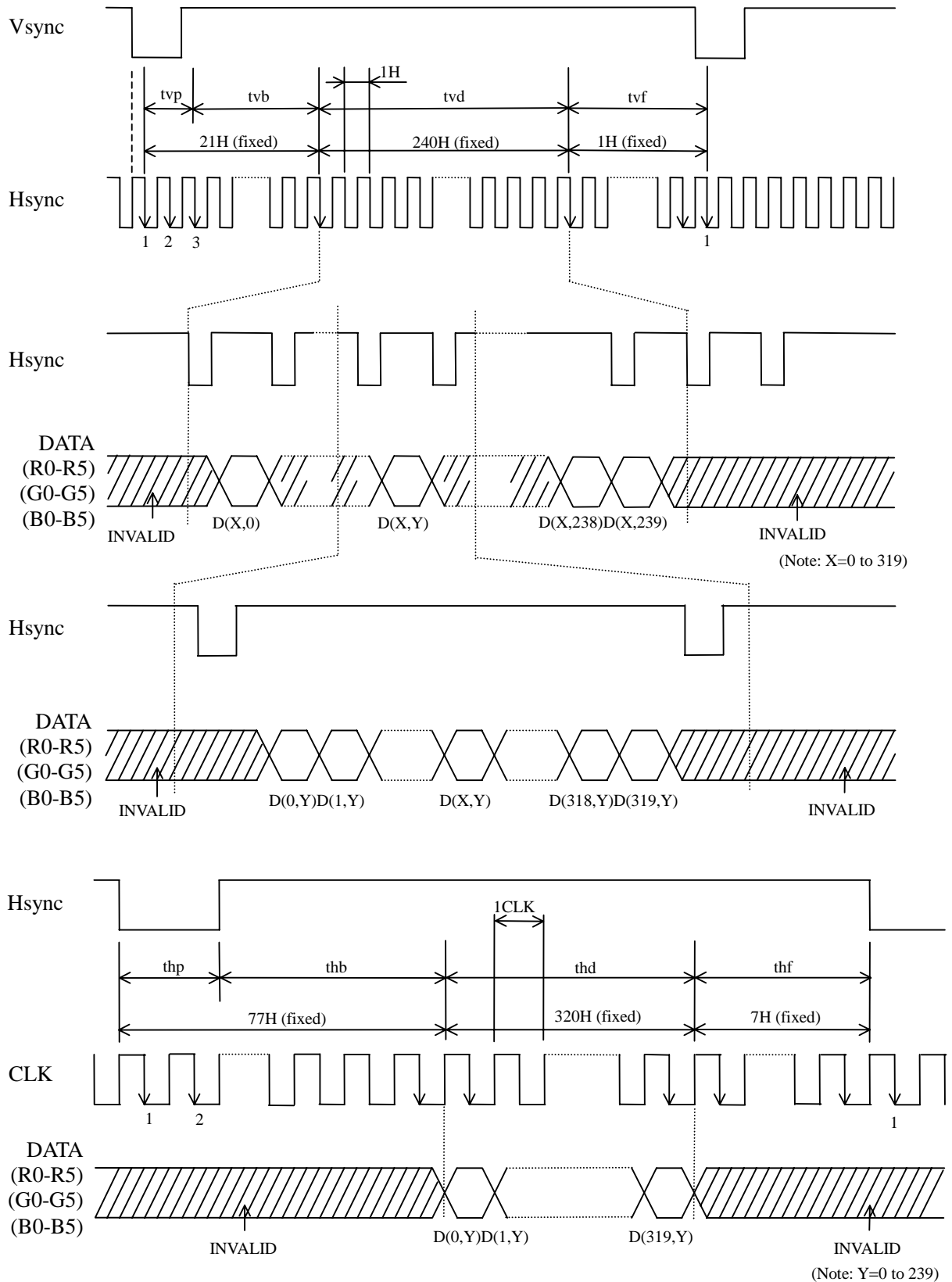Note2: Fixed mode cannot be used while working of DE mode.   ☆
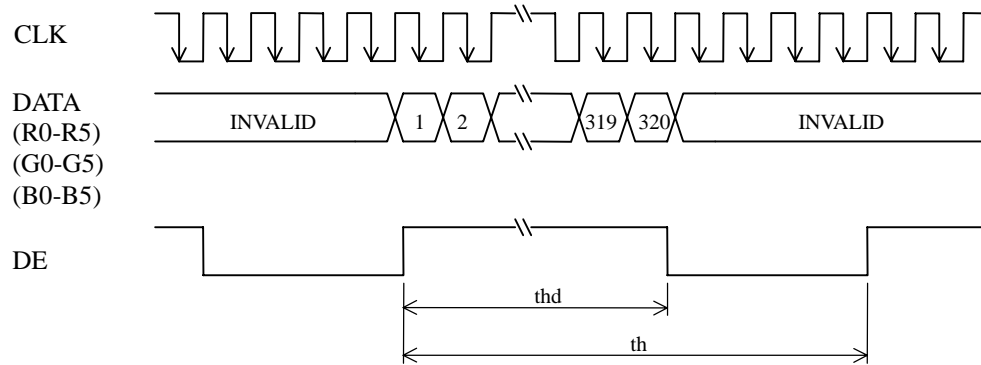Note3: See "**4.9.2 Input signal timing chart**" for numeration of pulse.
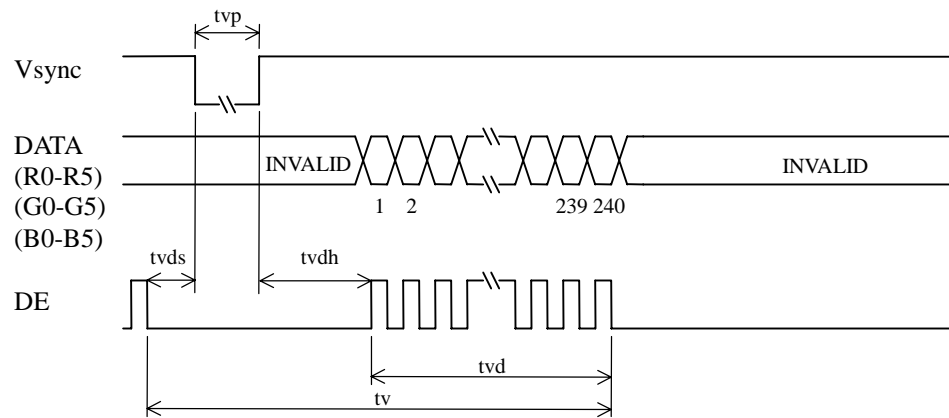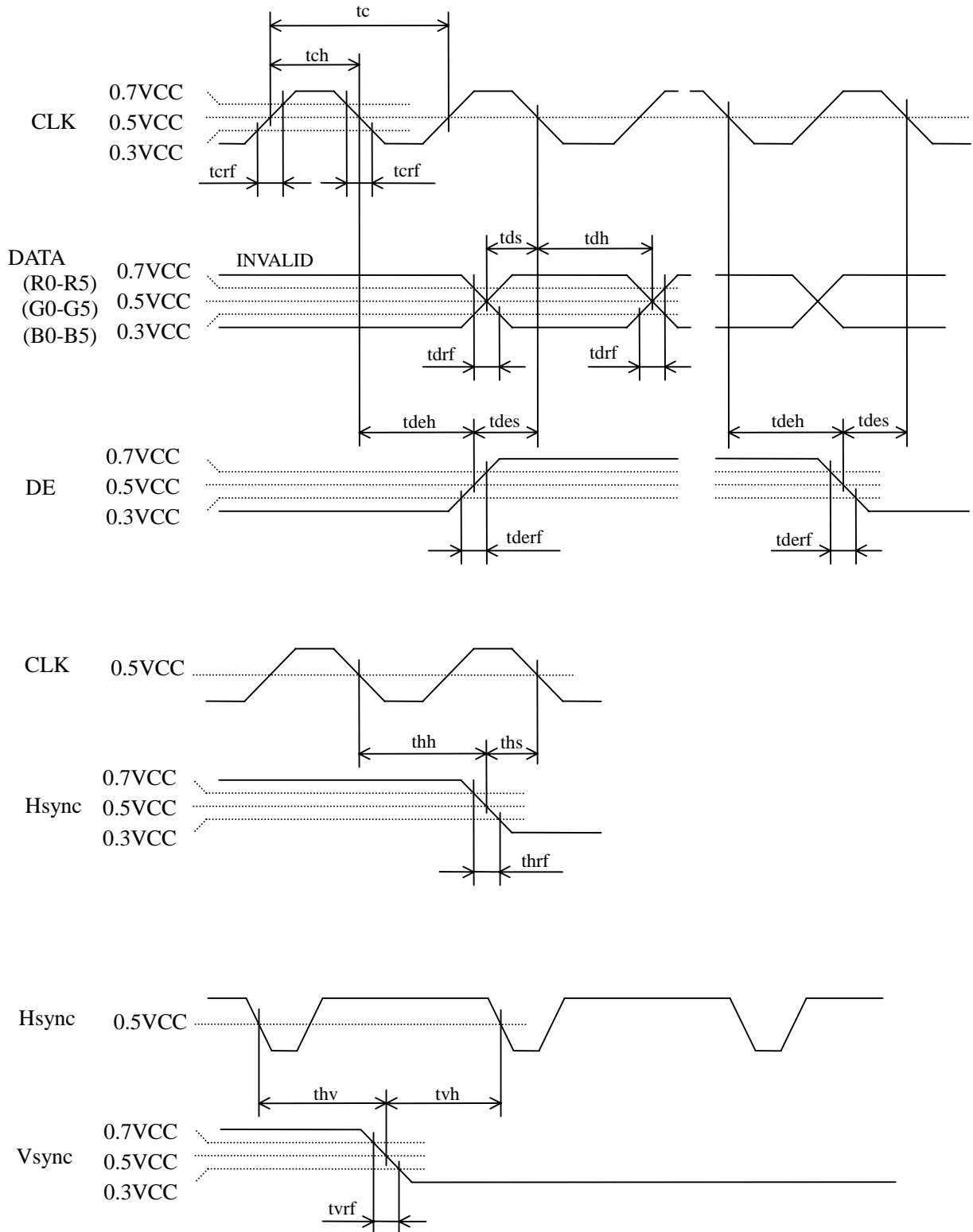
4.9.2 Input signal timing chart

(a) Fixed mode

Vsync

tvp   tvb   1H   tvd   tvf

21H (fixed)   240H (fixed)   1H (fixed)

Hsync

1 2 3   1

Hsync

DATA
(R0-R5)
(G0-G5)
(B0-B5)

INVALID   D(X,0)   D(X,Y)   D(X,238)D(X,239)   INVALID

(Note: X=0 to 319)

Hsync

DATA
(R0-R5)
(G0-G5)
(B0-B5)

INVALID   D(0,Y)D(1,Y)   D(X,Y)   D(318,Y)D(319,Y)   INVALID

Hsync

1CLK

thp   thb   thd   thf

77H (fixed)   320H (fixed)   7H (fixed)

CLK

1   2   1

DATA
(R0-R5)
(G0-G5)
(B0-B5)

INVALID   D(0,Y)D(1,Y)   D(319,Y)   INVALID

(Note: Y=0 to 239)

(b) DE mode

Horizontal timing

Vertical timing

(c) Common

4.9.3 Timing characteristics

(a) Fixed mode

(Note1)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	5.0	6.4	7.0	MHz	157.5 ns (typ.)
	Duty		tcd	0.4	-	0.6	-	-
	Rise time, Fall time		tcrf	-	-	10	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	5	-	-	ns	-
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Hsync	Cycle		th	57.7	63.5	80.8	μs	15.7 kHz (typ.)
					404		CLK	
	Display period		thd		320		CLK	Note2
	Front-porch		thf		7		CLK	
	Pulse width		thp	3	-	76	CLK	
	Back-porch		thb	1	-	74	CLK	
	Total of pulse width and back-porch		thp + thb		77		CLK	
	CLK- Hsync	Setup time	ths	5	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.1	16.6	21.2	ms	60.1 Hz (typ.)
					262		H	
	Display period		tvd		240		H	Note2
	Front-porch		tvf		1		H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb		21		H	
	Hsync-Vsync timing		thv	1	-	-	CLK	-
	Vsync-Hsync timing		tvh	10	-	-	ns	
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tc = 1CLK, tcd = tch/tc, th = 1H

Note2: Keep tvp + tvb and thp + thb within the table.

If it is out of specification, display position will be shifted to right/left side or up/down.

(b) DE mode

(Note1, Note2)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	5.0	6.4	7.0	MHz	157.5 ns (typ.)
	Duty		tcd	0.4	-	0.6	-	-
	Rise time, Fall time		tcrf	-	-	10	ns	
DATA (R0-R5) (G0-G5) (B0-B5)	CLK-DATA	Setup time	tds	5	-	-	ns	-
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	
Vsync	Pulse width		tvp	2	-	20	H	-
	Vsync-DE timing	Setup time	tvds	1	-	-	CLK	
		Hold time	tvdh	1	-	-	CLK	
	Rise time, Fall time		tvrf	-	-	10	μs	
DE	Horizontal	Cycle	th	57.7	63.5	80.8	μs	15.7 kHz (typ.)
				331	404	-	CLK	
		Display period	thd		320		CLK	-
	Vertical (One frame)	Cycle	tv	15.1	16.6	21.2	ms	60.1 Hz (typ.)
				242	262		H	
		Display period	tvd		240		H	
	CLK-DE	Setup time	tdes	5	-	-	ns	-
		Hold time	tdeh	10	-	-	ns	
	Rise time, Fall time		tderf	-	-	10	ns	

Note1: Definition of parameters is as follows.

   tc = 1CLK, tcd = tch/tc, th = 1H

Note2: Hsync signal (Pin No.3 of CN1) is not used inside the product at DE mode.

   Do not keep pin open to avoid noise problem.

4.10 OPTICS

4.10.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Remarks
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	320	400	-	-	Note3
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	320	400	-	cd/m²	-
Luminance uniformity		-	LU	-	1.25	1.35	-	Note4
Chromaticity	White	**x** coordinate	Wx	-	0.305	-	-	Note5
		y coordinate	Wy	-	0.330	-	-	
	Red	**x** coordinate	Rx	-	0.600	-	-	
		y coordinate	Ry	-	0.350	-	-	
	Green	**x** coordinate	Gx	-	0.320	-	-	
		y coordinate	Gy	-	0.560	-	-	
	Blue	**x** coordinate	Bx	-	0.150	-	-	
		y coordinate	By	-	0.130	-	-	
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	-	50	-	%	
Response time		White to Black	Ton	-	5	15	ms	Note6 Note7
		Black to White	Toff	-	25	50	ms	
Viewing angle	Right	θU = 0°, θD = 0°, CR ≥ 10	θR	-	65	-	°	Note8
	Left	θU = 0°, θD = 0°, CR ≥ 10	θL	-	65	-	°	
	Up	θR = 0°, θL = 0°, CR ≥ 10	θU	-	40	-	°	
	Down	θR = 0°, θL = 0°, CR ≥ 10	θD	-	65	-	°	

Note1: These are initial characteristics.   ☆
Note2: Measurement conditions are as follows.
    Ta=25°C, VCC=3.3V, IBL= 5.0mArms/lamp, Display: QVGA, Horizontal cycle = 15.7kHz,
    Vertical cycle = 60.1Hz, DPSH= Open, DPSV= Open   ☆

    Optical characteristics are measured at luminance saturation after 20minutes from working
the product, in the dark room. Also measurement method for luminance is as follows.
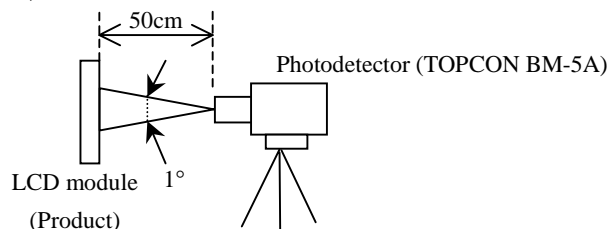
Note3: See "**4.10.2 Definition of contrast ratio**".
Note4: See "**4.10.3 Definition of luminance uniformity**".
Note5: These coordinates are found on CIE 1931 chromaticity diagram.
Note6: Product surface temperature: TopF = 32.5°C
Note7: See "**4.10.4 Definition of response times**".
Note8: See "**4.10.5 Definition of viewing angles**".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

	53	160	266
40	①		②
120		③	
200	④		⑤

☆
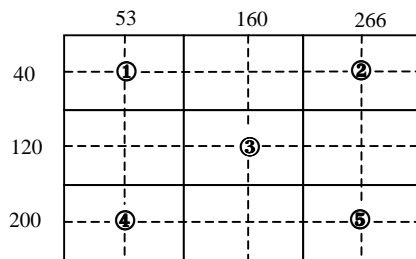
4.10.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).
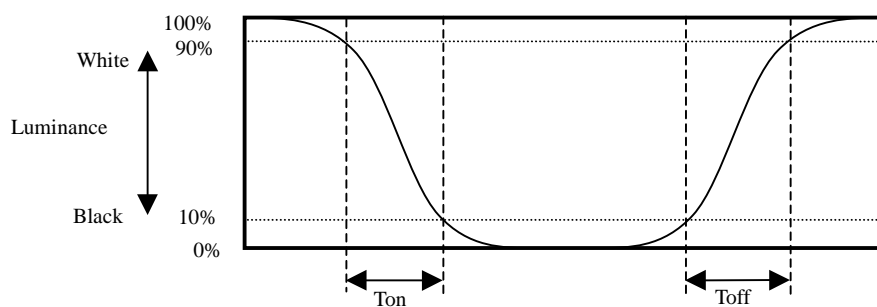
4.10.5 Definition of viewing angles
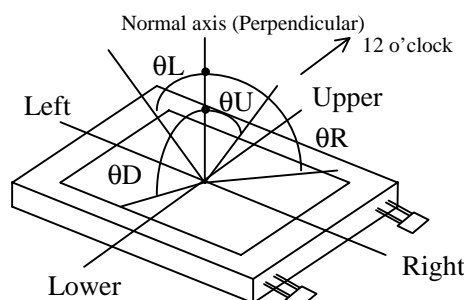
5. RELIABILITY TESTS

Test item	Condition	Judgement
High temperature and humidity (Operation)	① 55 ± 2°C, RH = 85%, 240hours ② Display data is black.	No display malfunctions Note1
High temperature (Operation)	① 70 ± 2°C, 240hours ② Display data is black.	
Heat cycle (Operation)	① -10 ± 3°C…1hour 70 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is black.	
Thermal shock (Non operation)	① -30 ± 3°C…30minutes 80 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Vibration (Non operation)	① 5 to 200Hz, 29.4m/s^2 ② 10 minute/cycle ③ X, Y direction…2hours ④ Z direction…4hours	No display malfunctions No physical damages Note1
Mechanical shock (Non operation)	① 980m/s^2, 11ms ② ±X, ±Y, ±Z direction ③ 3 times each directions	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.

Note2: See the following figure for discharge points.
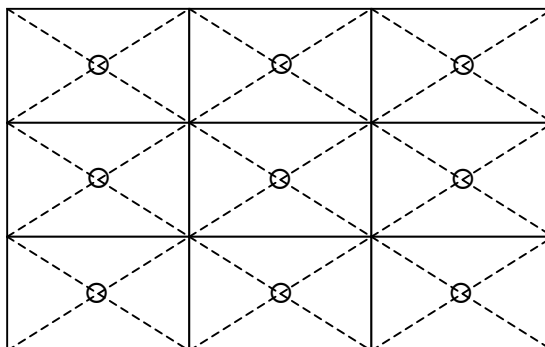
6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding this contents!**

⚠	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
⚡	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
✋	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

⚡
* **Do not touch the working backlight. Customer will be in danger of an electric shock.**

✋
* **Do not touch the working backlight. Customer will be in danger of burn injury.**
* **Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater $980m/s^2$ and to be not greater 11ms, Pressure: To be not greater 19.6 N)**

6.3 ATTENTIONS ⚠

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board cover when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
② Do not hook cables nor pull connection cables such as lamp cable and so on, for fear of damage.
③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
⑤ The torque for mounting screws must never exceed 0.29N·m. Higher torque values might result in distortion of the bezel.
⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area) except mounting hole portion.
Bends or twist described above and undue stress to any portion except mounting hole portion may cause display un-uniformity.

⑦ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

⑧ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp. This damage may cause a lamp breaking and abnormal operation of high voltage circuit.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.

② In order to prevent dew condensation occurring by temperature difference, the product packing box must be opened after leave under the environment of an unpacking room temperature enough. Because a situation of dew condensation occurring is changed by the environmental temperature and humidity, evaluate the leaving time sufficiently. (Recommendation leaving time: 6 hour or more with packing state)

③ Do not operate in high magnetic field. Circuit boards may be broken down by it.

④ This product is not designed as radiation hardened.

⑤ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polavrizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

① Response time, luminance and color may be changed by ambient temperature.

② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.

③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.

④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.

⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight.

⑥ Optical characteristics may be changed by input signal timings.

⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

① All GND, backlight inverter ground (GNDB), VCC and backlight inverter power supply voltage (VDDB) terminals should be used without a non-connected line.

② Do not disassemble a product or adjust variable resistors without permission of NEC.

③ See "REPLACEMENT MANUAL FOR LAMP HOLDER SET", if customer would like to replace backlight lamps.

④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.

⑤ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC for repair and so on.

7. OUTLINE DRAWINGS

7.1 FRONT VIEW
(Unit: mm)

$116.4^{+0.5}_{-0.5}$ (BEZEL OPENING AREA)

111.4 (DISPLAY AREA)

$12.5^{+0.5}_{-0.5}$

UPPER SIDE

DISPLAY CENTER

$104.5^{+0.5}_{-0.5}$

83.5 (DISPLAY AREA)

$88.5^{+0.5}_{-0.5}$ (BEZEL OPENING AREA)

LOWER SIDE

$134.0^{+0.5}_{-0.5}$

$100.0^{+5.0}_{-5.0}$

7.2 REAR VIEW
Unit: mm

MODEL : NL3224BC35-20
SERIAL : **************
PANEL : **************
NEC NEC LCD Technologies, Ltd.　MADE IN JAPAN
E170632

CN2

CN1

CN3

MOUNTING SCREW (M3)
Depth 3.0mm

THE TFT COLOR LCD
PANEL CONTAINS COLD CATHODE
FLOURESCENT LAMPS. PLEASE
FOLLOW LOCAL ORDINANCES
OR REGULATIONS FOR ITS
DISPOSAL

HIGH VOLTAGE
CAUTION
RISK OF ELECTRIC SHOCK
DISCONNECT THE ELECTRIC
POWER BEFORE SERVICE.

$12.5^{+0.5}_{-0.5}$

$100.0^{+5.0}_{-5.0}$

$10.2^{+0.7}_{-0.7}$

$22.3^{+0.5}_{-0.5}$

$30.0^{+0.7}_{-0.7}$

$60.0^{+0.3}_{-0.3}$

$12.5^{+0.5}_{-0.5}$

$4.1^{+0.5}_{-0.5}$

$125.8^{+0.3}_{-0.3}$

$4.1^{+0.5}_{-0.5}$