

TFT MONOCHROME LCD MODULE

NL160120BM27-03

NL160120BM27-03A

54 cm (21.3 Type)

UXGA

LVDS Interface (2 ports)

DATA SHEET 

DOD-PD-1216 (3rd edition)

**This DATA SHEET is updated document from
DATA SHEET DOD-PD-0886(2).**

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Please confirm the sales representative before
starting to design your system.**

INTRODUCTION

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Examples: Military systems, aircraft control equipment, aerospace equipment, nuclear reactor control systems, medical equipment/devices/systems for life support, etc.

The quality grade of this product is the "**Standard**" unless otherwise specified in this document.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL160120BM27-03 and NL160120BM27-03A are composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

- Ultra-wide viewing angle (Adoption of Super-Advanced Super Fine TFT (SA-SFT))
- High luminance
- High contrast
- High resolution
- 256 gray scales per 1 sub-pixel (8-bit)
- LVDS interface
- Adjustable gamma characteristics by using built-in 10-bit LUT (look up table)
- Selectable LVDS data input map
- Small foot print
- Incorporated edge light type backlight (without inverter)
- Replaceable backlight
- Difference between NL160120BM27-03 and NL160120BM27-03A

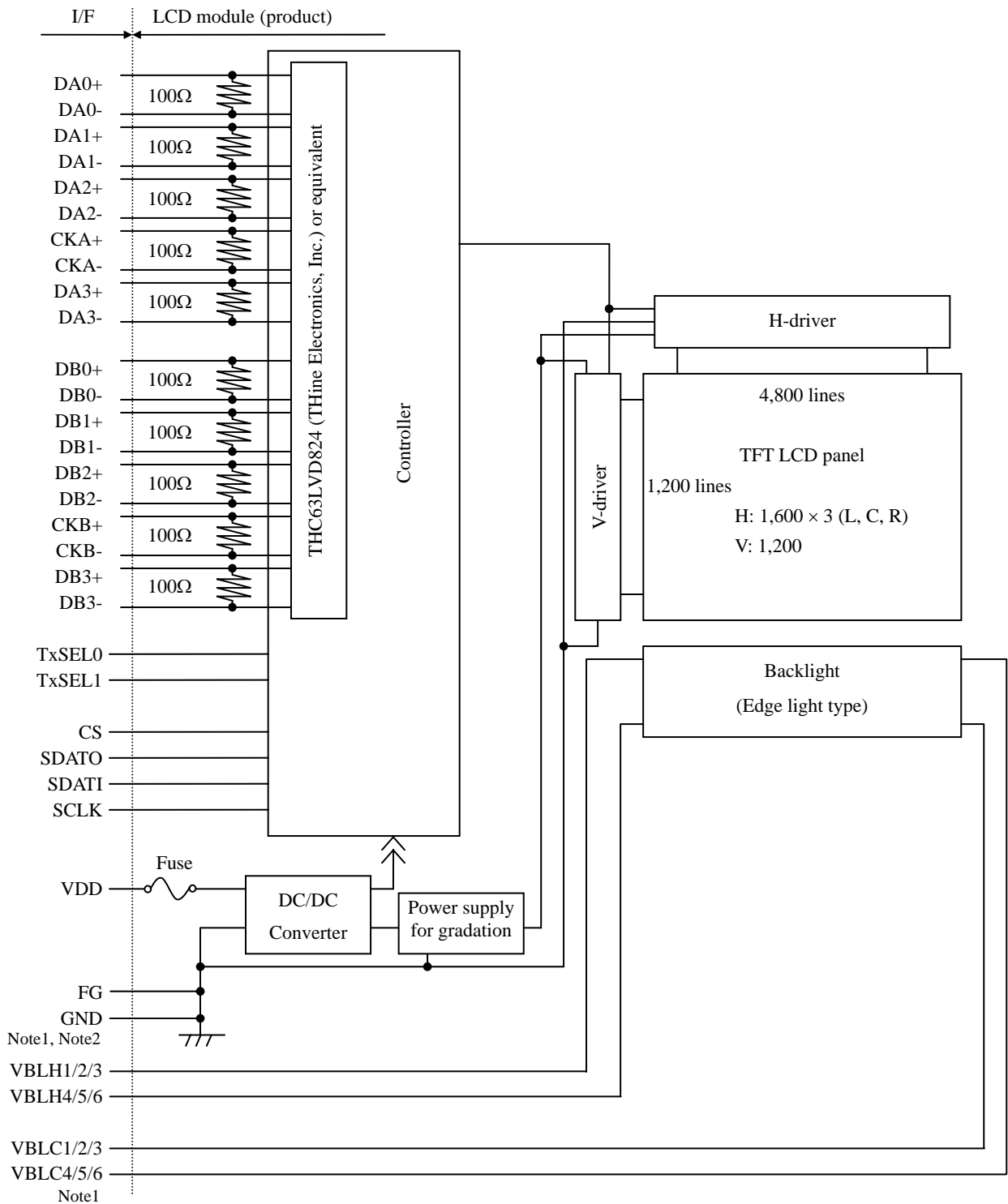
Item	NL160120BM27-03	NL160120BM27-03A
White chromaticity	W _x , W _y = (0.255, 0.310) (typ.)	W _x , W _y = (0.280, 0.304) (typ.)
Backlight unit (Replaceable part)	213LHS06	213LHS11
Cable color of backlight lamps	See " 4.5.2 Backlight lamp ".	

2. GENERAL SPECIFICATIONS

Display area	432.0 (H) × 324.0 (V) mm	
Diagonal size of display	54cm (21.3 inches)	
Drive system	a-Si TFT active matrix	
Display grayscale	256 gray scales per 1 sub-pixel (8-bit) (766 gray scales per 1 pixel)	
Pixel	1,600 (H) × 1,200 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)	
Pixel arrangement	LCR vertical stripe	
Dot pitch	0.090 (H) × 0.270 (V) mm	
Pixel pitch	0.270 (H) × 0.270 (V) mm	
Module size	457.0 (W) × 350.0 (H) × 25.0 (D) mm (typ.)	
Weight	3,750 g (typ.)	
Contrast ratio	700:1 (typ.)	
Viewing angle	At the contrast ratio ≥ 10:1 <ul style="list-style-type: none"> • Horizontal: Right side 85° (typ.), Left side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.) 	
Designed viewing direction	Viewing angle with optimum grayscale (γ= DICOM): normal axis (perpendicular) Note1	
Polarizer surface	Antiglare	
Polarizer pencil-hardness	2H (min.) [by JIS K5400]	
Response time	Ton+Toff (10%←→90%) 35 ms (typ.)	
Luminance	At IBL= 6.0mArms / lamp 1,000 cd/m ² (typ.)	
White chromaticity	NL160120BM27-03	Wx, Wy = (0.255, 0.310) (typ.)
	NL160120BM27-03A	Wx, Wy = (0.280, 0.304) (typ.)
Signal system	2 ports LVDS interface (THC63LVD824 THine Electronics, Inc. or equivalent) [LCR 8-bit signals, Data enable signal (DE), Dot clock (CLK)]	
Power supply voltage	LCD panel signal processing board: 12.0V	
Backlight	Edge light type: 6 cold cathode fluorescent lamps (without inverter) (Replaceable part • Backlight unit: Type No. 213LHS06 for NL160120BM27-03 213LHS11 for NL160120BM27-03A)	
Power consumption	At IBL= 6.0mArms/lamp, Checkered flag pattern 30.7 W (typ., Power dissipation of the inverter is not included.)	

Note1: When the product luminance is 800cd/m², the gamma characteristic is designed to γ=DICOM.

3. BLOCK DIAGRAM



Note1: Connections between GND (Signal ground), FG (Frame ground) and VBLC (Lamp low voltage terminal) in the product

GND - FG	Connected
GND - VBLC	Not connected
FG - VBLC	Not connected

Note2: GND and FG must be connected to customer equipment's ground, and it is recommended that GND, FG and customer inverter ground are connected together in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 25.0 ± 0.5 (D) Note1, Note2	mm
Display area	432.0 (H) × 324.0 (V) Note1	mm
Weight	3,750 (typ.), 4,000 (max.)	g

Note1: Excluding warpage of the signal processing board cover and the connection board cover

Note2: See "7. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board	VDD	-0.3 to +14.0	V	Ta = 25°C
	Lamp voltage	VBLH	2,000	Vrms	
Input signal voltage Note1		Vi	-0.3 to +2.8	V	Ta = 25°C VDD=12.0V
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature	Front surface	TopF	0 to +55	°C	Note2
	Rear surface	TopR	0 to + 60	°C	Note3
Relative humidity Note4		RH	≤ 70	%	Ta ≤ 55°C
Absolute humidity Note4		AH	≤ 73 Note5	g/m ³	Ta > 55°C
Operating altitude		-	≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude		-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-
CS, SDATI, SCLK, TxSEL0, TxSEL1

Note2: Measured at center of LCD panel surface (including self-heat)

Note3: Measured at center of LCD module's rear shield surface (including self-heat)

Note4: No condensation

Note5: Water amount at Ta = 55°C and RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDD	10.8	12.0	13.2	V	-
Supply current		IDD	-	310 Note1	700 Note2	mA	at VDD=12.0V
Ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input Threshold voltage	High	VTH	-	-	+100	mV	at VCM=1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-
Control signal input threshold voltage	High	VIH	Keep this pin open.			-	Note5
	Low	VIL	0	-	0.5	V	
Control signal input current	Low	IIL	-10	-	10	μA	
Serial communication signal input threshold voltage	High	V+	-	1.4	1.9	V	Note6
	Low	V-	0.4	0.7	-	V	
	Hysteresis	VH	0.3	-	-	V	
Output signal threshold voltage	High	VOH	1.9	-	-	V	Note7
	Low	VOL	-	-	0.4	V	
Output signal current	High	IOH	-4	-	-	mA	
	Low	IOL	-	-	4	mA	

Note1: Checkered flag pattern (by EIAJ ED-2522)

Note2: Pattern for maximum current

Note3: Common mode voltage for LVDS driver

Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, CKB+/-

Note5: TxSEL0, TxSEL1

Note6: CS, SDATI, SCLK

Note7: SDATO

4.3.2 Backlight lamp

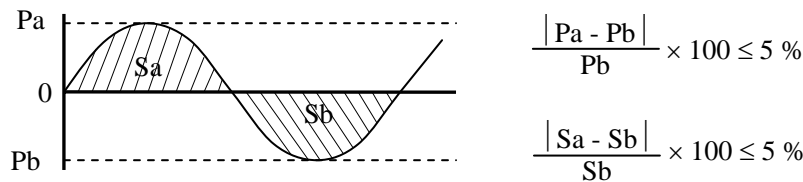
(Ta=25°C, Note1)

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Lamp current	IBL	3.0	6.0	7.0	mArms	at IBL=6.0mArms: L=1,000cd/m ² (typ.) Note3, Note5
Lamp voltage	VBLH	-	750	-	Vrms	Note2, Note3
Lamp starting voltage	VS	1,220	-	-	Vrms	Ta = 25°C Note2, Note3
		1,460	-	-	Vrms	Ta = 0°C Note2, Note3
Lamp oscillation frequency	FO	50	56	60	kHz	Note4

Note1: This product consists of 6 backlight lamps, and these specifications are for each lamp.

Note2: The lamp voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note3: The asymmetric ratio of working waveform for lamps (Lamp voltage peak ratio, Lamp current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal). When designing the inverter, evaluate asymmetric of lamp working waveform sufficiently.



Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note4: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal cycle period (See "4.8.1 Timing characteristics".)

n: Natural number (1, 2, 3)

Note5: Method of lamp cable installation may invite fluctuation of lamp current and voltage or asymmetric of lamp working waveform. When designing method of lamp cable installation, evaluate the fluctuation of lamp current, voltage and working waveform sufficiently.

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage (Measure at input terminal of power supply)	Note1	Unit
VDD	12.0 V	≤ 100		mVp-p

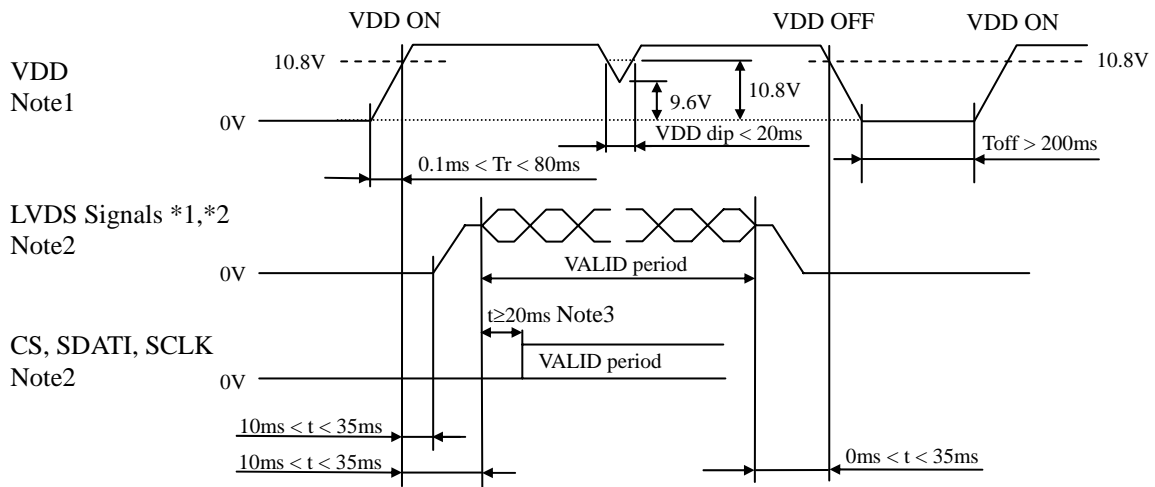
Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16132AB	KAMAYA ELECTRIC Co., Ltd.	1.25 A	2.5 A, 5s max.	Note1
			32V		

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE



- *1: LVDS signals: DA0+/-, DA1+/-, DA2+/-, DA3+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/- and CKB+/-
- *2: LVDS signals should be measured at the terminal of 100Ω resistance.

Note1: In terms of voltage variation (voltage drop) while VDD rising edge is below 10.8V, a protection circuit may work, and then this product may not work.

Note2: LVDS signals and CS, SDATI, SCLK must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged. If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. VDD should be cut when the display and function signals are stopped.

Note3: At the beginning of the serial communication mode, take 20ms or more after the LVDS signal input. When writing and reading the LUT data, see “4.10 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT”.

Note4: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

(1) CN1

Socket (LCD module side): DF19G-30P-1H (56) (Hirose Electric Co., Ltd. (HRS))

☆

Adaptable plug: DF19-30S-1C (Hirose Electric Co., Ltd. (HRS))

Pin No.	Symbol	Signal	Remarks			
1	DA0-	Pixel data A0	Odd pixel data Input (LVDS differential signal) Note1			
2	DA0+					
3	DA1-	Pixel data A1	Odd pixel data Input (LVDS differential signal) Note1			
4	DA1+					
5	DA2-	Pixel data A2	Odd pixel data Input (LVDS differential signal) Note1			
6	DA2+					
7	GND	Ground	Signal ground Note2			
8	CKA-	Pixel clock	Odd pixel clock Input (LVDS differential signal) Note1			
9	CKA+					
10	DA3-	Pixel data A3	Odd pixel data Input (LVDS differential signal) Note1			
11	DA3+					
12	DB0-	Pixel data B0	Even pixel data Input (LVDS differential signal) Note1			
13	DB0+					
14	GND	Ground	Signal ground Note2			
15	DB1-	Pixel data B1	Even pixel data Input (LVDS differential signal) Note1			
16	DB1+					
17	GND	Ground	Signal ground Note2			
18	DB2-	Pixel data B2	Even pixel data Input (LVDS differential signal) Note1			
19	DB2+					
20	CKB-	Pixel clock	Even pixel clock Input (LVDS differential signal) Note1			
21	CKB+					
22	DB3-	Pixel data B3	Even pixel data Input (LVDS differential signal) Note1			
23	DB3+					
24	GND	Ground	Signal ground Note2			
25	TxSEL0	Selection of LVDS data input map	Note3, Note4	TxSEL1	TxSEL0	Mode
26	TxSEL1			Open	Open	A
				Open	Low	B
				Low	Open	C
		Low	Low	A		
27	GND	Ground	Signal ground Note2			
28	VDD	Power supply	12V Note2			
29	VDD					
30	VDD					

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note2: All GND and VDD terminals should be used without any non-connected lines.

Note3: This terminal is pulled-up in the product. (Pull-up resistance: 50kΩ)

Note4: See "4.6 LVDS DATA INPUT MAP".

(2) CN3

Socket (LCD module side): SM10B-SRSS-TB(LF)(SN) (J.S.T. Mfg Co., Ltd.)

☆

Adaptable plug: SHR-10V-S, SHR-10V-S-B or 10SR-3S (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	RSVD	Reserved	Keep open
2	RSVD	Reserved	Keep open
3	RSVD	Reserved	Keep open
4	GND	Ground	Signal ground Note1
5	CS	Chip selection	For LUT communication control Note2
6	SDATO	Serial data output	For LUT output signal
7	SDATI	Serial data input	For LUT communication control Note3
8	SCLK	Serial clock	For LUT communication control Note3
9	GND	Ground	Signal ground Note1
10	RSVD	Reserved	Keep open

Note1: All GND terminals should be used without any non-connected lines.

Note2: These terminals are pulled-up in the product. (Pull-up resistance: 50kΩ)

Note3: These terminals are pulled-down in the product. (Pull-down resistance: 50kΩ)

4.5.2 Backlight lamp

Attention: VBLH and VBLC must be connected correctly. Wrong connections will cause electric shock and also break down of the product.

(1) NL160120BM27-03

CN201 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) ☆
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH1	Upper side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC1	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN202 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) ☆
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH2	Upper side lamp, High voltage (Hot)	Cable color: White
2	VBLC2	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN203 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) ☆
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH3	Upper side lamp, High voltage (Hot)	Cable color: Blue
2	VBLC3	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN204 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) ☆
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH4	Lower side lamp, High voltage (Hot)	Cable color: Pink
2	VBLC4	Lower side lamp, Low voltage (Cold)	Cable color: Gray

CN205 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) ☆
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH5	Lower side lamp, High voltage (Hot)	Cable color: White
2	VBLC5	Lower side lamp, Low voltage (Cold)	Cable color: Gray

CN206 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN) ☆
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

Pin No.	Symbol	Function	Remarks
1	VBLH6	Lower side lamp, High voltage (Hot)	Cable color: Blue
2	VBLC6	Lower side lamp, Low voltage (Cold)	Cable color: Gray

(2) NL160120BM27-03A

CN201 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN)
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

☆

Pin No.	Symbol	Function	Remarks
1	VBLH1	Upper side lamp, High voltage (Hot)	Cable color: Red
2	VBLC1	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN202 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN)
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

☆

Pin No.	Symbol	Function	Remarks
1	VBLH2	Upper side lamp, High voltage (Hot)	Cable color: White
2	VBLC2	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN203 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN)
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

☆

Pin No.	Symbol	Function	Remarks
1	VBLH3	Upper side lamp, High voltage (Hot)	Cable color: Blue
2	VBLC3	Upper side lamp, Low voltage (Cold)	Cable color: Gray

CN204 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN)
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

☆

Pin No.	Symbol	Function	Remarks
1	VBLH4	Lower side lamp, High voltage (Hot)	Cable color: Red
2	VBLC4	Lower side lamp, Low voltage (Cold)	Cable color: Gray

CN205 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN)
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

☆

Pin No.	Symbol	Function	Remarks
1	VBLH5	Lower side lamp, High voltage (Hot)	Cable color: White
2	VBLC5	Lower side lamp, Low voltage (Cold)	Cable color: Gray

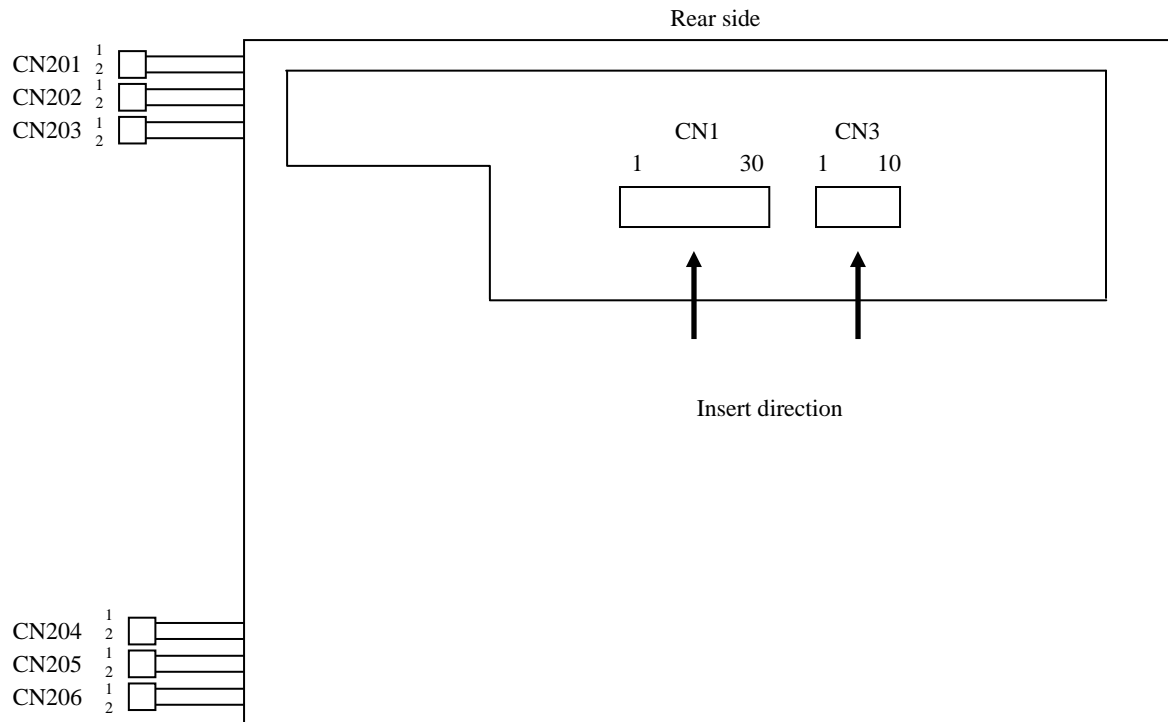
CN206 plug (LCD module side): BHSR-02VS-1 (J.S.T. Mfg Co., Ltd.)

Adaptable socket: SM02B-BHSS-1-TB(LF)(SN)
SM02B-BHSS-1-TB (J.S.T. Mfg Co., Ltd.)

☆

Pin No.	Symbol	Function	Remarks
1	VBLH6	Lower side lamp, High voltage (Hot)	Cable color: Blue
2	VBLC6	Lower side lamp, Low voltage (Cold)	Cable color: Gray

4.5.3 Positions of plug and socket



4.6 LVDS DATA INPUT MAP

4.6.1 Mode A

Input data		Transmitter		CN1			
		Pin	THC63LVDF83A			Pin	THC63LVD823
Odd pixel data and control signal	Note1 LA2 →	51	TA0	53	R12	Note2 Pin Symbol 1 DA0- 2 DA0+ 3 DA1- 4 DA1+ 5 DA2- 6 DA2+ 7 GND 8 CKA- 9 CKA+ 10 DA3- 11 DA3+ 12 DB0- 13 DB0+ 14 GND 15 DB1- 16 DB1+ 17 GND 18 DB2- 19 DB2+ 20 CKB- 21 CKB+ 22 DB3- 23 DB3+ 24 GND 25 TxSEL0 26 TxSEL1 27 GND 28 VDD 29 VDD 30 VDD	
	LA3 →	52	TA1	54	R13		
	LA4 →	54	TA2	57	R14		
	LA5 →	55	TA3	58	R15		
	LA6 →	56	TA4	59	R16		
	LA7 →	3	TA5	60	R17		
	CA2 →	4	TA6	63	G12		
	CA3 →	6	TB0	64	G13		
	CA4 →	7	TB1	65	G14		
	CA5 →	11	TB2	66	G15		
	CA6 →	12	TB3	67	G16		
	CA7 →	14	TB4	68	G17		
	RA2 →	15	TB5	73	B12		
	RA3 →	19	TB6	74	B13		
	RA4 →	20	TC0	75	B14		
	RA5 →	22	TC1	76	B15		
	RA6 →	23	TC2	77	B16		
	RA7 →	24	TC3	78	B17		
	Note3 RSVD →	27	TC4	7	RSVD		
	Note3 RSVD →	28	TC5	8	RSVD		
	DE →	30	TC6	9	DE		
	LA0 →	50	TD0	51	R10		
	LA1 →	2	TD1	52	R11		
	CA0 →	8	TD2	61	G10		
	CA1 →	10	TD3	62	G11		
	RA0 →	16	TD4	69	B10		
	RA1 →	18	TD5	70	B11		
	Note1 RSVD →	25	TD6	-	-		
	CLK →	31	CLKIN	10	CLK		
	Even pixel data	LB2 →	51	TA0	81		R22
		LB3 →	52	TA1	82		R23
LB4 →		54	TA2	83	R24		
LB5 →		55	TA3	84	R25		
LB6 →		56	TA4	85	R26		
LB7 →		3	TA5	86	R27		
CB2 →		4	TA6	91	G22		
CB3 →		6	TB0	92	G23		
CB4 →		7	TB1	93	G24		
CB5 →		11	TB2	94	G25		
CB6 →		12	TB3	95	G26		
CB7 →		14	TB4	96	G27		
RB2 →		15	TB5	99	B22		
RB3 →		19	TB6	100	B23		
RB4 →		20	TC0	1	B24		
RB5 →		22	TC1	2	B25		
RB6 →		23	TC2	5	B26		
RB7 →		24	TC3	6	B27		
Note3 RSVD →		27	TC4	-	-		
Note3 RSVD →		28	TC5	-	-		
Note3 RSVD →		30	TC6	-	-		
LB0 →		50	TD0	79	R20		
LB1 →		2	TD1	80	R21		
CB0 →		8	TD2	89	G20		
CB1 →		10	TD3	90	G21		
RB0 →		16	TD4	97	B20		
RB1 →		18	TD5	98	B21		
Note3 RSVD →		25	TD6	-	-		
CLK →		31	CLKIN	-	-		

4.6.2 Mode B

Input data		Transmitter		CN1					
		Pin	DS90CF383, C385						
Odd pixel data and control signal	Note1	LA7 →	51 TXIN0	1st	Note2	Pin	Symbol		
		LA6 →	52 TXIN1		TA1- →	1	DA0-		
		LA5 →	54 TXIN2		TA1+ →	2	DA0+		
		LA4 →	55 TXIN3						
		LA3 →	56 TXIN4		TB1- →	3	DA1-		
		LA2 →	3 TXIN6		TB1+ →	4	DA1+		
		CA7 →	4 TXIN7						
		CA6 →	6 TXIN8		TC1- →	5	DA2-		
		CA5 →	7 TXIN9		TC1+ →	6	DA2+		
		CA4 →	11 TXIN12			7	GND		
		CA3 →	12 TXIN13		TCLK1- →	8	CKA-		
		CA2 →	14 TXIN14		TCLK1+ →	9	CKA+		
		RA7 →	15 TXIN15						
		RA6 →	19 TXIN18		TD1- →	10	DA3-		
		RA5 →	20 TXIN19		TD1+ →	11	DA3+		
		RA4 →	22 TXIN20						
		RA3 →	23 TXIN21						
		RA2 →	24 TXIN22						
	Note3	RSVD →	27 TXIN24						
	Note3	RSVD →	28 TXIN25						
		DE →	30 TXIN26						
		LA1 →	50 TXIN27						
		LA0 →	2 TXIN5						
		CA1 →	8 TXIN10						
		CA0 →	10 TXIN11						
		RA1 →	16 TXIN16						
		RA0 →	18 TXIN17						
	Note3	RSVD →	25 TXIN23						
		CLK →	31 CLKIN						
	Even pixel data		LB7 →		51 TXIN0	2nd			
			LB6 →		52 TXIN1		TA2- →	12	DB0-
		LB5 →	54 TXIN2	TA2+ →	13		DB0+		
		LB4 →	55 TXIN3		14		GND		
		LB3 →	56 TXIN4	TB2- →	15		DB1-		
		LB2 →	3 TXIN6	TB2+ →	16		DB1+		
		CB7 →	4 TXIN7		17		GND		
		CB6 →	6 TXIN8	TC2- →	18		DB2-		
		CB5 →	7 TXIN9	TC2+ →	19		DB2+		
		CB4 →	11 TXIN12						
		CB3 →	12 TXIN13	TCLK2- →	20		CKB-		
		CB2 →	14 TXIN14	TCLK2+ →	21		CKB+		
		RB7 →	15 TXIN15						
		RB6 →	19 TXIN18	TD2- →	22		DB3-		
		RB5 →	20 TXIN19	TD2+ →	23		DB3+		
		RB4 →	22 TXIN20		24		GND		
		RB3 →	23 TXIN21		25		TxSEL0		
		RB2 →	24 TXIN22		26		TxSEL1		
Note3		RSVD →	27 TXIN24		27		GND		
Note3		RSVD →	28 TXIN25		28		VDD		
Note3		RSVD →	30 TXIN26		29		VDD		
		LB1 →	50 TXIN27		30		VDD		
		LB0 →	2 TXIN5						
		CB1 →	8 TXIN10						
		CB0 →	10 TXIN11						
		RB1 →	16 TXIN16						
		RB0 →	18 TXIN17						
Note3		RSVD →	25 TXIN23						
		CLK →	31 CLKIN						

4.6.3 Mode C

Input data		Transmitter		CN1					
		Pin	DS90CF383, C385						
Odd pixel data and control signal	Note1	LA7 →	51 TXIN0	1st	Note2	TA1- →	1 DA0-		
		LA6 →	52 TXIN1		TA1+ →	2 DA0+			
		LA5 →	54 TXIN2		TB1- →	3 DA1-			
		LA4 →	55 TXIN3		TB1+ →	4 DA1+			
		LA3 →	56 TXIN4		TC1- →	5 DA2-			
		LA2 →	3 TXIN6		TC1+ →	6 DA2+			
		CA7 →	4 TXIN7		TCLK1- →	7 GND			
		CA6 →	6 TXIN8		TCLK1+ →	8 CKA-			
		CA5 →	7 TXIN9			9 CKA+			
		CA4 →	11 TXIN12		TD1- →	10 DA3-			
		CA3 →	12 TXIN13		TD1+ →	11 DA3+			
		CA2 →	14 TXIN14						
		RA7 →	15 TXIN15						
		RA6 →	19 TXIN18						
		RA5 →	20 TXIN19						
		RA4 →	22 TXIN20						
		RA3 →	23 TXIN21						
		RA2 →	24 TXIN22						
	Note3	RSVD →	27 TXIN24						
	Note3	RSVD →	28 TXIN25						
		DE →	30 TXIN26						
		LA1 →	50 TXIN27						
		LA0 →	2 TXIN5						
		CA1 →	8 TXIN10						
		CA0 →	10 TXIN11						
		RA1 →	16 TXIN16						
		RA0 →	18 TXIN17						
	Note3	RSVD →	25 TXIN23						
		CLK →	31 CLKIN						
	Even pixel data		LB7 →		51 TXIN0	2nd		TA2- →	12 DB0-
			LB6 →		52 TXIN1		TA2+ →	13 DB0+	
		LB5 →	54 TXIN2	TB2- →	14 GND				
		LB4 →	55 TXIN3	TB2+ →	15 DB1-				
		LB3 →	56 TXIN4		16 DB1+				
		LB2 →	3 TXIN6	TC2- →	17 GND				
		CB7 →	4 TXIN7	TC2+ →	18 DB2-				
		CB6 →	6 TXIN8		19 DB2+				
		CB5 →	7 TXIN9	TCLK2- →	20 CKB-				
		CB4 →	11 TXIN12	TCLK2+ →	21 CKB+				
		CB3 →	12 TXIN13	TD2- →	22 DB3-				
		CB2 →	14 TXIN14	TD2+ →	23 DB3+				
		RB7 →	15 TXIN15		24 GND				
		RB6 →	19 TXIN18		25 TxSEL0				
		RB5 →	20 TXIN19		26 TxSEL1				
		RB4 →	22 TXIN20		27 GND				
		RB3 →	23 TXIN21		28 VDD				
		RB2 →	24 TXIN22		29 VDD				
Note3		RSVD →	27 TXIN24		30 VDD				
Note3		RSVD →	28 TXIN25						
Note3		RSVD →	30 TXIN26						
		LB1 →	50 TXIN27						
		LB0 →	2 TXIN5						
		CB1 →	8 TXIN10						
		CB0 →	10 TXIN11						
		RB1 →	16 TXIN16						
		RB0 →	18 TXIN17						
Note3		RSVD →	25 TXIN23						
		CLK →	31 CLKIN						

Note1: LSB (Least Significant Bit) – LA0, CA0, RA0, LB0, CB0, RB0
 MSB (Most Significant Bit) – LA7, CA7, RA7, LB7, CB7, RB7

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

Note3: Input signal RSVD is not used inside the product, but do not keep pin open to avoid noise problem.

4.7 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 256 gray scales in each LCR sub-pixel and 766 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as the following table.

Display grayscale		Data signal (0: Low level, 1: High level)																							
		LA7 LA6 LA5 LA4 LA3 LA2 LA1 LA0								CA7 CA6 CA5 CA4 CA3 CA2 CA1 CA0								RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0							
		LB7 LB6 LB5 LB4 LB3 LB2 LB1 LB0	CB7 CB6 CB5 CB4 CB3 CB2 CB1 CB0	RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0																					
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:							:								:				
	↓					:							:								:				
bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:							:								:				
	↓					:							:								:				
bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	
White	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:							:								:				
	↓					:							:								:				
bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

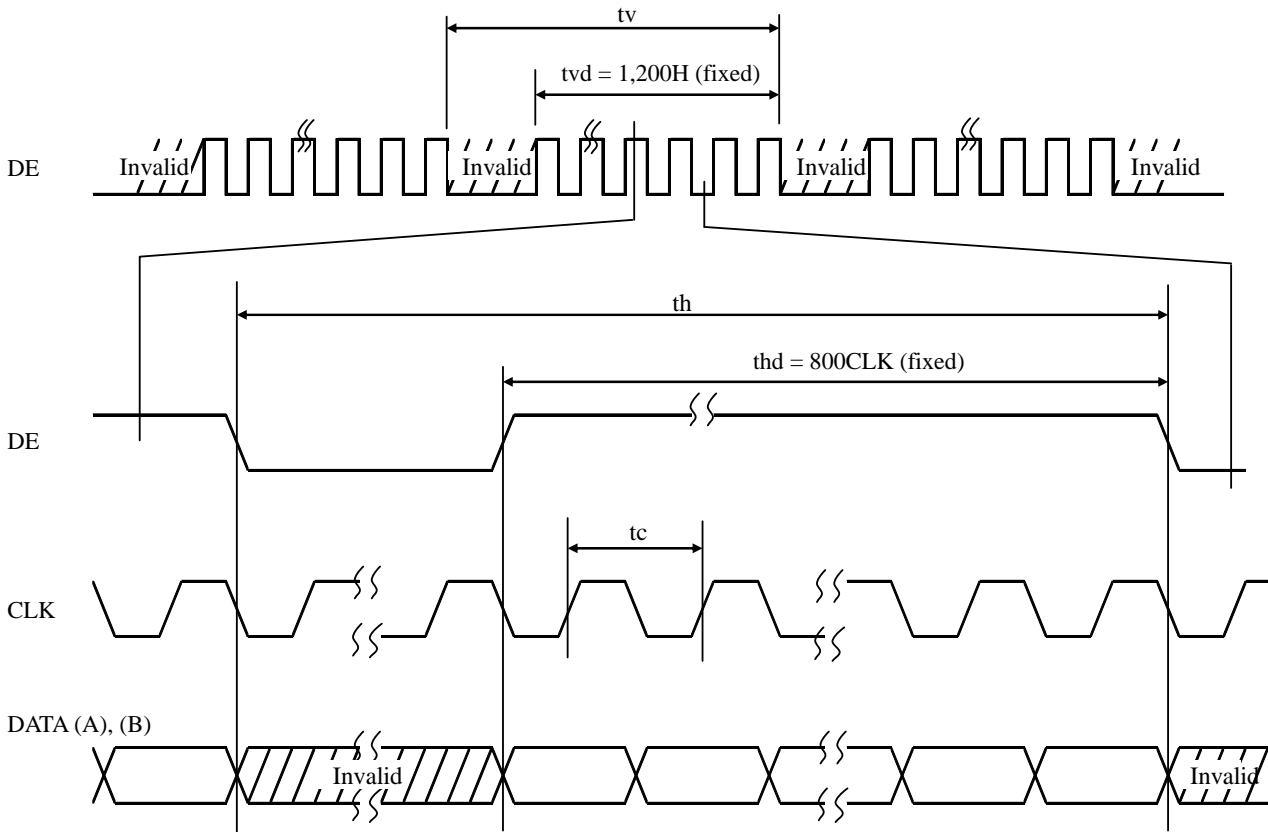
4.8 INPUT SIGNAL TIMINGS

4.8.1 Timing characteristics

Parameter	Symbol	min.	typ.	max.	Unit	Remarks		
CLK	Frequency	1/ tc	60.0	64.5	65.0	MHz	LVDS transmitter input	
	Pulse width	tc	15.38	15.5	-	ns		
	Duty	-	See the data sheet of LVDS transmitter.			-		-
	Rise, fall	-				ns		
Horizontal	Cycle period	th	13.1	13.3	19.2	μ s	-	
			848	860	1,156	CLK		
	Display period	thd	800			CLK	-	
Vertical	Cycle period	1/tv	59	60	61	Hz	-	
		tv	1,206	1,250	-	H		
	Display period	tvd	1,200			H	-	
DE, DATA	Setup time	-	See the data sheet of LVDS transmitter.			ns	-	
	Hold time	-				ns		
	Rise, fall	-				ns		

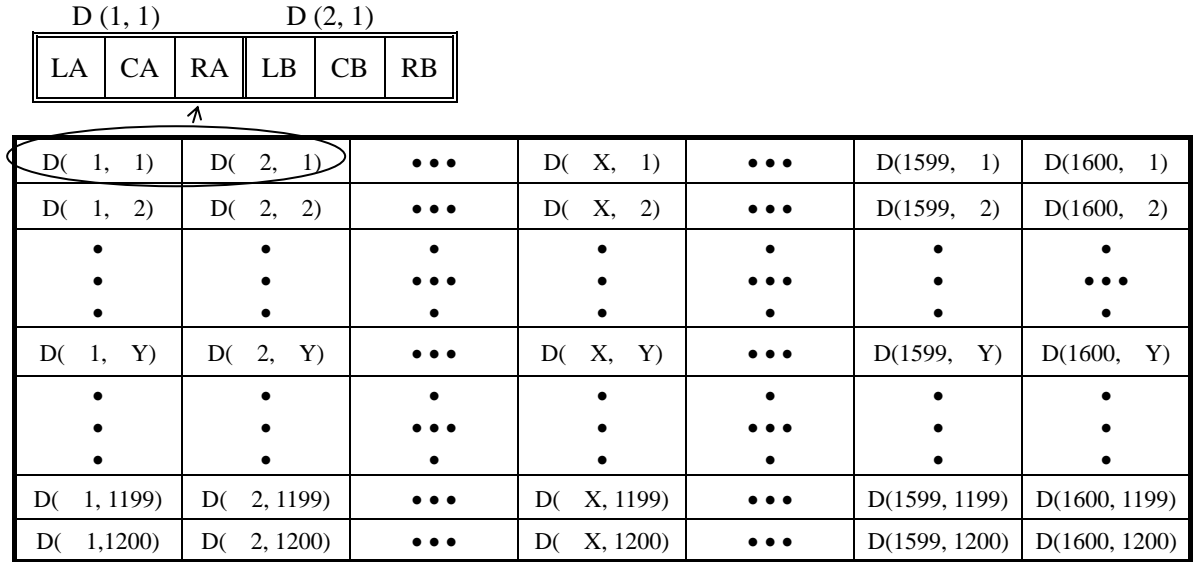
☆

4.8.2 Input signal timing chart



4.9 DISPLAY POSITIONS

Odd pixel: LA= Left data Even pixel: LB= Left data
 CA= Center data CB= Center data
 RA= Right data RB= Right data



4.10 TEN-bit LOOK UP TABLE FOR GAMMA ADJUSTMENT

Adjustment of gamma characteristics for each 8-bit LCR data is possible by using built-in 10-bit LUT (look up table) for Gamma characteristics.

The LUT is set with the serial data. The combination of the control command determines the R/W actions.: READ, Random/Sequential Address WRITE and Individual/Simultaneous LCR setting.

The serial data is composed as Table1.

Table1: Serial data Composition

DATA	DATA name	Function	Remarks
D31	CMD5	Control Command	See Table2 and 3.
D30	CMD4	Control Command	
D29	CMD3	Control Command	
D28	CMD2	Control Command	
D27	CMD1	Control Command	
D26	CMD0	Control Command	
D25	ADD9	LUT Address (MSB)	See Table4.
D24	ADD8	LUT Address	
D23	ADD7	LUT Address	
D22	ADD6	LUT Address	
D21	ADD5	LUT Address	
D20	ADD4	LUT Address	
D19	ADD3	LUT Address	
D18	ADD2	LUT Address	
D17	ADD1	LUT Address	
D16	ADD0	LUT Address (LSB)	See Table5.
D15	Dummy	Dummy Data "0"	
D14	Dummy	Dummy Data "0"	
D13	Dummy	Dummy Data "0"	
D12	Dummy	Dummy Data "0"	
D11	Dummy	Dummy Data "0"	
D10	Dummy	Dummy Data "0"	
D9	DATA9	LUT Data (MSB)	
D8	DATA8	LUT Data	
D7	DATA7	LUT Data	
D6	DATA6	LUT Data	
D5	DATA5	LUT Data	
D4	DATA4	LUT Data	
D3	DATA3	LUT Data	
D2	DATA2	LUT Data	
D1	DATA1	LUT Data	
D0	DATA0	LUT Data (LSB)	

Table2: Command table (CMD5 to CMD0: 6-bit)

DATA name	Parameter	Remarks
CMD5	Selection of WRITE/READ mode "1": WRITE mode "0": READ mode	In case of "0", must be set as follows. CMD4: "1", CMD3: "0", CMD2: "1" CMD1: "0", CMD0: "0"
CMD4	Must be set to "1".	-
CMD3	Selection of Random/Sequential Address WRITE "1": Random Address WRITE "0": Sequential Address WRITE	-
CMD2	Must be set to "1".	-
CMD1	Selection of Individual/Simultaneous LCR setting "1": Individual LCR setting "0": Simultaneous LCR setting	"1": Select the sub-pixel by using ADD9 and ADD8. (See Table4.) "0": ADD9 and ADD8 are invalid.
CMD0	Must be set to "0".	-

Table3: Command Combination table (CMD5 to CMD0: 6-bit)

CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	Mode
1	1	1	1	1	0	Random Address WRITE, Individual LCR setting
1	1	1	1	0	0	Random Address WRITE, Simultaneous LCR setting
1	1	0	1	1	0	Sequential Address WRITE, Individual LCR setting
1	1	0	1	0	0	Sequential Address WRITE, Simultaneous LCR setting
0	1	0	1	0	0	READ mode

*Other combinations are prohibited, and may cause function error.

Table4: Address table (ADD9 to ADD0: 10-bit)

DATA name	Parameter	Remarks
ADD9	Sub-pixel selection ADD[9:8]= 0:0 Left sub-pixel 0:1 Center sub-pixel 1:0 Right sub-pixel 1:1 ON/OFF selection of Gamma Correction	When "ADD[9:8]=1:1", ON/OFF of Gamma correction can select according to the GMA[2:0]. (See Table6 and Table7.)
ADD8		
ADD7		
ADD6		
ADD5	LUT Address 256 address = 00h - FFh	When ADD[9:8] = 1:1, ADD[7:0] must be set to 00h.
ADD4		
ADD3		
ADD2		
ADD1		
ADD0		

Table5: Data table (DATA15 to DATA0: 16-bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	DATA9	[MSB]	-
DATA8	DATA8	10-bit LUT Data 000h - 3FFh	
DATA7	DATA7		
DATA6	DATA6		
DATA5	DATA5		
DATA4	DATA4		
DATA3	DATA3		
DATA2	DATA2		
DATA1	DATA1		
DATA0	DATA0	[LSB]	

Table6: Gamma correction table (DATA15 to DATA0: 16bit)

DATA	DATA name	Parameter	Remarks
DATA15	Dummy	Dummy Data Must be set to "0".	-
DATA14	Dummy		
DATA13	Dummy		
DATA12	Dummy		
DATA11	Dummy		
DATA10	Dummy		
DATA9	Dummy		
DATA8	Dummy		
DATA7	Dummy		
DATA6	Dummy		
DATA5	Dummy		
DATA4	Dummy		
DATA3	Dummy		
DATA2	GMA2	[MSB]	See Table7.
DATA1	GMA1	GMA Data	
DATA0	GMA0	[LSB]	

Table7: Control code GMA[2:0]

GMA2	GMA1	GMA0	Function
0	0	0	No correction (Initial setting)
0	0	1	Correction according to the LUT Data. Note1

*Other combinations are prohibited, and may cause function error.

Note1: Initial setting of the LUT is undefined data. The LUT should be enabled by setting of the GMA after writing the LUT data in all the 256 addresses, in order to avoid undefined data display.

Note2: Transfer the data every power-on, because the LUT data isn't stored in the LCD module.

Note3: As writing and reading the LUT data, a noise may appear on the display image. In order to prevent the noise appearing on the display, following measures should be performed.

(1) The LUT data should be rewritten during invalid period of pixel data (See "4.8 INPUT SIGNAL TIMINGS").

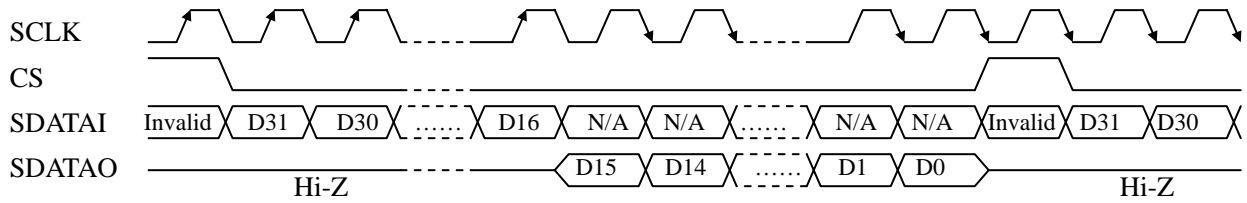
(2) The LUT data should be rewritten when the Gamma Correction is OFF (GMA[2:0] = 000).



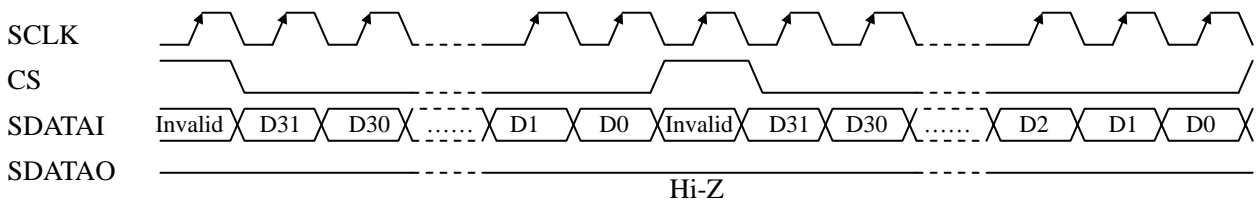
4.11 LUT SERIAL COMMUNICATION TIMINGS

4.11.1 Timing Chart

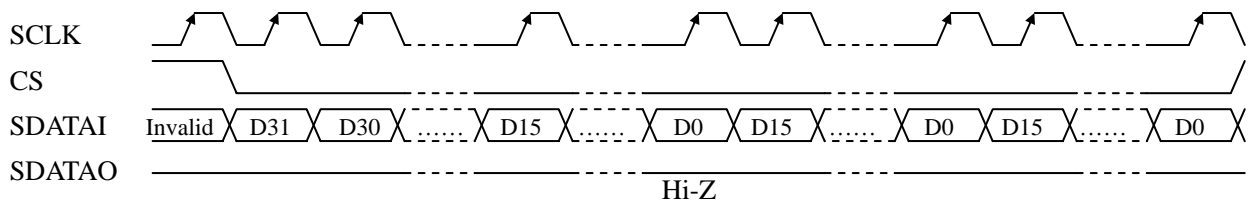
(1) READ Timing Chart



(2) Random Address WRITE Timing Chart



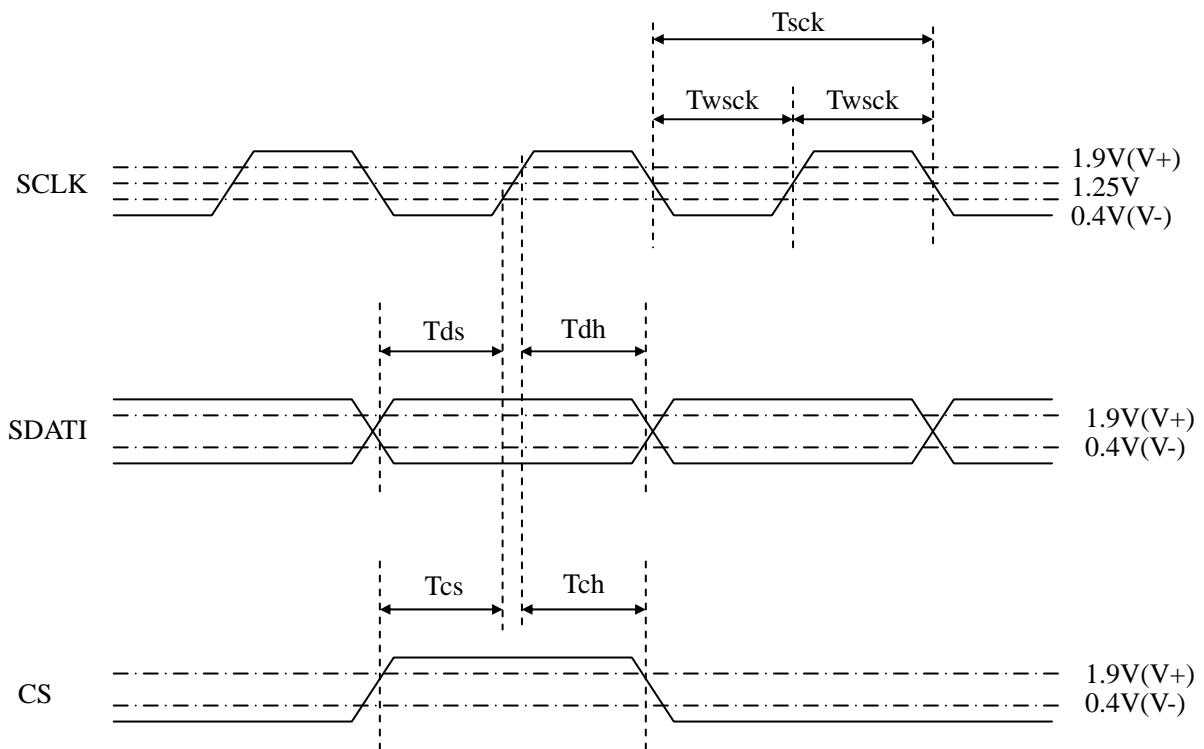
(3) Sequential Address WRITE Timing Chart



4.11.2 Timing specifications

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
SCLK Frequency	1/Tsck	-	-	5	MHz	-
SCLK Pulse Width (WRITE)	Twsck	50	-	-	ns	-
SCLK Pulse Width (READ)	Twsck	5	-	-	tc	Note1
SDATI-SCLK Setup Time	Tds	50	-	-	ns	-
SDATI-SCLK Hold Time	Tdh	50	-	-	ns	-
CS-SCLK Setup Time	Tcs	50	-	-	ns	-
CS-SCLK Hold Time	Tch	50	-	-	ns	-

Note1: At the READ of the serial communication mode, the SCLK Pulse Width (Twsck) must be greater than 5CLK (5 tc's). (See "4.8.1 Timing characteristics".)



Note2: During the serial communication mode, the display noise may appear because of rewriting the data. To avoid this, rewrite the LUT data when the pixel data is invalid or the Gamma Correction is OFF (GMA[2:0] = 000). The external noise may cause the data change, refresh the data regularly according to need.

4.12 OPTICS

4.12.1 Optical characteristics

(1) NL160120BM27-03

(Note1, Note2)

Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	700	1,000	-	cd/m ²	BM-5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	400	700	-	-	BM-5A or SR-3	Note3	
Luminance uniformity	White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.2	1.3	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	-	0.255	-	-	SR-3	Note5
		y coordinate	Wy	-	0.310	-	-		
Response time	Black to White	Ton	-	17	25	ms	BM-5A	Note6 Note7	
	White to Black	Toff	-	18	25	ms			
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θR	70	85	-	BM-5A	Note8	
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θL	70	85	-			
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θU	70	85	-			
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θD	70	85	-			

(2) NL160120BM27-03A

(Note1, Note2)

Parameter	Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks	
Luminance	White at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	L	700	1,000	-	cd/m ²	BM-5A or SR-3	-	
Contrast ratio	White/Black at center $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	CR	400	700	-	-	BM-5A or SR-3	Note3	
Luminance uniformity	White $\theta R = 0^\circ, \theta L = 0^\circ, \theta U = 0^\circ, \theta D = 0^\circ$	LU	-	1.2	1.3	-	BM-5A	Note4	
Chromaticity	White	x coordinate	Wx	-	0.280	-	-	SR-3	Note5
		y coordinate	Wy	-	0.304	-	-		
Response time	Black to White	Ton	-	17	25	ms	BM-5A	Note6 Note7	
	White to Black	Toff	-	18	25	ms			
Viewing angle	Right	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θR	70	85	-	BM-5A	Note8	
	Left	$\theta U = 0^\circ, \theta D = 0^\circ, CR \geq 10$	θL	70	85	-			
	Up	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θU	70	85	-			
	Down	$\theta R = 0^\circ, \theta L = 0^\circ, CR \geq 10$	θD	70	85	-			

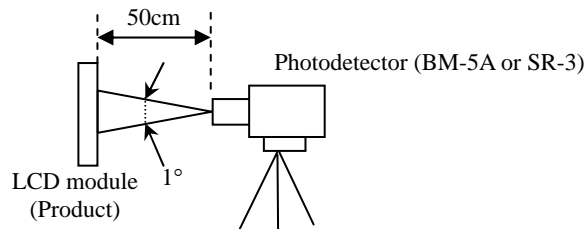
Note1: These are initial characteristics.

Note2: Measurement conditions are as follows.

Ta = 25°C, VDD = 12V, IBL = 6.0 mArms/lamp, Display mode: UXGA,

Horizontal cycle = 1/75.19kHz, Vertical cycle = 1/60.0Hz

Optical characteristics are measured after 20 minutes from working the product, in the dark room. Also measurement methods are as follows.



Note3: See "**4.12.2 Definition of contrast ratio**".

Note4: See "**4.12.3 Definition of luminance uniformity**".

Note5: These coordinates are found on CIE 1931 chromaticity diagram.

Note6: Product surface temperature: TopF = 35°C

Note7: See "**4.12.4 Definition of response times**".

Note8: See "**4.12.5 Definition of viewing angles**".

4.12.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

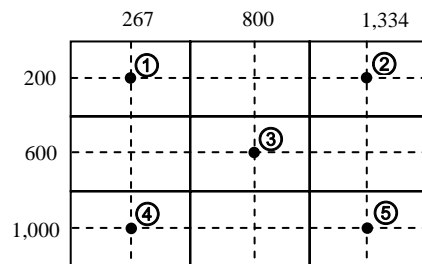
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.12.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

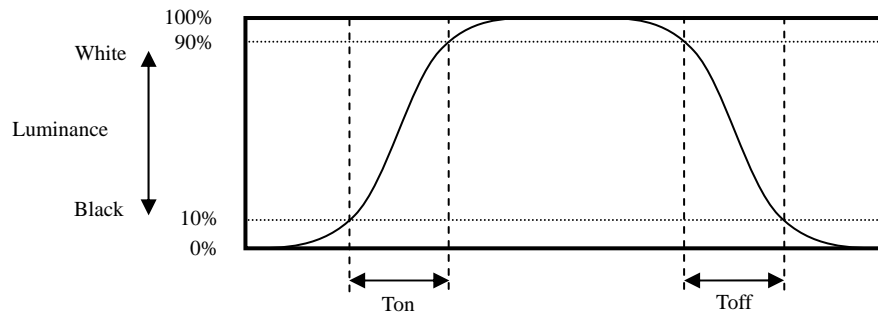
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

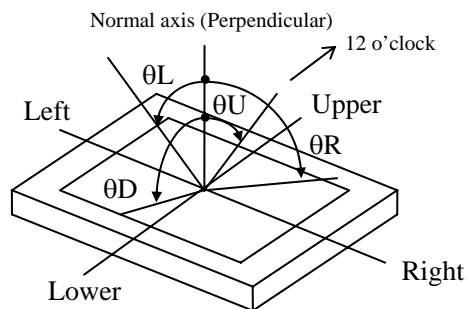


4.12.4 Definition of response times

Response time is measured, the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).



4.12.5 Definition of viewing angles

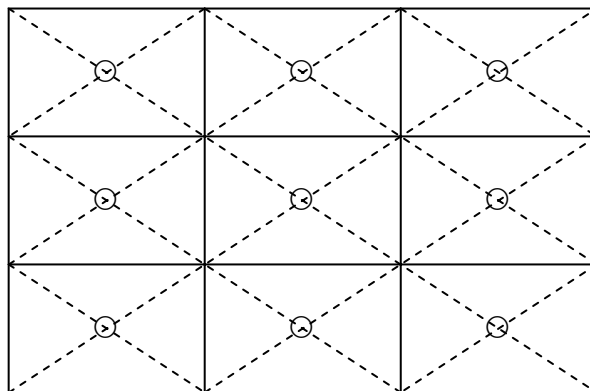


5. RELIABILITY TESTS

Test item	Condition	Judgment Note1
High temperature and humidity (Operation)	① 60 ± 2°C, RH = 60%, 240hours ② Display data is white.	No display malfunctions
Heat cycle (Operation)	① 0 ± 3°C...1hour 55 ± 3°C...1hour ② 50cycles, 4hours/cycle ③ Display data is white.	
Thermal shock (Non operation)	① -20 ± 3°C...30minutes 60 ± 3°C...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)	① 5 to 100Hz, 11.76m/s ² ② 1 minute/cycle ③ X, Y, Z direction ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)	① 294m/s ² , 11ms ② X, Y, Z direction ③ 3 times each directions	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions
Dust (Operation)	① Sample dust: No.15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Low pressure	Non-operation	No display malfunctions
	Operation	
	① 15 kPa (Equivalent to altitude 13,600m) ② -20°C±3°C...24 hours ③ +60°C±3°C...24 hours	
	① 53.3 kPa (Equivalent to altitude 4,850m) ② 0°C±3°C...24 hours ③ +55°C±3°C...24 hours	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.




Note2: See the following figure for discharge points



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS


The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS" and "6.3 ATTENTIONS", after understanding these contents!**

	This sign has the meaning that customer will be injured by himself or the product will sustain a damage, if customer has wrong operations.
	This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.
	This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS



*** Do not touch the working backlight. There is a danger of an electric shock.**



*** Do not touch the working backlight. There is a danger of burn injury.**
*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s² and to be not greater 11ms, Pressure: To be not greater 19.6N (φ16mm jig))**

6.3 ATTENTIONS 

6.3.1 Handling of the product

- ① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
- ② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
- ③ When the product is put on the table temporarily, display surface must be placed downward.
- ④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
- ⑤ The torque for product mounting screws must never exceed 0.735 N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 5.3mm.
- ⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
- ⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, use of the cloth with ethanolic liquid such as screen cleaner for LCD is recommended.

- ⑧ Do not push nor pull the interface connectors while the product is working.
- ⑨ Do not bend or unbend the lamp cable at the near part of the lamp holding rubber, to avoid the damage for high voltage side of the lamp.
- ⑩ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.

6.3.2 Environment

- ① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
- ② In order to prevent dew condensation occurring by temperature difference, the product packing box should be opened after enough time being left under the environment of an unpacking room. Evaluate the leaving time sufficiently because a situation of dew condensation occurring is changed by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with packing state)
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ This product is not designed as radiation hardened.

6.3.3 Characteristics

The following items are neither defects nor failures.

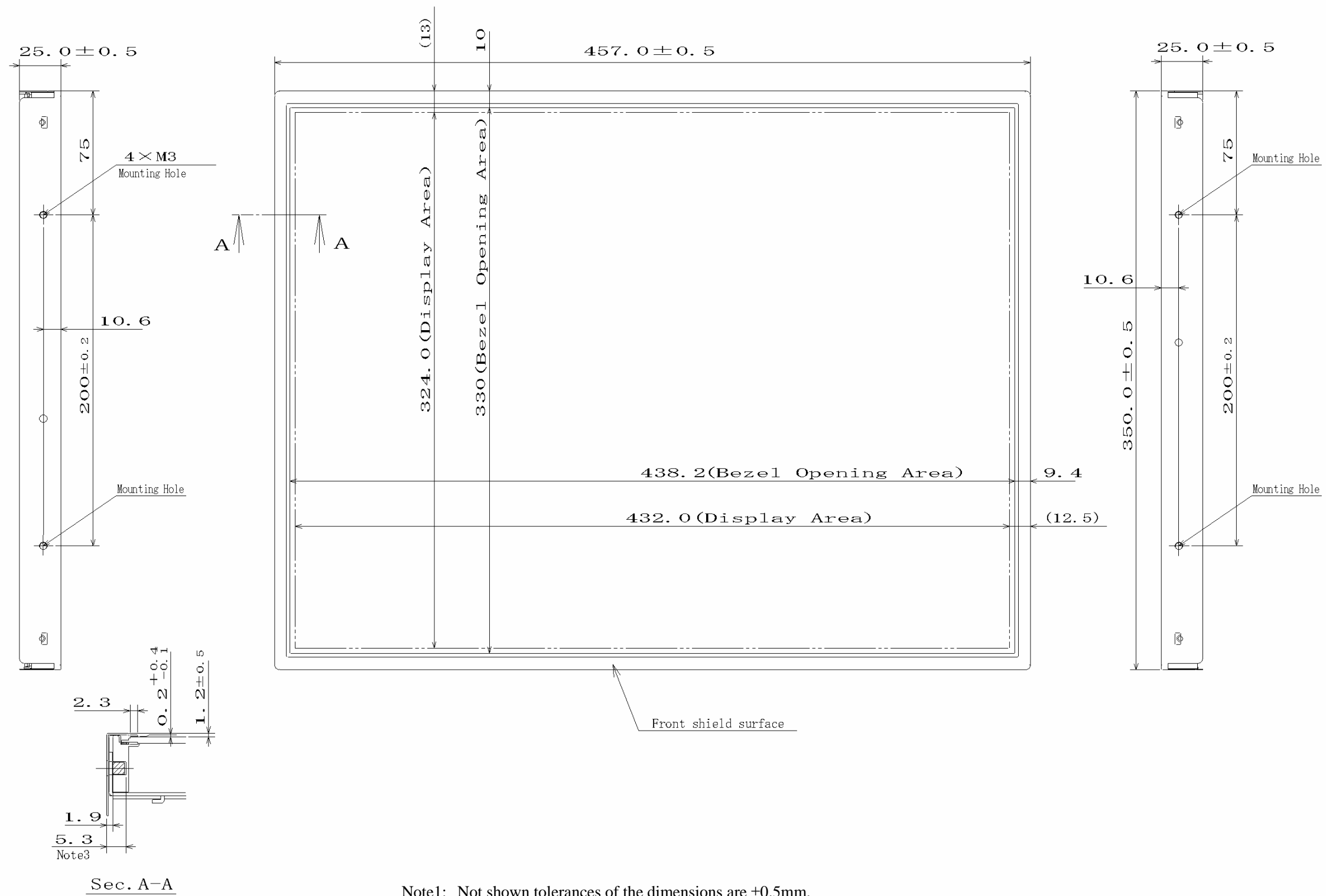
- ① Response time, luminance and color may be changed by ambient temperature.
- ② Display mura, flicker, vertical seam or small spot may be observed depending on display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
- ⑥ Optical characteristics may be changed depending on input signal timings.
- ⑦ The interference noise between input signal frequency for this product's signal processing board and luminance control frequency of the inverter may appear on a display. Set up luminance control frequency of the inverter so that the interference noise does not appear.

6.3.4 Other

- ① All VDD and GND terminals should be used without any non-connected lines.
- ② Do not disassemble a product or adjust variable resistors.
- ③ See "REPLACEMENT MANUAL FOR BACKLIGHT UNIT", when replacing backlight lamps.
- ④ Pack the product with original shipping package, in order to avoid any damages during transportation, when returning the product to NEC for repair and so on.
- ⑤ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

7. OUTLINE DRAWINGS

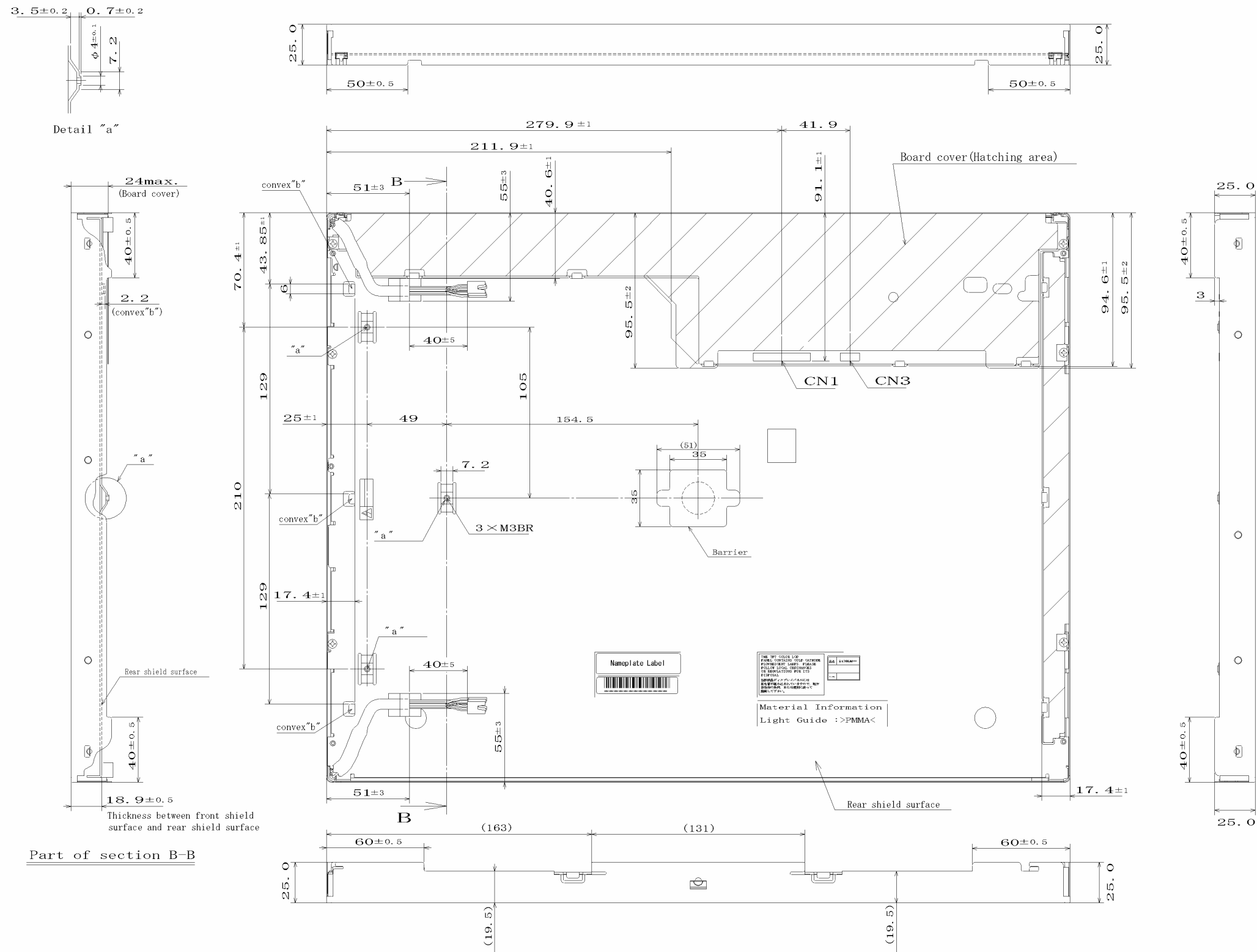
7.1 FRONT VIEW



- Note1: Not shown tolerances of the dimensions are ±0.5mm.
- Note2: The torque for product mounting screws must never exceed 0.735N·m.
- Note3: The length of product mounting screws from surface of plate must be ≤ 5.3mm.
- Note4: The values in parentheses are for reference.

Unit: mm

7.2 REAR VIEW



- Note1: Not shown tolerances of the dimensions are ±0.5mm.
- Note2: The torque for product mounting screws must never exceed 0.735N·m.
- Note3: The values in parentheses are for reference.

Unit: mm