TFT COLOR LCD MODULE

Type: NL128102AC31-02A
51cm (20.1 Type), SXGA

SPECIFICATIONS

First Edition

PRELIMINARY

This document is preliminary. All information in this document are subject to change without prior notice.

NEC Corporation NEC Electron Devices Display Device Operations Unit Color LCD Division Application Engineering Department		
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Prepared		August 8, 2000

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Application examples recommended by NEC Corporation.

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Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, or any other equipment for which specifically high standard of quality or reliability is required.

CONTENTS

1. DESCRIPTION

NL128102AC31-02A is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL128102AC28-02A has a built-in backlight with an inverter.

The 51cm(20.1 Type) diagonal display area contains 1280×1024 pixels and can display 16,777,216 colors. Also, it has wide viewing angle and multi-scan function.

NL128102AC31-02A is a model that mounted the CRT (Analog RGB) and TMDS interface board on NL128102AC31-02.

2. FEATURES

- Ultra-wide viewing angle (with lateral electric field)
- TMDS interface (adapted for SiI161A Silicon Image, Inc. as a receiver)
- CRT interface
  - Auto recognition of input signal (analog RGB signals, synchronous signals (Hsync, Vsync, Composite, Sync on green))
  - Digital control (with on screen display*):
    e.g., Language select, Brightness adjust, Contrast adjust, Display position adjust and Gamma adjust.
  - Corresponding to DDC1/2B (analog) and DDC2B (digital)
  - Corresponding to VESA DPMS
  - Auto adjust (clock and display position)
  - Free supply voltage sequence
  - Multi-scan function: e.g., SXGA, XGA, SVGA, VGA, VGA-TEXT, MAC, SUN
- High luminance (Typ. 250cd/m^2)
- High contrast (Typ. 250:1)
- Wide color gamut (Typ. 60%, at center, to NTSC)
- Incorporated direct type backlight (twelve lamps, Inverter)
- Backlight unit replaceable (part No.: 201LHS02)
- Inverter replaceable (part No.: 201PW021)

＊On Screen Display
Application with the OSD function might conflict with patents in Europe and/or the U.S.A.
If you apply the OSD function appreciate the patents at your side.

VESA:	Video Electronics Standards Association
DPMS:	Display Power Management Signaling
DDC1:	Display Data Channel 1
DDC2B:	Display Data Channel 2B

3. APPLICATIONS

- Desk-top type of PCs, Engineering work stations
- Display terminals for control system
- Monitors

4. STRUCTURE AND FUNCTIONS

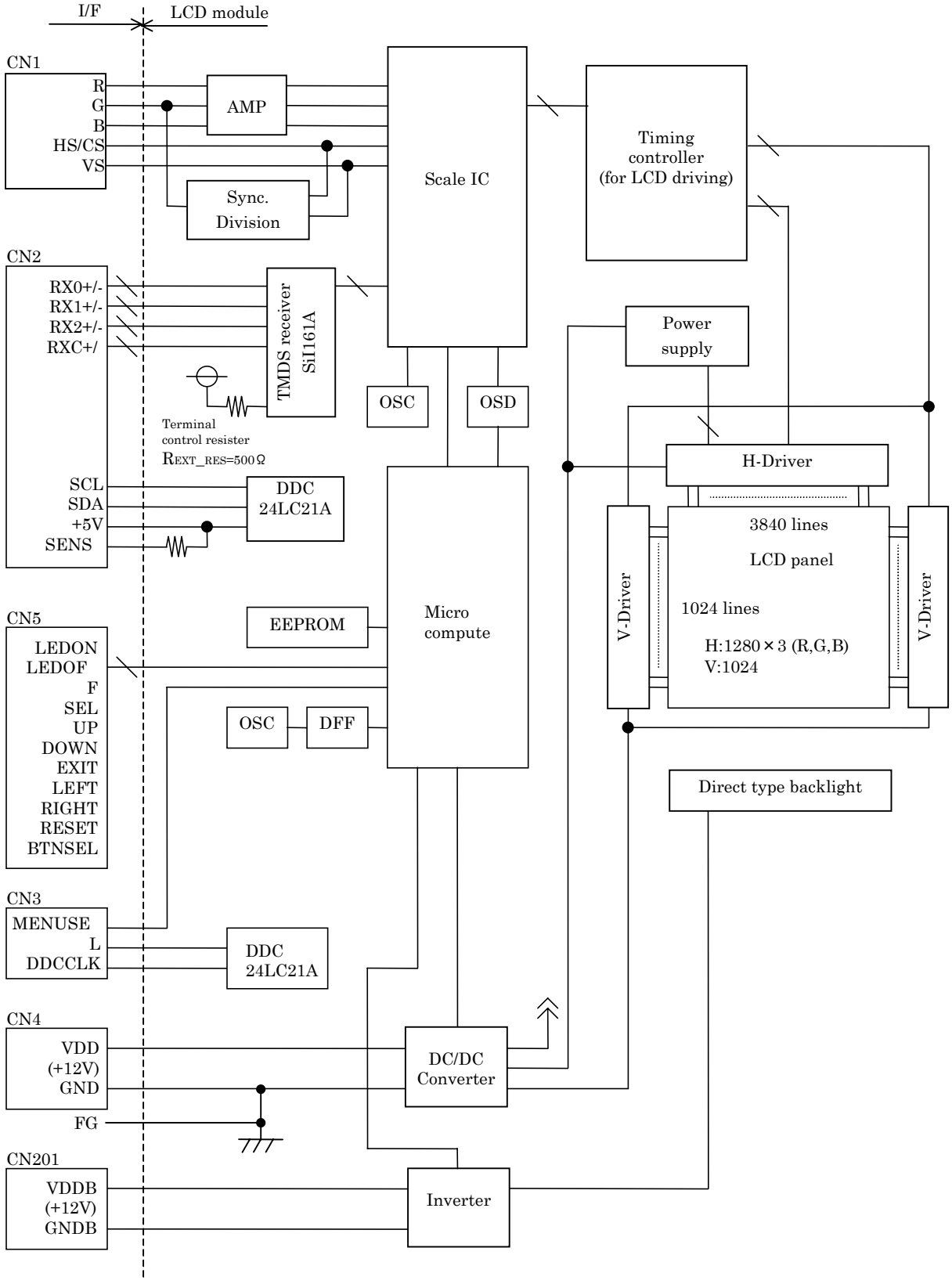
A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between TFT array and color filter glass substrates. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cell. Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

5. OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	399.36 (H)×319.49 (V) mm
Drive system	a-Si TFT active matrix
Display colors	16,777,216
Number of pixels	1280×1024
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.312 (H)×0.312 (V)mm
Module size	470.0 (H, Typ.)×382.0 (V, Typ.)×42.5 (D, Max.) mm
Weight	2380 g (Typ.)
Contrast ratio	250:1 (Typ.)
Viewing angle (more than the contrast ratio of 10:1)	Horizontal: 85 ° (Typ. , left side, right side) Vertical: 85 ° (Typ. , up side, down side)
Designed viewing direction	Optimum grayscale (γ =2.2): Perpendicular
Polarizer Pencil-hardness	3 H (Min., at JIS K5400)
Color gamut	60 %(Typ., At center, To NTSC)
Response time	25 ms (Typ.), " Black" to " White" (0%→90%)
Luminance	250 cd/m^2 (Typ.)
Signal system	・Analog RGB signals, Synchronous signals (Vsync and Hsync or Composite) ・2 port TMDS interface (Receiver: SiI161A×1pcs, Silicon Image, Inc.) RGB 8-bit signals, Synchronous signals (Hsync, Vsync), DE encoded with (SiI160 Silicon Image, Inc.) are preferable.
Supply voltage	12V (Logic, LCD driving) , 12V (Backlight)
Backlight	Direct light type: Twelve cold cathode fluorescent lamps with an inverter 【Replaceable parts】 ・Lamps holder: 201LHS02 ・Inverter: 201PW021
Power consumption	50 W(Typ.)

6. BLOCK DIAGRAM



Note 1: GND (signal ground) is connected to FG (frame ground) in the LCD module and neither GND nor FG are connected to GNDB (backlight ground). These grounds should be connected to system ground in customer equipment.

7. SPECIFICATIONS

7.1 GENERAL SPECIFICATIONS

Items	Contents	Units
Module size	470.0±1.0 (H)×382.0±1.0 (V)×42.5 Max.(D)	mm
Display area	399.36 (H)×319.49 (V) 【Diagonal display area: 51cm (Type 20.1)】	mm
Number of pixels	1280 (H)×1024 (V)	pixel
Pixel pitch	0.312 (H)×0.312 (V)	mm
Dot pitch	0.104 (H)×0.312 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	―
Display colors	16,777,216 (RGB, 8bit)	color
Weight	2380 (Typ.), 2490 (Max.)	g

7.2 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbols	Ratings	Units	Remarks
Supply voltage	VDD	-0.3 to +14.0	V	Ta = 25℃
	VDDB	-0.3 to +14.0	V	
Logic input voltage (LCD)	Vin1	-0.3 to 3.6	V	Ta = 25℃ VDD=12V
Logic input voltage (backlight-BRTC signal)	Vin2	-0.3 to +5.5	V	Ta = 25℃ VDDB=12V
Logic input voltage (backlight-BRTL signal)	Vin3	-0.3 to +1.5	V	
Storage temperature	Tst	-20 to +60	℃	―
Operating temperature	Top	0 to +55	℃	Module surface Note 1
Relative humidity (RH)	Note 2	≤ 95	%	Ta≤40℃
		≤ 85	%	40℃＜Ta≤50℃
		≤ 70	%	50℃＜Ta≤55℃
Absolute humidity	Note 2	Absolute humidity shall not exceed Ta=55℃, RH=70% level.	g/m^3	Ta＞55℃

Note 1: Measured at the display area (including self-heat)
Note 2: No condensation

7.3 ELECTRICAL CHARACTERISTICS

(1) Logic, LCD driving

Ta＝25℃

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Supply voltage	VDD	10.8	12.0	13.2	V	－
Ripple voltage	VRP	－	－	100	mV	for VDD
Logic input “L” voltage	ViL	0	－	0.8	V	TTL level
Logic input “H” voltage	ViH	2.0	－	5.25	V	
Logic output “L” voltage	VoL	－	－	0.4	V	DDCDAT, SDA
Logic output “H” voltage	VoH	2.4	－	－	V	
TMDS differential input amplitude	VID	TBD	500	TBD	mV	TMDS differential input signal
TMDS terminal resistor Note 1	RT	－	500	－	Ω	－
Analog RGB signals maximum amplitude (white - black)	VIRGB	0	0.7	0.9	Vp-p	－
Analog RGB signals DC input level	VIdcRGB	-0.5	－	2.5	V	－
Sync level	VIS	0.2	0.3	0.6	Vp-p	G terminal (sync on green)
Supply current	IDD	－	670 Note 2	1500 Note 3	mA	VDD=12.0V
		－	TBD Note 2	TBD Note 3	mA	Power saving mode VDD=12.0V

Note 1: Terminal control resistor (R_{EXT_RES}) of TMDS receiver is 500Ω (settlement).

Note 2: Checker flag pattern (in EIAJ ED-2522)

Note 3: Theoretical maximum current pattern

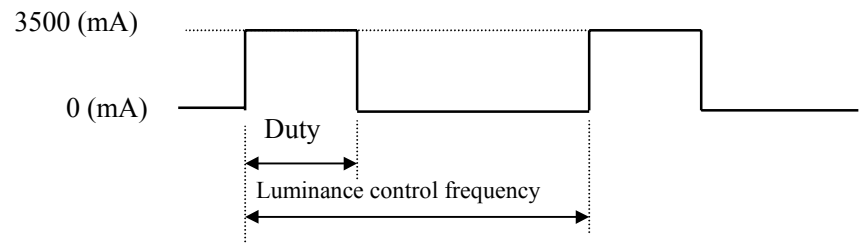
(2) Backlight

Ta = 25℃

Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
Supply voltage	VDDB	10.8	12.0	13.2	V	Back light power supply
Logic input “L” current 1	IiL1	-1.6	－	－	mA	for BRTP
Logic input “H” current 1	IiH1	－	－	3.5	mA	
Logic input “L” current 2	IiL2	-610	－	－	μA	for BRTC, PWSEL
Logic input “H” current 2	IiH2	－	－	440	μA	
Supply current	IDDB	－	3500 Note 1	4200	mA	VDDB=12.0V (at Max. luminance)

Note 1: Display color is white.

(3) Inverter current wave



Maximum luminance control : 100%

Minimum luminance control : 20%

Luminance control frequency ≒ Input Vsync frequency×K

Vsync frequency ≦ 75Hz: K= 4.6

Vsync frequency ＞ 75Hz: K= 3.6

7.4. SUPPLY VOLTAGE SEQUENCE

(1) Analog RGB input signals

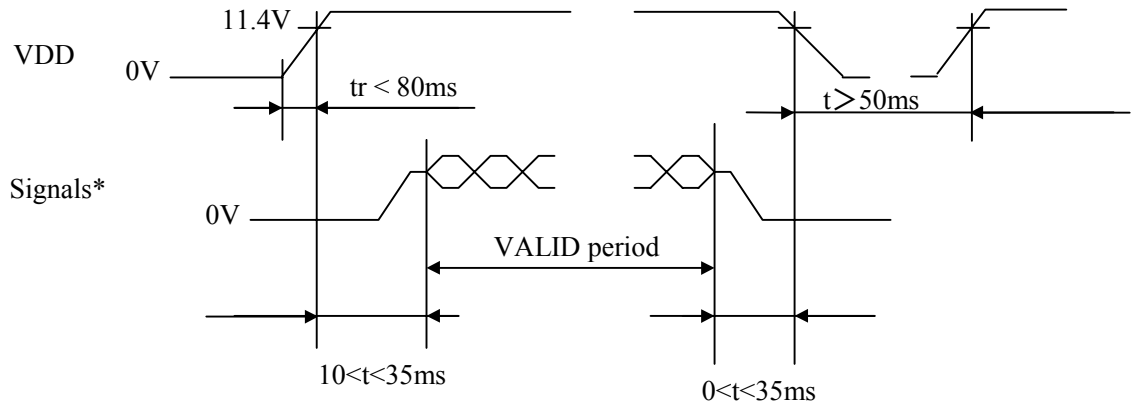
① 12V for backlight should be started up within 800ms, otherwise, the protection circuit makes the backlight turns off.

② Please note that the supply voltage must not be applied while the control signals (SEL, UP, DOWN, EXIT, LEFT, RIGHT, RESET and ADTSEL) are connected to GND. Otherwise the module may cause malfunction.

③ If the power supply voltage is applied while UP and DOWN are connected to GND, the input control signals become ineffective mode. To reset this mode, turn off the power once and turn on the power while UP and DOWN are connected to GND. Then, the mode will be released.

④ Do not change MENUSEL and BTNSEL setting while the module is operated.
MENUSEL and BTNSEL selection is set when the power supply voltage is applied.

(2) TMDS input signals



＊The value of signals are in terminal of resistor 50Ω.

Note 1: Logic signals (synchronous signals and control signals) must be “0” voltage (V), when VDD is not input. If input voltage to signal lines is higher than 0.3 V, the internal circuit will be damaged.
Note 2: The supply voltage for input signals should be the same as VDD.
Note 3: The backlight ON/OFF (BRTC signal) should be controlled while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON with no logic signals
Note 4: The backlight is turned off with safety circuit, when “L” period of BRTP signal is input more than 50 ms or 12V for backlight is started up more than 800ms.
Note 5: Do not input “H” to PWSEL, when VDDB is 0V or BRTC is “L”.
Note 6: Wrong power sequence may damage the module.

(3) Fuse

This LCD module uses fuses as follows.

Supply voltage	Part No.	Supplier	Ratings	Remarks
VDD	CCF1NTE3.15	KOA	60VDC/3.15A	—
VDDB	TBD	TBD	TBD	—

Note 1: Before the power is designed, fuses should be considered. The power capacity should be used more than 2.0 times of fuses rating.
When the power capacity is less than 2.0 times of fuses rating, the module must be evaluated enough from safety point of view.

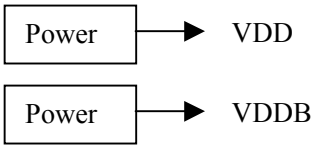
(4) Ripple of supply voltage

Supply voltage	VDD (for logic and LCD driver)	VDDB (for backlight)
Acceptable range	≦ 100mVp-p	≦ 200mVp-p

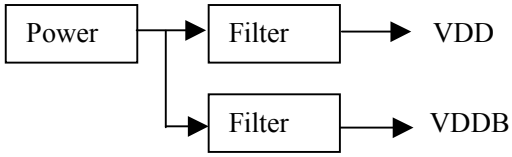
Note 1:The acceptable range of ripple voltage includes spike noise.

Example of the power supply connection

a) Separate the power supply



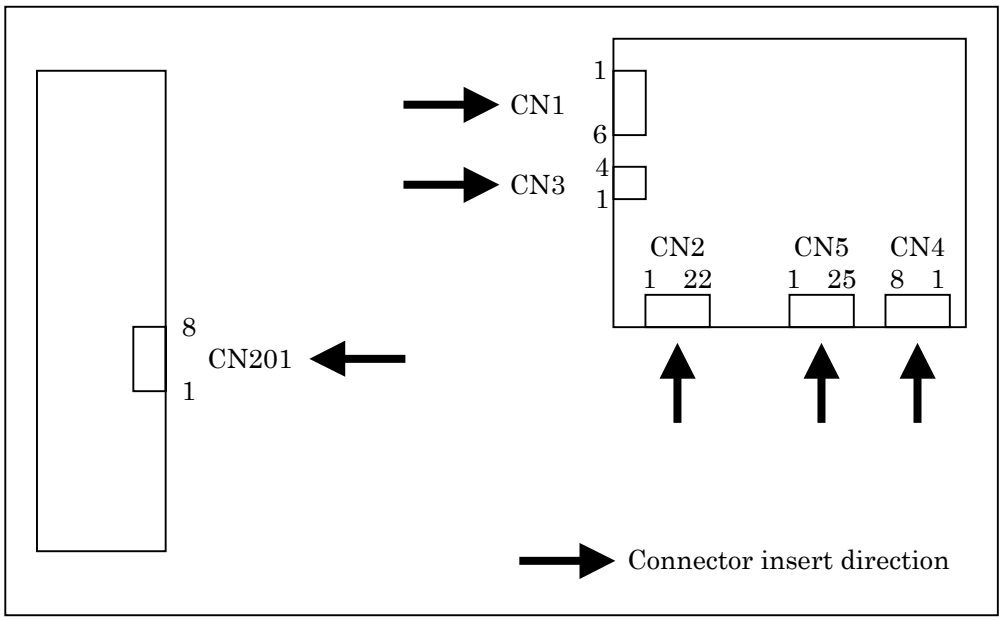
b) Put the filter



7.5 INTERFACE PIN CONNECTIONS

(1) Connectors for power supply and signals

Connector locations



CN1

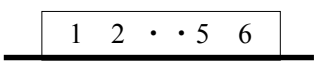
Part No.: MRF03-6R-SMT

Adaptable socket : MRF03-6P-1.27(for cable type) or MRF03-6PR-SMT(for board to board type)

Supplier: HIROSE ELECTRIC CO., LTD.

Pin No.	Symbols	Pin No.	Symbols
1	B	4	Vsync
2	G	5	Hsync/Csync
3	R	6	N.C.

Figure from socket view



Note 1: N.C.(no connection) must be open.

Note 2: A coaxial cable should be connected with GND.

CN2

Part No.: FI-XD7S-HF
Adaptable socket: FI-XD7M(FPC, coaxial type) or FI-XD7H(for cable type)
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	GND	12	RXC-
2	RX2+	13	GND
3	RX2-	14	N.C.
4	GND	15	N.C.
5	RX1+	16	GND
6	RX1-	17	SENSE
7	GND	18	+5V DC
8	RX0+	19	GND
9	RX0-	20	SDA
10	GND	21	SCL
11	RXC+	22	GND

Figure from socket view

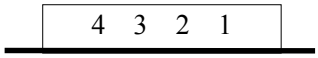
Note 1: N.C.(no connection) must be open.
Note2 : Use 50Ω twist pair wires for the cable.

CN3

Part No. : IL-Z-4PL-SMTY
Adaptable socket: IL-Z-8S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	DDCCLK	3	MENUSEL
2	DDCDAT	4	GND

Figure from socket view



CN4

Part No.: IL-Z-8PL-SMTY
Adaptable socket: IL-Z-8S-S125C3
Supplier: Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbols	Pin No.	Symbols
1	VDD	5	GND
2	VDD	6	GND
3	VDD	7	GND
4	VDD	8	GND

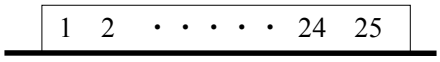
Figure from socket view

CN5

Part No.: DF14A-25P-1.25H
Adaptable socket: DF14-25S-1.25C
Supplier: HIROSE ELECTRIC CO, LTD.

Pin No.	Symbols	Pin No.	Symbols
1	LEDON	14	EXIT
2	LEDOFF	15	GND
3	GND	16	N.C.
4	N.C.	17	GND
5	ADTSEL	18	TEST Note 1
6	RIGHT	19	BTNSEL
7	LEFT	20	N.C.
8	RESET	21	N.C.
9	N.C.	22	N.C.
10	GND	23	GND
11	SEL	24	N.C.
12	UP	25	N.C.
13	DOWN		

Figure from socket view



Note 1: TEST must connect to GND.
Note 2: N.C. (no connection) must be open.

CN201

Part No.: DF-3-8P-2H
Adaptable socket : DF-3-8S-2C
Supplier: HIROSE ELECTRIC CO., LTD.

Pin No.	Symbols	Pin No.	Symbols
1	GNDB	5	VDDB
2	GNDB	6	VDDB
3	GNDB	7	VDDB
4	GNDB	8	VDDB

Figure from socket view

Remark 1: Do not keep pins free (VDD, VDDB, GND, GNDB) to avoid noise issue.
Remark 2: GND (signal ground) is connected to FG (frame ground) in the LCD module and neither GND nor FG are connected to GNDB (backlight ground). These grounds should be connected to system ground in customer equipment.

(2) PIN FUNCTIONS

Symbols	I/O	Logic	Descriptions
R	Input	—	Analog red video signal input（0.7Vp-p, input impedance 75Ω）
G	Input	—	Analog green video signal input, Sync on green input （0.7Vp-p, input impedance 75Ω）
B	Input	—	Analog blue video signal input（0.7Vp-p, input impedance 75Ω）
Hsync/ Csync	Input	Positive Negative	Horizontal synchronous signal input or composite synchronous signal input（TTL level）, Positive / Negative auto recognition
Vsync	Input	Positive Negative	Vertical synchronous signal input（TTL level） Positive / Negative auto recognition, Clock input for DDC1
RX2+	Input	—	TMDS differential data input R (+)
RX2-	Input	—	TMDS differential data input R (-)
RX1+	Input	—	TMDS differential data input G (+)
RX1-	Input	—	TMDS differential data input G (-)
RX0+	Input	—	TMDS differential data input B (+)
RX0-	Input	—	TMDS differential data input B (-)
RXC+	Input	—	TMDS differential clock input (+)
RXC-	Input	—	TMDS differential clock input (-)
+5V DC	—	—	+5V power supply (DDC power supply for digital input)
SENSE	Output	Positive	Connection detective signal
SCL	Input	Positive	Clock for DDC2B (for digital input)
SDA	Input/ Output	Positive	Data for DDC2B (for digital input) read / write
DDCCLK	Input	Positive	Clock for DDC2B (for analog input)
DDCDAT	Input/ Output	Positive	Data for DDC1 / 2B (for analog input) read / write
LEDON	Output	Positive	Indicator for LED power on “H”:LED select, “L”:Other status
LEDOFF	Output	Positive	Indicator for Power save mode “H”:Power mode select, “L”:Other status
SEL	Input	Negative	Control function select signal (TTL level) SEL is pulled up in the module. “H” or “open ”: SEL off, “L” : SEL on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.
UP	Input	Negative	Control signal (TTL level) The signal increases the value of the functions selected. UP is pulled up in the module. “H” or “open ”: UP off, “L” : UP on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.
DOWN	Input	Negative	Control signal (TTL level) The signal decreases the value of the functions selected. DOWN is pulled up in the module. “H” or “open ”: DOWN off, “L” : DOWN on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.
EXIT	Input	Negative	Control function exit signal (TTL level) EXIT is pulled up in the module. “H” or “open ”: EXIT off, “L” : EXIT on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.

Symbols	I/O	Logic	Descriptions
RIGHT Note 1	Input	Negative	Control signal (TTL level) The signal increases the value of the functions selected. RIGHT is pulled up in the module. "H" or "open ": RIGHT off, "L" : RIGHT on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.
LEFT Note 1	Input	Negative	Control signal (TTL level) The signal decreases the value of the functions selected. LEFT is pulled up in the module. "H" or "open ": LEFT off, "L" : LEFT on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.
RESET Note 1	Input	Negative	Control signal (TTL level) RESET is pulled up in the module. "H" or "open ": RESET off, "L" : RESET on Detail of the functions is mentioned in **7.13. CONTROL FUNCTIONS**.
BTNSEL	Input	—	Number of adjust switches select signal (TTL level) BTNSEL is pulled up in the module. "open": 7, "L": 4 Detail of the functions is mentioned in **NUMBER OF ADJUST SWITCHES SELECT**.
TEST	Input	—	Must be connected to GND. TEST is pulled up in the module.
MENUSEL	Input	—	OSD display select signal (TTL level) MENUSEL is pulled up in the module. Detail of the functions is mentioned in **OSD DISPLAY DIRECTION SELECT**.
ADTSEL	Input	—	Analog input / digital input select signal ADTSEL is pulled up in the module. Detail of the functions is mentioned in **INPUT SIGNAL SELECT**.
VDD	—	—	Power supply for Logic and LCD driving +12V（ ±10%）
VDDB	—	—	Power supply for backlight +12V （ ±10%）
GND	—	—	Ground for logic and LCD driving (VDD) Note 2
GNDB	—	—	Ground for backlight power supply (VDDB) Note 2

Note 1: This terminal becomes effective only when the value of BTNSEL is "open".
Detail of the functions is mentioned in NUMBER OF ADJUST SWITCHES SELECT.

Note 2: GND is connected to FG in the LCD module. Neither GND nor FG are connected to GNDB.
These grounds should be connected to system ground in customer equipment.

(3) NUMBER OF ADJUST SWITCHES SELECT

BTNSEL	"L"	"open"
Function	4 (SEL, UP, DOWN and EXIT) number of adjust switch are selected.	7 (SEL, UP, DOWN, RIGHT, LEFT, EXIT and RESET) number of adjust switch are selected.

(4) OSD DISPLAY DIRECTION SELECT

MENUSEL	"L"	"open"
Function	OSD is displayed in normal direction (rotation angle = 0°).	OSD is displayed in left rotation direction. (rotation angle =90°)

(5) INPUT SIGNAL SELECT

Every time ADTSEL is "L", an analog input and digital input are changed.

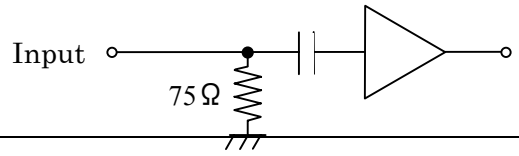
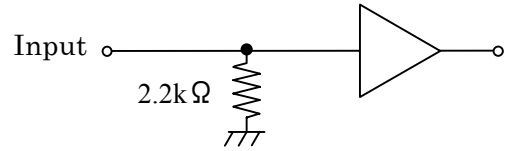
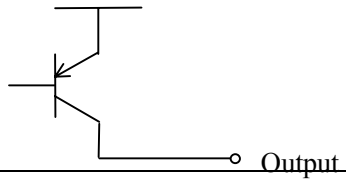
Auto recognition function of input signals works when power supply is input.

Analog input: Detail of the functions is mentioned in **7.6. INPUT SYNCHRONOUS SIGNALS (1)**.

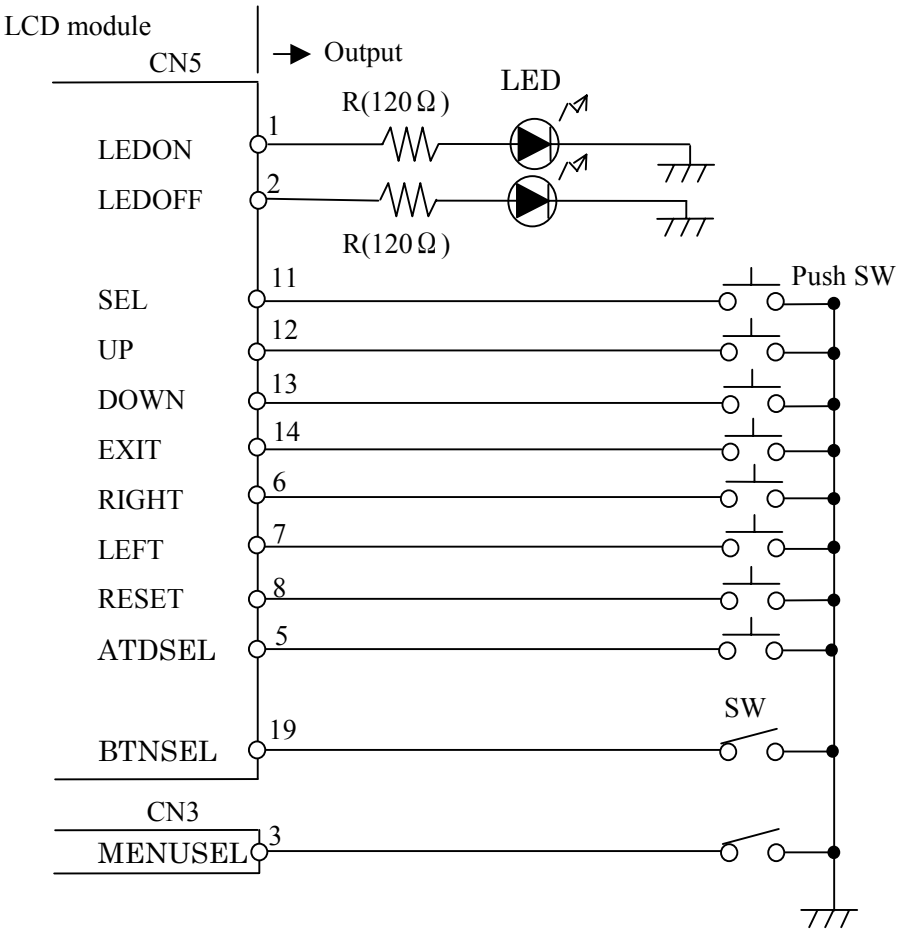
Digital input: Detail of the functions is mentioned in **7.6. INPUT SYNCHRONOUS SIGNALS (2)**.

In case that both the analog signal and the digital signal are input, the analog signal is recognized preferentially.

(6) Equivalent circuit

Symbols	I/O	Equivalent circuit
R,G, B	Input	
Hsync/Csync, Vsync	Input	
LEDON LEDOFF	Output	RN2306(Toshiba) or equivalent 

<Example of LED circuit>



7.6 INPUT SYNCHRONOUS SIGNALS

This module is corresponding to the synchronous signals below.

(1) Analog input

Auto recognition mode	Synchronous signal		
	Hsync/Csync	Vsync	Sync. On Green
Separate synchronous signal mode (Hsync, Vsync)	Input	Input	Input or no input
Composite synchronous mode Note 1	Input (Csync)	No input	Input or no input
Sync on Green mode Note 2	No input	No input	Input
Power save mode	Input (Hsync)	No input	Input or no input
	No input	Input	Input or no input
	No input	No input	No input

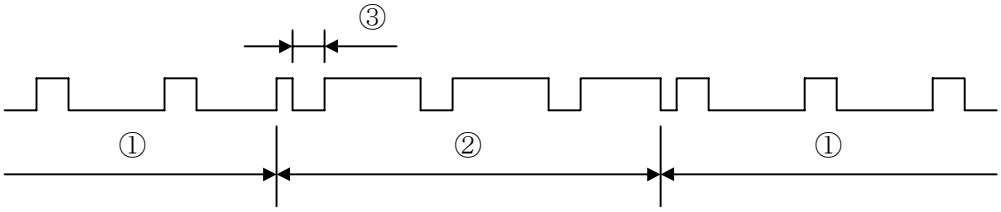
Remark 1: Power save mode corresponds to VESA DPMA.

Note 1: Composite synchronous signals type

(1) Type A

There are Hsync pulses (equivalent) in Vsync period.

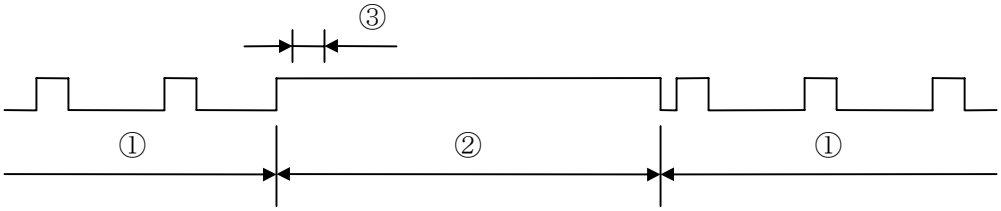
Type A becomes composite synchronous mode.



(2) Type B

There are no Hsync pulses (equivalent) in Vsync period.

Type B becomes power save mode

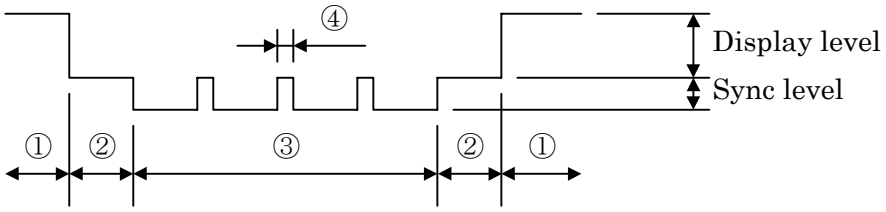


①Non Vsync period ②Vsync period ③Hsync pulse (equivalent)

Note 2: Sync on green signal types

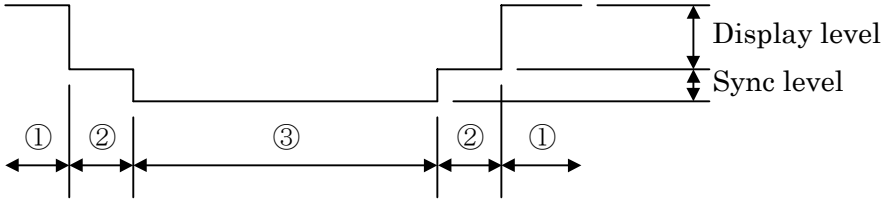
(1) SonG type A

There are Hsync pulses (equivalent) in Vsync period.
Type A becomes composite synchronous mode.



(2) SonG type B

There are no Hsync pulses (equivalent) in Vsync period.
Type B becomes power save mode



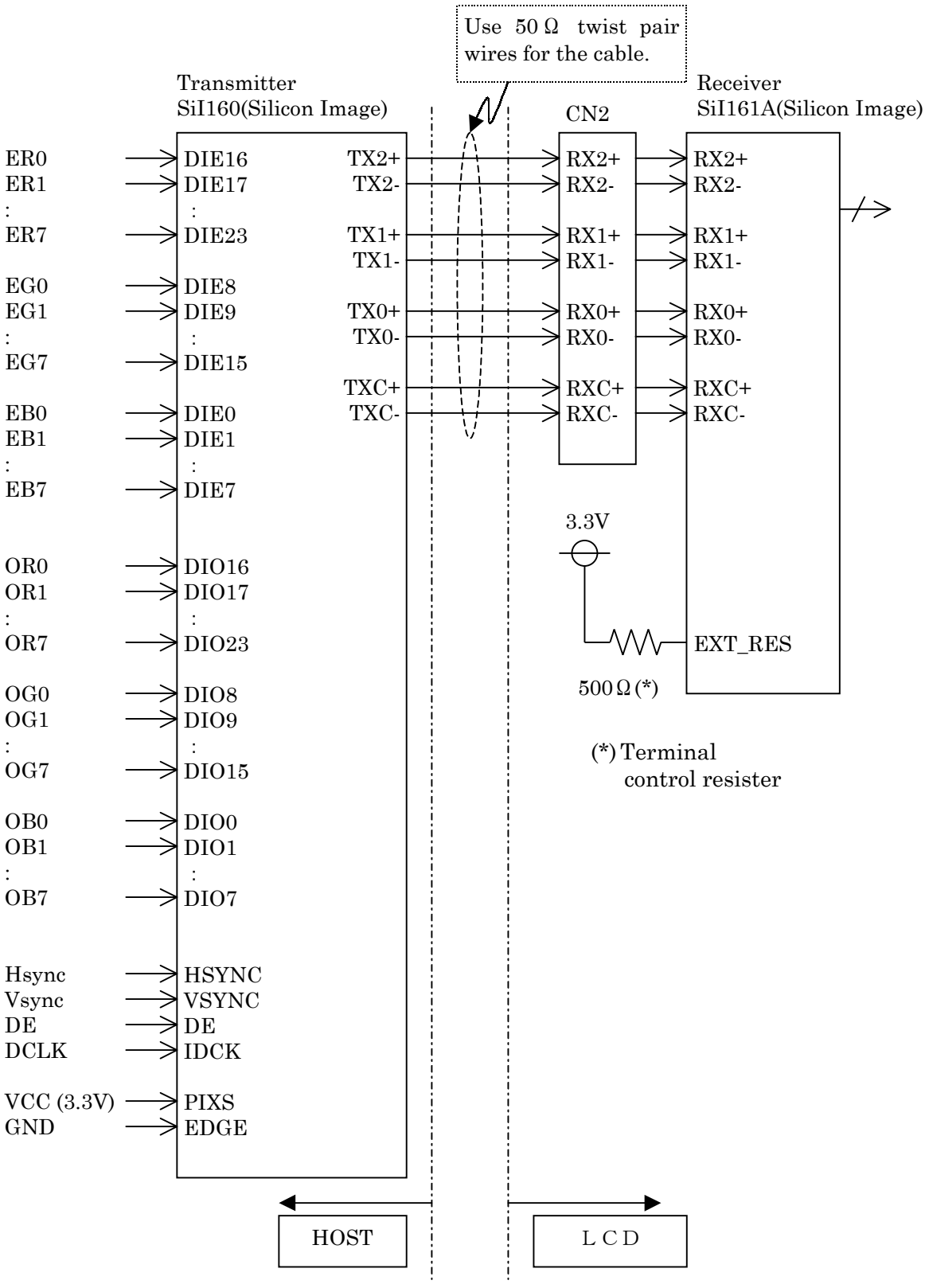
①Display level ②Black level period ③Vsync period ④Hsync pulse (equivalent)

(2) TMDS input

Auto recognition mode	Synchronous signal		
	Hsync	Vsync	DE
Normal mode	Input	Input	Input
	No Input	No input	Input
Power save mode	Input or no input	Input or no input	No input

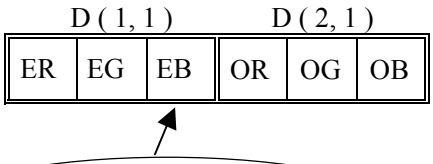
7.7 TMDS interface

(1) Method of connection for Sii160



(2) Display positions of input data

Odd Pixel: ER= R DATA Even Pixel : OR=R DATA
Odd Pixel: EG= G DATA Even Pixel : OG=G DATA
Odd Pixel: EB= B DATA Even Pixel : OB=B DATA



D(0,0)	D(1,0)	•••	D(1279,0)
D(0,1)	D(1,1)	•••	D(1279,1)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(0,1023)	D(1,1023)	•••	D(1279,1023)

(3)TMDS INPUT SIGNAL TIMINGS

①Timing regulations (SXGA mode)

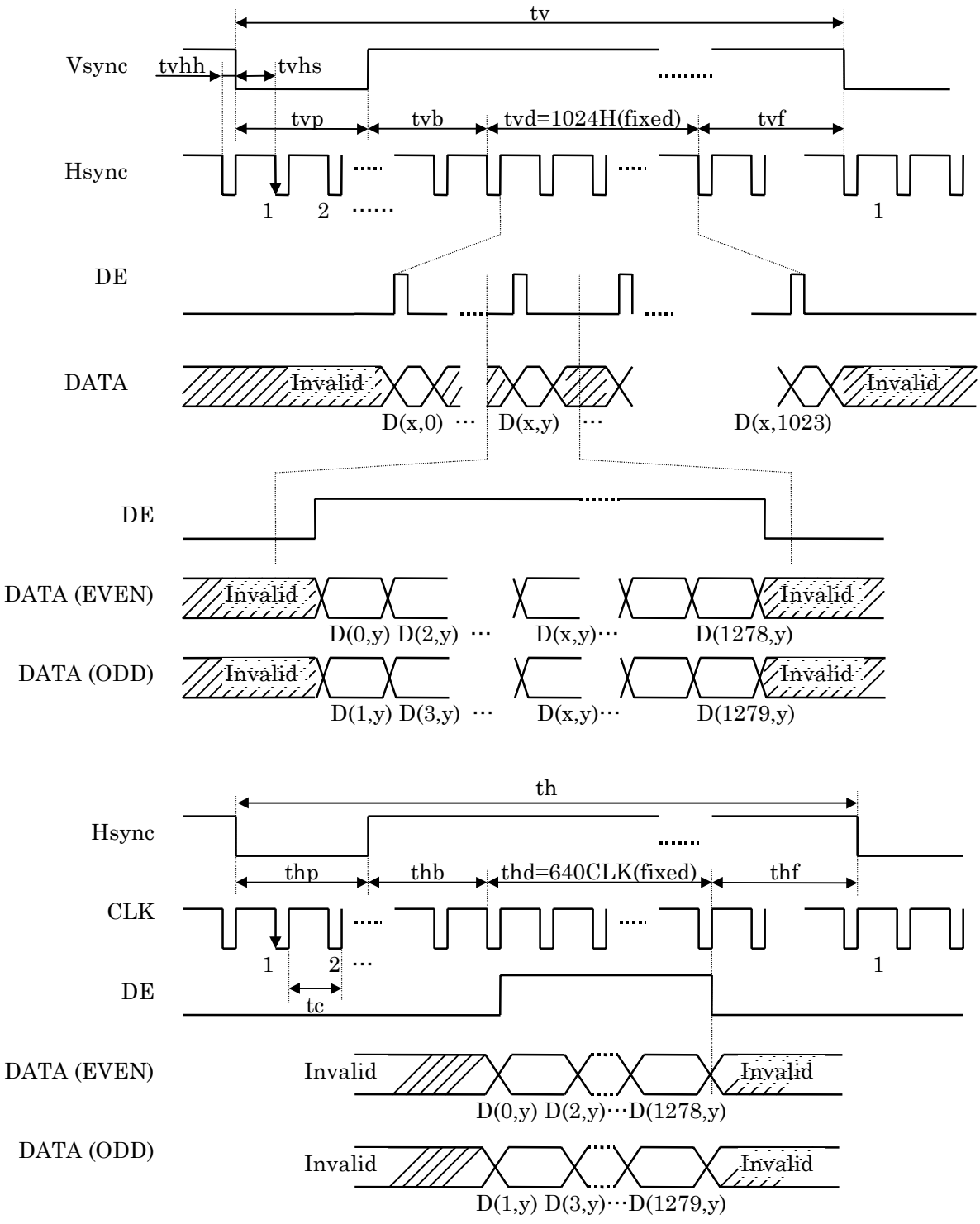
	Parameters	Symbols	Min.	Typ.	Max.	Units	Remarks
CLK	Frequency	fc (1/tc)	65.0	67.5	70.0	MHz	TMDS transmitter input Vf= 75Hz
			51.5	54.0	56.5	MHz	TMDS transmitter input Vf= 60Hz
	Period	tc	―	14.815	―	ns	TMDS transmitter input Vf= 75Hz
			―	18.52	―	ns	TMDS transmitter input Vf= 60Hz
	HIGH period	tch	TBD	―	―	ns	at fc= 81MHz
	LOW period	tcl	TBD	―	―	ns	at fc= 81MHz
	Clock jitter	tIJIT	―	―	2	ns	―
	Rise, fall	tcrf	TBD	―	TBD	ns	―
Hsync	Period	th	12.3 690	12.504 844	― ―	μ s CLK	Typ=80.0kHz Note 2
	Display period	thd	―	640	―	CLK	―
	Front-porch	thf	TBD	―	TBD	CLK	―
	Pulse width	thp *	TBD	72	TBD	CLK	―
	Back-porch	thb *	TBD	124	TBD	CLK	―
	* thp + thb		TBD	―	TBD	CLK	―
Vsync	Period	tv	― 1027	13.329 1066	― ―	ms H	Typ=75.0Hz
	Display period	tvd	―	1024	―	H	―
	Front-porch	tvf *	TBD	―	TBD	H	―
	Pulse width	tvp *	TBD	3	TBD	H	―
	Back-porch	tvb *	TBD	38	TBD	H	―
	* tvf + tvp +tvb		TBD	―	TBD	CLK	―
	Vsync-Hsync timing	tvhs	1	―	―	CLK	for Hsync
	Hsync-Vsync timing	tvhh	1	―	―	CLK	for Hsync
Vsync, Hsync, DE, DATA	DATA-CLK (Set up)	ts	1.5	―	―	ns	―
	CLK-DATA (Hold)	th	3	―	―	ns	―
	Rise, fall	trf	TBD	―	TBD	ns	―
Vsync, Hsync-DE	Fall delay	tDDF	1	―	―	CLK	for fall of DE
	Rise delay	tDDR	1	―	―	CLK	for rise of DE
DE signal	HIGH period	tHDE	―	―	8000	CLK	―
	LOW period	tLDF	10	―	―	CLK	―

Note 1: These values are in the timing regulation of SiL160 (Silicon Image).
The product equivalent to SiL160 (Silicon Image) is recommended to the input of LVDS transmitter.
The Timing regulation prescribes in the input of the LVDS transmitter.

Note 2: “th” must keep both values (time and CLK number).

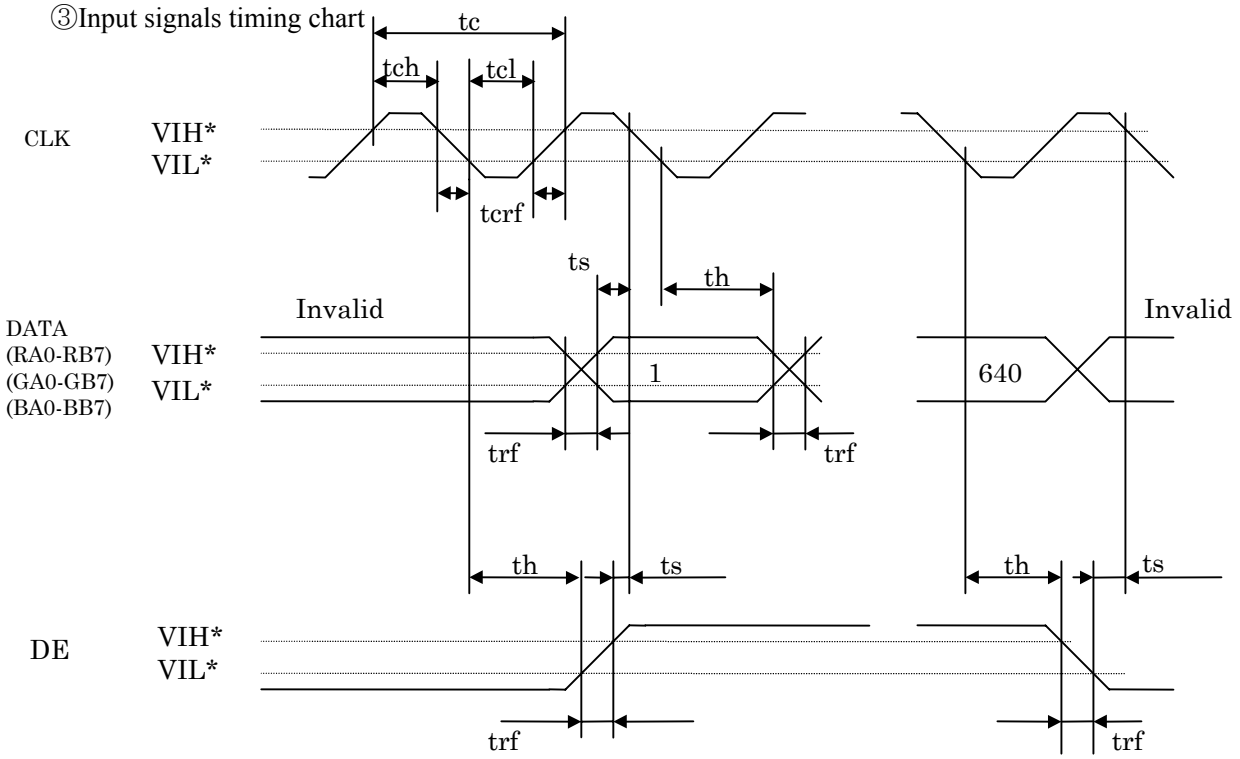
Remark: Shipping inspection is used SiL160 (Silicon Image) as the LVDS transmitter

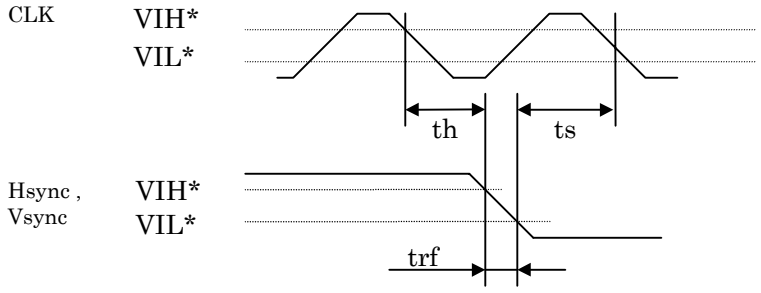
②Input signals timing chart (SXGA mode)

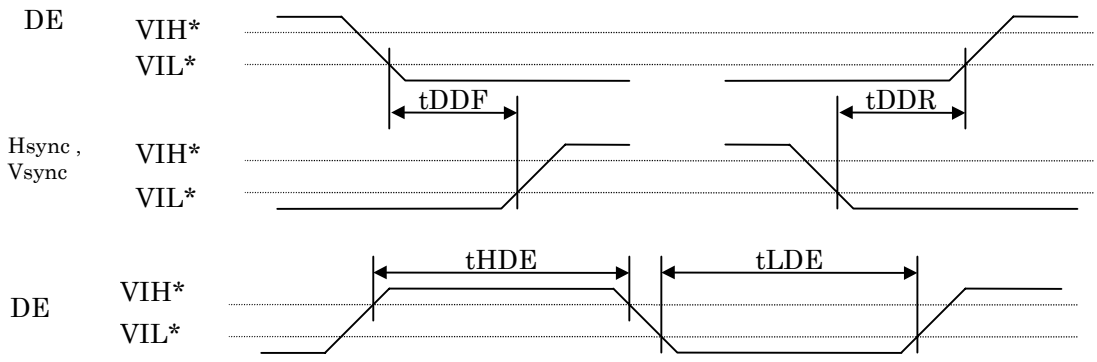


Remark 1: TMDS transmitter input

③Input signals timing chart





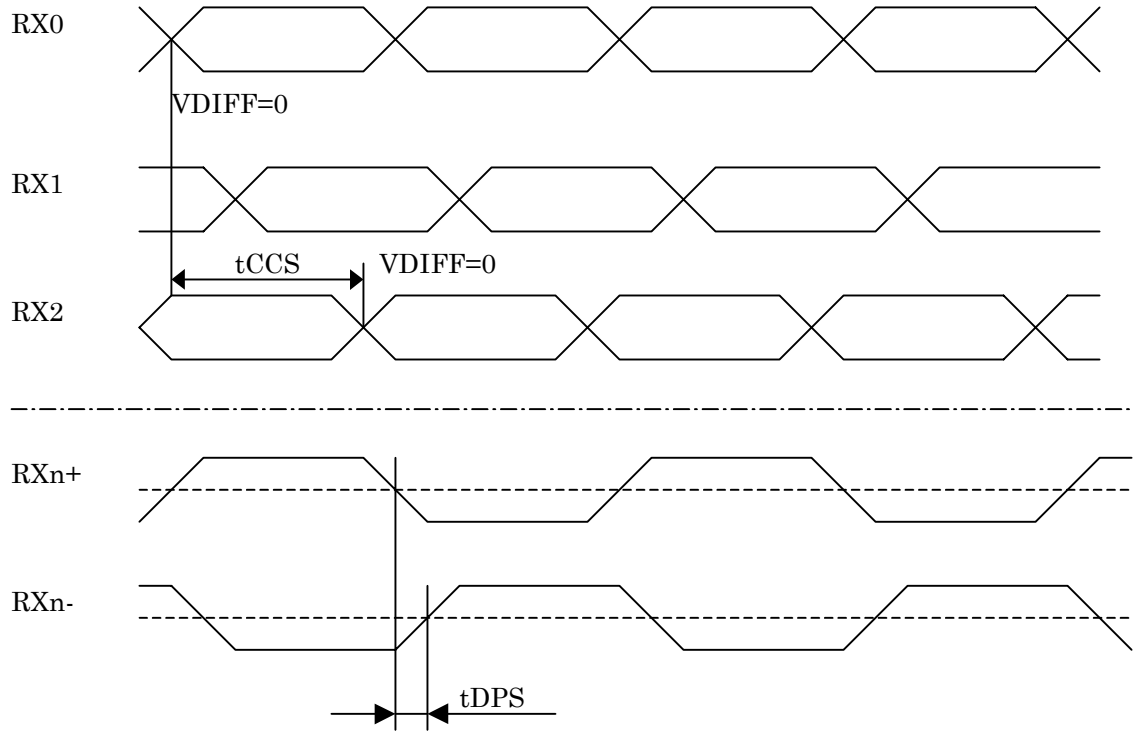


＊VIH and VIL : Refer to TMDS transmitter specifications
Remark 1: TMDS transmitter input

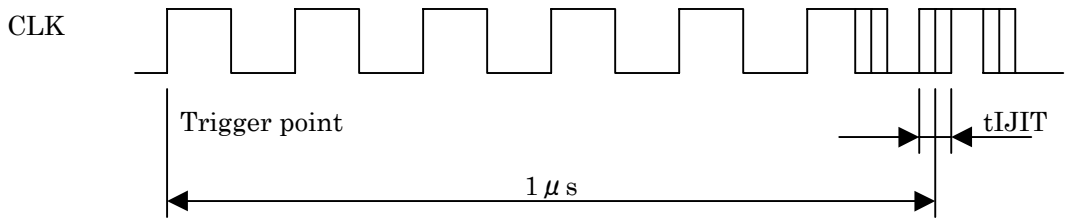
④Timing regulations (TMDS input signals)

Names	Symbols	Min.	Typ.	Max.	Units	Remarks
Differential signal pair skew	tDPS	—	—	245	ps	165MHz,1pixel/clock
Differential signal channel skew	tCCS	—	—	4	ns	165MHz,1pixel/clock
Input CLK jitter	tIJIT	—	—	182	ps	165MHz,1pixel/clock

⑤Input signals timing chart
TMDS receiver input (CN2 input)



⑥Input signals timing chart
TMDS transmitter input



7.8. DISPLAY COLORS vs. INPUT DATA SIGNALS

Display colors		Data signal (0: Low level, 1: High level)																									
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑					:								:								:			
	↓					:								:								:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Colors are developed in combination with 8-bit signals (256 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 16,777,216 (256×256×256) colors.

7.9. PRESET TIMINGS

The eighteen kinds of timings below are already programmed in this module. The input synchronous signals are automatically recognized.

No.	Display size	Vsync (Hz)	Hsync (kHz)	DOTCLK (MHz)	V Pulse (H)	V B.Porch (V)	H Pulse (DOTCLK)	H B.Porch (DOTCLK)	Sync logic V,H	Remarks
1	640×480	59.992	31.469	25.175	2	33	96	48	-,-	VGA
2	720×400	70.087	31.469	28.322	2	35	108	45	+,-	VGA TXT
3	800×600	60.317	37.879	40.000	4	23	128	88	+,+	VESA
4	640×480	66.667	35.000	30.240	3	39	64	96	SonG type A	Macintosh
5	640×480	75.000	37.500	31.500	3	16	64	120	-,-	VESA
6	720×400	85.039	37.927	35.500	3	42	36	144	+,-	VESA※ 1
7	640×480	85.008	43.269	36.000	3	25	48	112	-,-	VESA※ 1
8	1024×768	60.004	48.363	65.000	6	29	136	160	-,-	VESA
9	800×600	75.000	46.875	49.500	3	21	80	160	+,+	VESA
10	832×624	74.565	49.735	57.283	3	39	64	224	SonG type A	Macintosh
11	800×600	85.061	53.674	56.250	3	27	64	152	+,+	VESA※ 1
12	1024×768	70.069	56.476	75.000	6	29	136	144	-,-	VESA
13	1024×768	75.029	60.023	78.750	3	28	96	176	-,-	VESA
14	1280×1024	60.020	63.981	108.000	3	38	112	248	+,+	VESA
15	1152×900	66.003	61.846	94.500	4	31	128	208	CS(-)	SUN※ 1
16	1280×1024	67.189	71.691	117.000	8	33	112	224	CS(-)	SUN
17	1152×900	76.149	71.809	108.000	8	33	128	192	CS(-)	SUN※ 1
18	1280×1024	75.025	79.976	135.000	3	38	144	248	+,+	VESA

*1: Out of specification.

Note 1: Even if the preset timing is entered, a little adjustment of the functions such as Horizontal period, CLK-delay and display position, are required. The adjusted values are memorized in every preset No.

Note 2: This module recognizes the synchronous signals with near preset timing of the frequency of Hsync, Vsync, even in the case that the signals other than the preset timing that were entered. For instance, it is displayed with presetting number 5 in the case of 640×480 dot, HS: 37.861kHz, Vsync: 72.809Hz an example. Adopt the evaluation, because adjustment may not fit, in the case that the magnifying ratio differs or, in the case that you use it with except for the display timing that was preset.

Note 3: The display color scale may be difference between Sync on Green Input and others.

7.10. EXPANSION MODE

T.B.D.

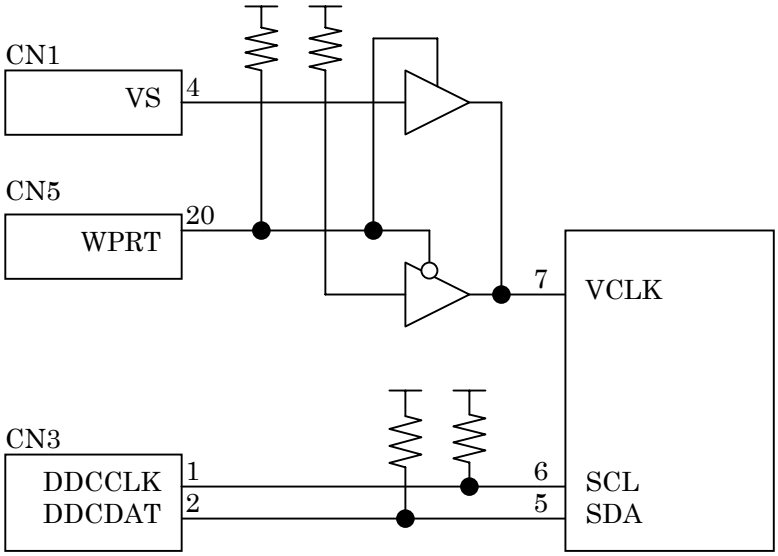
7.11. DDC FUNCTION

This function is corresponding to VESA DDC™ and EDID™ (Structure Version 1).
Follow the specifications of the IC when you write a data. (VCLK is fixed on "H")
Please write a data into necessary addresses in advance when you use this function. Data "55H" in address "00H" and "FFH" in other address are already programmed when shipping. The input equivalent circuit diagram is as follow.

EDID: Extended Display Identification Data

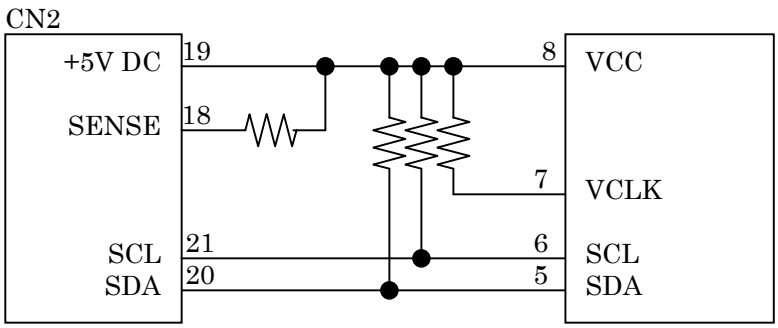
<Internal circuit diagram>

Analog (DDC 1/2B)



Product: Microchip Technology Inc.
24LC21A or equivalent

Digital (DDC 2B)



Product: Microchip Technology Inc.
24LC21A or equivalent

7.12. DPMS

Analog input

This function is corresponding to VESA DPMS™ Standard.

VESA DPMS Standard						NL128102AC31-02A	
State	Signal			Power saving	Recovery time	Power saving	Recovery time
	Horizontal	Vertical	Video				
On	Pulses	Pulses	Active	None	Not applicable	None	Not applicable
Stand-by	No pluses	Pluses	Blanked	Minimum	Short	Maximum	Short
Suspend	Pluses	No pluses	Blanked	Substantial	Longer	Maximum	Short
Off	No pluses	No pluses	Blanked	Maximum	System dependent	Maximum	Short

Digital input

T.B.D.

7.13. CONTROL FUNCTION ITEMS

No.	Items		At digital signal input	Functions
1	Brightness		valid	Brightness of backlight control
2	Contrast	W, R, G, B	valid	White-level of video signals synchronous color and each color control
		W		White-level of video signal synchronous color control
3	Color Level	W, R, G, B	valid	Color level of video signals synchronous color and each color control
		W		Color level of video signal synchronous color control
4	Gamma	W, R, G, B	valid	Gamma of video signals synchronous color and each color control
		W		Gamma of video signal synchronous color control
5	Auto gain		invalid	According to the amplitude of the input signal, the gain can be automatically adjusted.
6	Position	H. Position	invalid	Horizontal position adjust
		V. Position		Vertical position adjust
7	Clock	H. Size	invalid	Horizontal display period adjust
		Clock Phase		CLK-phase adjust
8	Auto adjust		invalid	Clock and Position auto adjust
9	OSD position		valid	OSD position adjust The display position of OSD can be moved.
10	Language		valid	The display language of OSD can choose from the English, German, French and Spanish.
11	All Reset		valid	Reset to initial value The values in No.1 to No.7, No.9 and No.10 are returned to the initial values.
12	Information		valid	Video signal information Display multi-scan function, Hsync and Vsync frequency

Remark 1: ① In order to achieve the best picture quality, the above functions should be adjusted by setting SEL ([S]), UP([↑]), DOWN([↓]), LEFT([←]), RIGHT([→]), RESET([R]) and EXIT([E]) signals.
And Clock and Position adjusted value are memorized every display modes.

② The memorized values are not affected even if the power is switched off. But the selected value is not memorized in case that a selected mode is changed to another one.

Remark 2: The Auto adjusted value may not become an optimal value for the best picture quality by customer equipment and display screens. And the Auto adjust function does not act normally when both Sync On Green signal and separate synchronous signals are input in this module, In those cases, please adjust each function (Clock and Position).

Remark 3: A screen may be disturbed only a moment when each adjusted value is changed.

7.14. FLOW CHART OF CONTROL FUNCTIONS

T.B.D.

7.15. INITIAL VALUE CHAGE FUNCTIONS

This module changes initial value, OSD items, and so on in customers.
The changed initial value becomes initial value in each preset timing, and is applicable when it is reset (including All Reset).

◎How to transpose to initial value change mode.

Connect UP to GND while SEL is connected to GND when OSD function is “information”.

◎Operation

SEL, UP, DOWN and EXIT

◎How to return to normal mode

Connect EXIT to GND or turn off Power supply when OSD closes.
Both LEDON and LEDOFF become “H”, when this mode is operating.

◎Initial value of each item: T.B.D.

7.16. INFORMATION DISPLAY BY OSD

1. Input signal change: Every time it pushes the push button, it changes an analog signal input and a digital signal input.

2. NO SIGNAL: "NO SIGNAL" is displayed for four seconds when signals are no input.

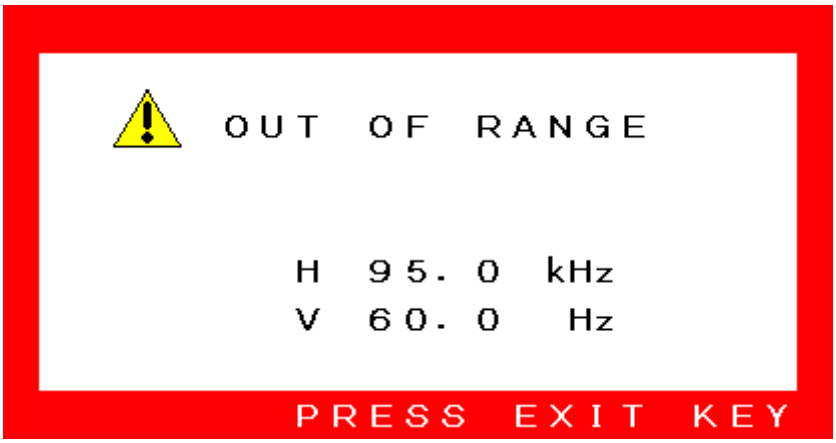
3. POWER SAVE: Frequency of horizontal, vertical synchronous signal is displayed for four seconds at the time of the Power Saving mode switchover.

※It is displayed when Horizontal synchronous signal frequency (Hf) and vertical synchronous signal frequency (Vf) are the following.

① Hf＜10 KHz
② Vf＜40 Hz
③ ① and ②

It is not displayed when Power Save OSD no display is selected with 7.15. INITIAL VALUE CHANGE FUNCTIONS.

4. OUT OF RANGE: Each frequency is displayed for four seconds when the Horizontal and Vertical synchronous signal outside the corresponding range is inputted.



※It is displayed when Horizontal synchronous signal frequency (Hf) and vertical synchronous signal frequency (Vf) are the following.

① 10 kHz≦Hf≦24 KHz or 90 kHz＜Hf
② 40 Hz≦Vf＜50 Hz or 200 Hz≦Vf
③ ①and②

But it is not displayed when either Hf or Vf is power saving mode.

※ Display or no display for Out of Range can not be selected.

5. KEY DISABLE: It is displayed for four seconds that the switch for adjusts is disable.

8. OPTICAL CHARACTERISTICS

(Ta = 25℃, VDD = 12V, VDDB = 12V , Note 1)

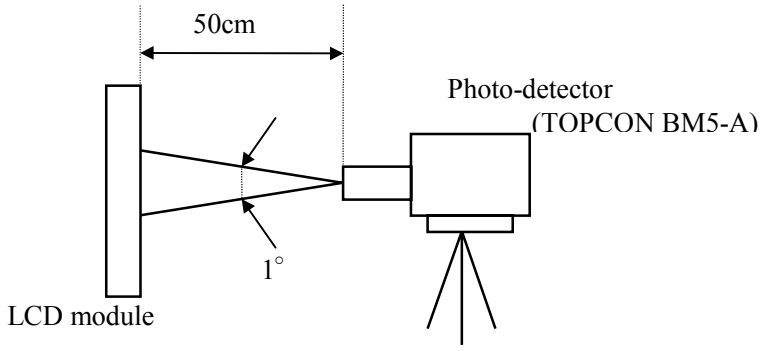
Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio	CR	γ=2.2 viewing angle θR=0°, θL=0°,θU=0°, θD=0°, White／Black, at center	150	250	-	-	Note 2
Luminance	Lvmax	White, at center	200	250	-	cd/m^2	-
Luminance uniformity	—	White	-	1.1	1.3	-	Note 3

Reference data

(Ta = 25℃, VDD = 12V, VDDB = 12V, Note 1)

Items	Symbols	Condition	Min.	Typ.	Max.	Unit	Remarks
Chromaticity Coordinates	W	White (x, y)	-	0.300, 0.315	-	-	-
	R	Red (x, y)	-	TBD	-	-	-
	G	Green (x, y)	-	TBD	-	-	-
	B	Blue (x, y)	-	TBD	-	-	-
Color gamut	C	θR=0°, θL=0°,θU=0°, θD=0°, at center, to NTSC	50	60	-	%	-
Viewing angle range (CR>10)	θ x+	CR > 10, White/Black θU=0°, θD=0°	70	85	-	deg.	Note 4
	θ x-		70	85	-	deg.	
	θ y+	CR > 10, White/Black θR=0°, θL=0°	70	85	-	deg.	
	θ y-		70	85	-	deg.	
Viewing angle range (CR>5)	θ x+	CR > 10, White/Black θU=0°, θD=0°	-	TBD	-	deg.	
	θ x-		-	TBD	-	deg.	
	θ y+	CR > 10, White/Black θR=0°, θL=0°	-	TBD	-	deg.	
	θ y-		-	TBD	-	deg.	
Response time	Ton	Black to White	-	25	TBD	ms	Note 5
	Toff	White to Black	-	35	TBD		
Luminance control range	—	Maximum luminance: 100%	30 to 100			%	-

Note 1: Optical characteristics are measured after 20 minutes from the module works, with all pixels in "white". The typical value is measured after luminance saturation.
Display mode: SXGA-75Hz



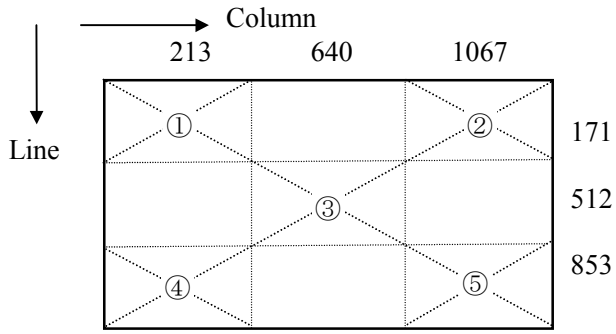
Note 2: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in "white"}}{\text{Luminance with all pixels in "black"}}$$

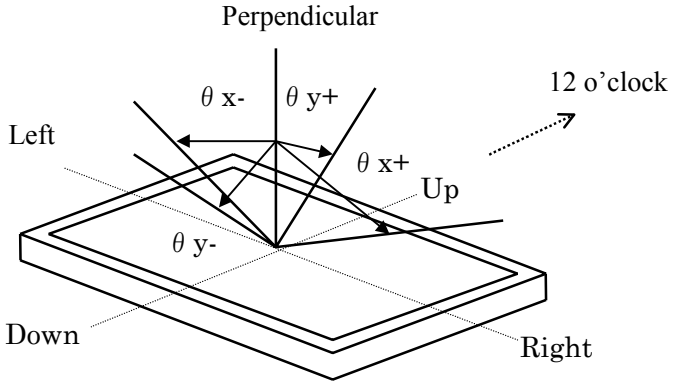
Note 3: Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

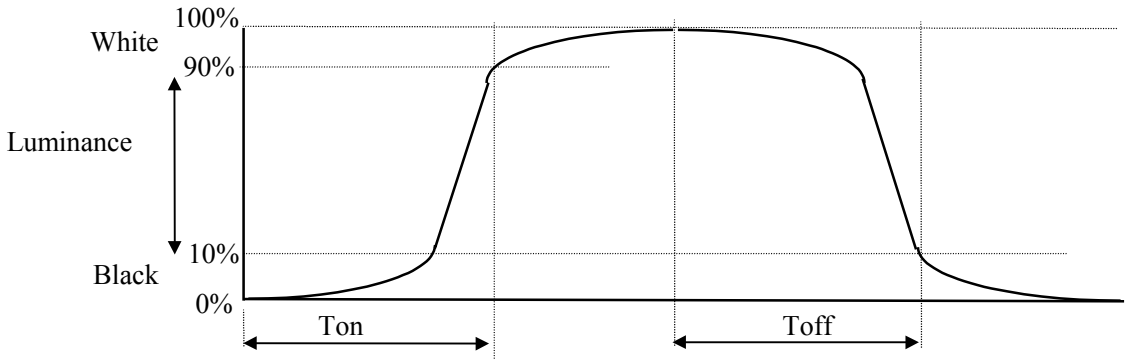
The luminance is measured at near the five points shown below.



Note 4: Definitions of viewing angle are as follows.



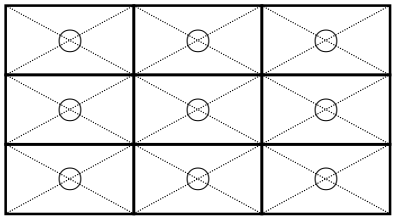
Note 5: Definitions of response time is as follows.
Photo-detector output signal is measured when the luminance changes "black" to "white" or "white" to "black".



9. RELIABILITY TEST

Test items	Test condition	Judgment
High temperature/humidity operation	60±2℃, RH=60% 240 hours, Display data is black.	*1
Heat cycle (operation)	① 0℃±3℃・・・1 hour 55℃±3℃・・・1 hour ② 50 cycles , 4 hours/cycle ③ Display data is black.	*1
Thermal shock (non-operation)	① -20℃±3℃・・・30 minutes 60℃±3℃・・・30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	*1
Vibration (non-operation)	① 5-100Hz, 11.76m/s^2 (1.2G) ② 1 minute/cycle, X,Y,Z direction ③ 10 times each direction	*1, *2
Mechanical shock (non-operation)	① 294m/s^2 (30G), 11ms X,Y,Z direction ② 3 times each direction	*1, *2
ESD (operation)	150pF, 150Ω, ±10kV 9 places on a panel *3 10 times each place at one-second intervals	*1
Dust (operation)	15 kinds of dust (JIS-Z 8901) Hourly 15 seconds stir, 8 times repeat	*1

*1: Display function is checked by the same condition as LCD module out-going inspection.
*2: Physical damage
*3: Discharge points are shown in the figure.



10. EXPECTED LIFE-TIME OF THE BARE LAMP

Note 1, Note 3

	Bare lamp
Condition	Luminance Maximum Room temp.（25±2℃）, Continuous operation
Expected value (MTTF)	50,000h Note 2
Criteria	Half value luminance (compared with initial value.)

Note 1: The lifetime is expected value (reference).
Note 2: These estimations are based on the test results with a bare lamp operation. The MTTF estimation for the module might be different from these values, because of the influence of ambient and clamshell conditions.
Note 3: This module consists of twelve lamps.

11. GENERAL CAUTIONS

Because next figures and sentence are very important, please understand these contents as follows.

⚠CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 **CAUTION**

Do not touch an inverter --on which is stuck a caution label-- while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module
① Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module
① As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.
②
 As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
③ As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
④ Do not pull the interface connectors in or out while the LCD module is operating.
⑤ Put the module display side down on a flat horizontal plane.
⑥ Handle connectors and cables with care.
⑦ When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.
⑧The torque to mounting screw should never exceed 0.39N・m (4 kgf・cm) .

(3) Cautions for the atmosphere
①Dew drop atmosphere should be avoided.
②Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
③This module uses cold cathode fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.
④Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

①Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(5) Other cautions

① Do not disassemble and/or reassemble LCD module.

② Do not readjust variable resistor or switch etc.

③ When returning the module for repair or etc., please pack the module not to be broken. We recommend to the original shipping packages.

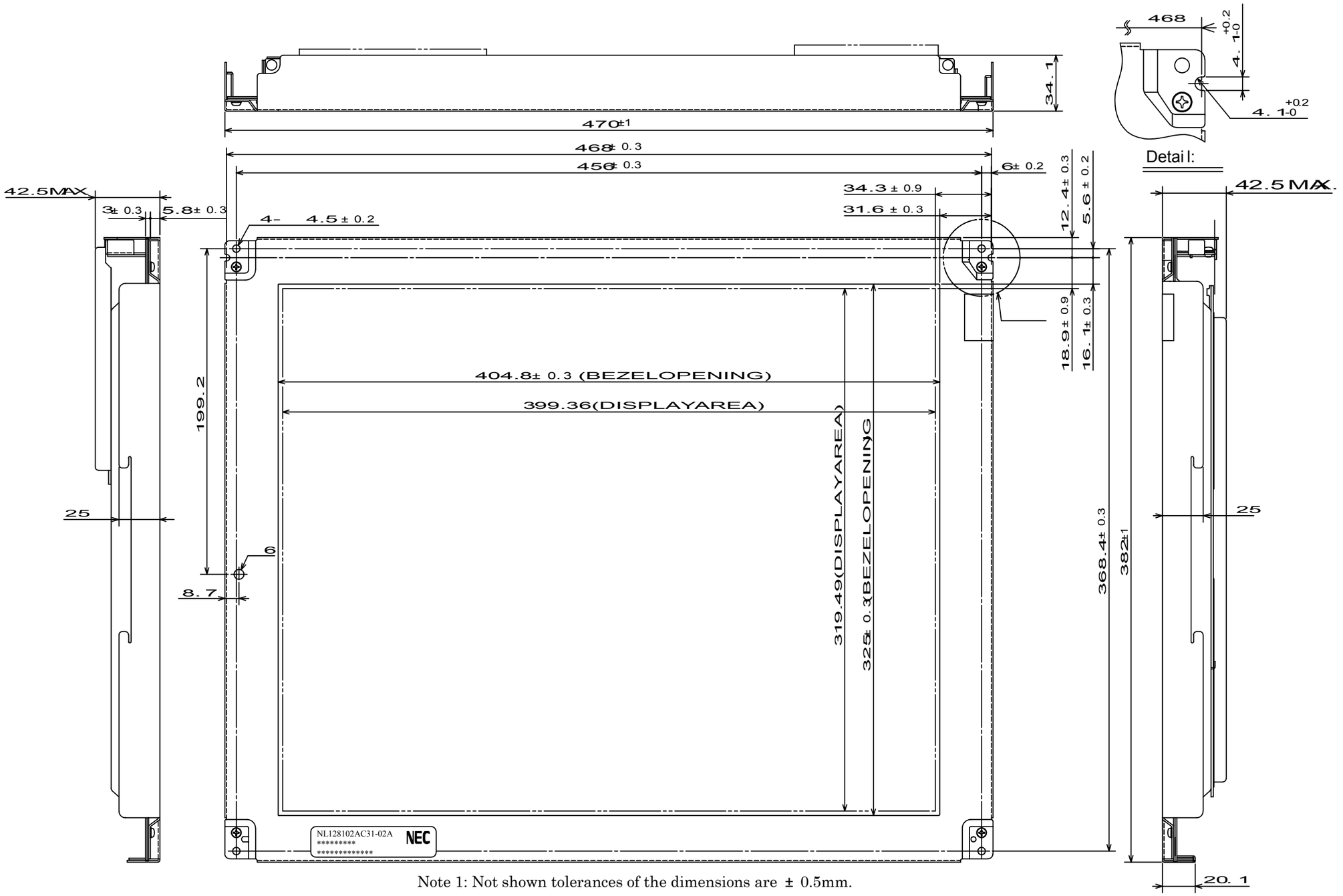
Liquid Crystal Display has the following specific characteristics. There are not defects nor malfunctions.

The display condition of LCD module may be affected by the ambient temperature. The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

12. OUTLINE DRAWINGS (Unit: mm)

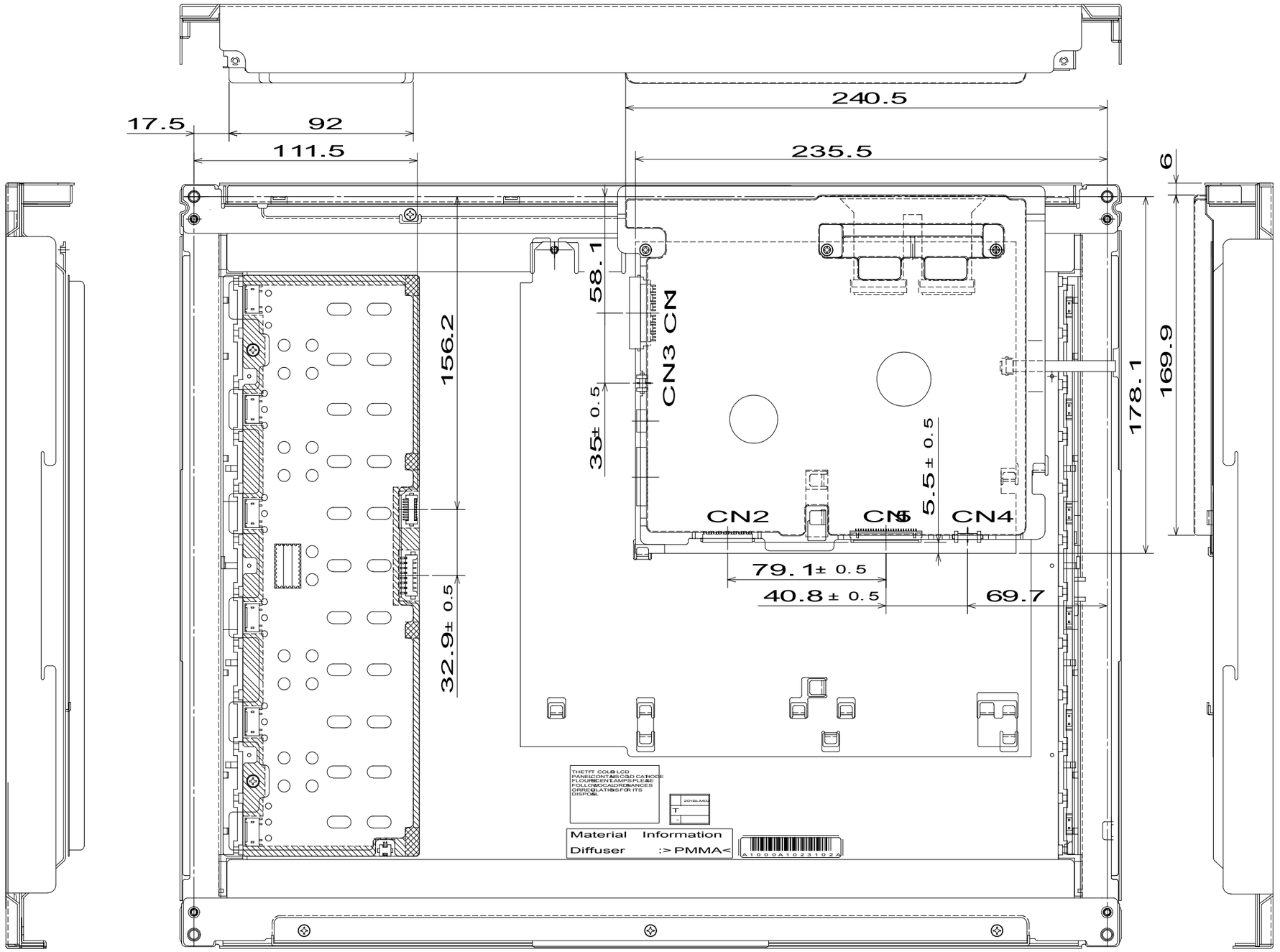
12.1 FRONT VIEW



Note 1: Not shown tolerances of the dimensions are ± 0.5mm.

Note 2: The torque for mounting screw should never exceed 0.392N m(4kgf cm).

12.2 REAR VIEW



Note 1: Not shown tolerances of the dimensions are ± 1.0mm.

Note 2: The torque for mounting screw should never exceed 0.392N m(4kgf cm).

Revision History

Rev.	Prepared Date	Revision contents	Approved	Checked	Prepared	Issued date
1	August 8, 2000	DOD-H-8024				-