NEC

TFT COLOR LCD MODULE

NL10276AC30-07
38cm (15 Type)
XGA

PRELIMINARY DATA SHEET

(6th Edition)

All information is subject to change without notice.

Published by
1st Engineering Department
Color LCD Division
Display Device Operations Unit
NEC Electron Devices

INTRODUCTION

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Anti-radioactive design is not implemented in this product.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL10276AC30-07 module is composed of the driver LSIs for driving the TFT (Thin Film Transistor) array with an amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into the narrow gap between a TFT array glass substrate and a color filter glass substrate.

RGB (Red, Green, Blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn address the individual TFT cells.

Working as an electro-optical switch, each TFT cell regulates transmitted light from the backlight assembly when worked by the data source. Color images are created by regulating the amount of transmitted light through the array of red, green and blue dots.

1.2 APPLICATIONS

- FA monitor

1.3 FEATURES

- Parallel 8bit interface (2 port)
- Ultra-wide viewing angle (with lateral electric field)
- Fast response time
- High luminance
- High contrast
- Wide color gamut
- Luminance control
- Small foot print
- Direct light type
- Replaceable backlight unit and inverter
- Acquisition product for UL/c-UL (File No.E170632)

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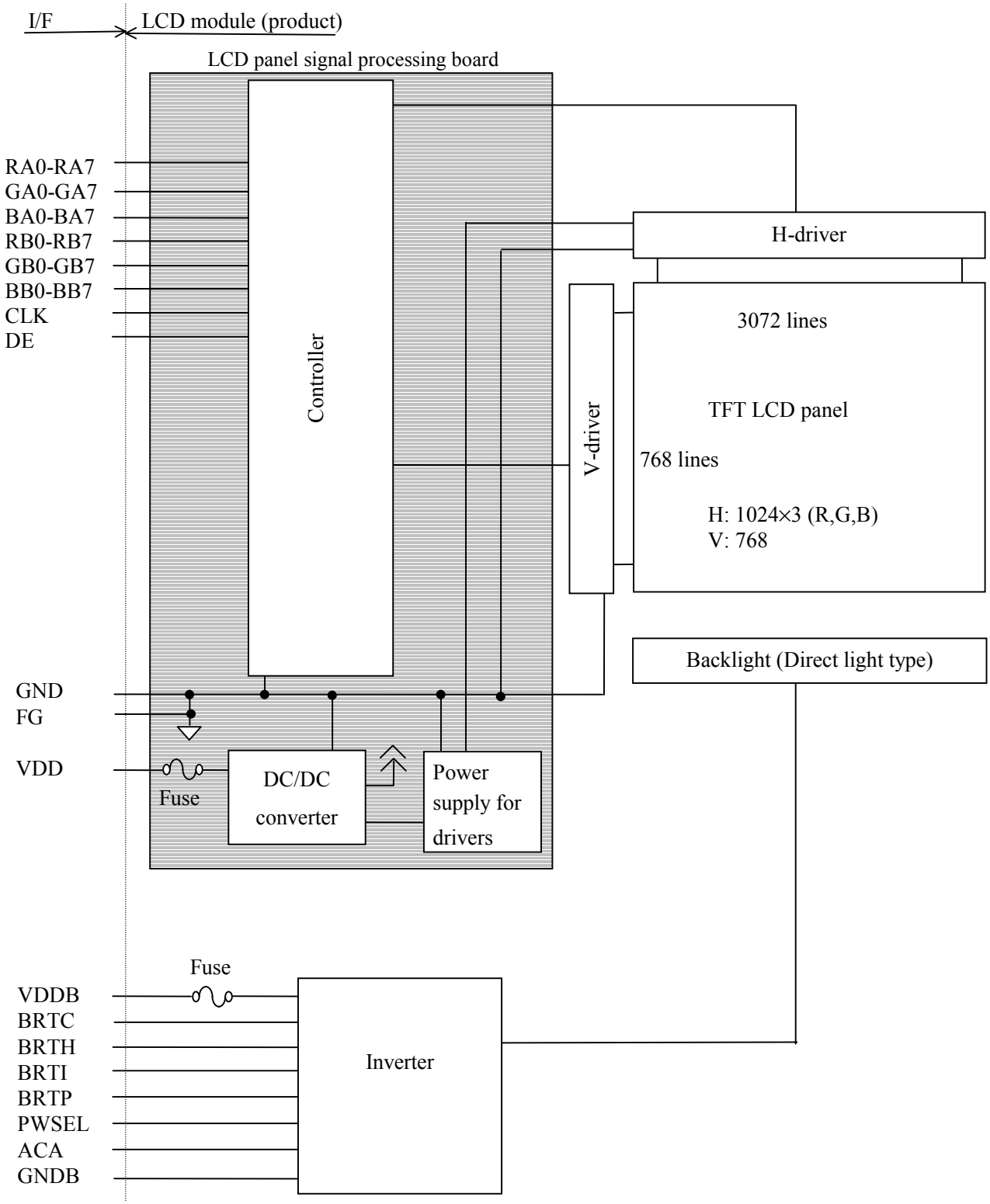
2. GENERAL SPECIFICATIONS

Display area	304.128 (H) × 228.096 (V) mm	
Diagonal size of display	38 cm (15.0 inches)	
Drive system	a-Si TFT active matrix	
Display colors	16,777,216 colors (6bit + FRC)	
Number of pixels	1024 (H) × 768 (V) pixel	
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	
Dot pitch	0.099 (H) × 0.297 (V) mm	
Pixel pitch	0.297 (H) × 0.297 (V) mm	
Module size	330.0 (H) × 256.0 (V) × 30.0 max.(D) mm	
Weight	1100 g (typ.)	
Contrast ratio	300:1 (typ.)	
Viewing angle	At the contrast ratio 10:1 • Horizontal: Left side 85° (typ.), Right side 85° (typ.) • Vertical: Up side 85° (typ.), Down side 85° (typ.)	
Designed viewing direction	• Optimum grayscale (γ=2.2): perpendicular	
Polarizer pencil-hardness	3H (min.) [by JIS K5400]	6
Color gamut	At LCD panel center 60 % (typ.) [against NTSC color space]	
Response time	Ton (black 10%→ white 90%) 20 ms (typ.)	6
Luminance	400 cd/m^2 (typ.)	
Signal system	Parallel 8bit interface (2port) [8-bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE)]	
Supply voltage	LCD panel signal processing board: 5.0V Backlight inverter: 12.0V	
Backlight	Direct light type: 8 cold cathode fluorescent lamps [Replaceable parts] • Backlight unit: 150LHS16 • Inverter: 150PW151	6
Power consumption	At maximum luminance and checkered flag pattern 25.1 W (typ.)	6

3. BLOCK DIAGRAM



Note1: GND (Signal ground) is connected to FG (Frame ground = Metallic bezel) in the LCD module. Neither GND nor FG is connected to GNDB (Backlight ground). These grounds should be connected to system ground in customer equipment.

Note2: Metallic bezel must be connected to system ground in customer equipment to stabilize the ground line.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	330.0 ± 1.0 (H) × 256.0 ± 1.0 (V) × 30.0 max. (D) Note1	mm
Display area	304.128 (H) × 228.096 (V) Note1	mm
Weight	1,100 (typ.), 1200 (max.)	g

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Note1: See "**11.OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit	Remarks
Supply voltage	LCD panel signal board	VDD	-0.3 to +6.0	V	Ta = 25°C
	Inverter	VDDB	-0.3 to +15.0	V	
Input voltage	Display signals Note3	Vi	-0.3 to +3.8	V	Ta = 25°C VDD=5.0V
	BRTC	ViB1	-0.3 to +5.5	V	Ta = 25°C VDDB=12V
	BRTP	ViB2	-0.3 to +5.5	V	
	PWSEL	ViB3	-0.3 to +5.5	V	
	ACA	ViB4	-0.3 to +5.5	V	
	BRTI	ViB5	-0.3 to +1.5	V	6
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature		Top1	0 to +55		Module front surface Note1
		Top2	≤ 65		Module rear surface Note2 6
Relative humidity Note4		RH	≤ 95	%	Ta≤ 40°C
			≤ 85		40°C <Ta≤ 50°C
			≤ 70		50°C <Ta≤ 55°C
Absolute humidity Note4		-	≤ 73 Note5	g/m^3	Ta>55°C 6
Operating altitude			≤ 4,850	m	0°C ≤ Ta ≤ 55°C
Storage altitude			≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: Measure at the display area center
Note2: Measure at the rear shield center
Note3: Display signals are DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7
Note4: No condensation
Note5: Ta = 55°C, RH = 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDD	4.5	5.0	5.5	V	-
Supply current		IDD	-	210 Note1	450 Note2	mA	at VDD=5.0V
Ripple voltage		VRP	-	-	100	mV	at VDD=5.0V
Logic input voltage	Low	VTL	0	-	0.8	V	LVTTL level
Logic input voltage	High	VTH	2.0	-	3.6	V	

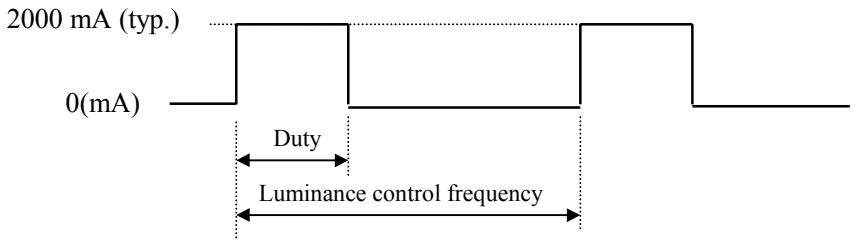
Note1: Checker flag pattern [by EIAJ ED-2522]
Note2: Theoretical maximum current pattern

4.3.2 Driving for backlight inverter

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDDB	11.4	12.0	12.6	V	Backlight power supply
Supply current	Note1	IDDB	-	2000	2400	mA	VDDB=12.0V (at Max. luminance)
Logic input voltage	BRTC	ViBL1	0	-	0.8	V	-
		ViBH1	2.0	-	5.0	V	
	BRTP	ViBL2	0	-	0.8	V	-
		ViBH2	2.0	-	5.0	V	
	PWSEL	ViBL3	0	-	0.8	V	-
		ViBH3	2.0	-	5.0	V	
	ACA	ViBL4	0	-	0.8	V	-
		ViBH4	2.0	-	5.0	V	
Logic input current	BRTC	IiBL1	-610	-	-	µA	-
		IiBH1	-	-	440	µA	
	BRTP	IiBL2	-1580	-	-	µA	-
		IiBH2	-	-	3500	µA	
	PWSEL	IiBL3	-610	-	-	µA	-
		IiBH3	-	-	440	µA	
	ACA	IiBL4	-810	-	-	µA	-
		IiBH4	-	-	440	µA	
BRTI input current	BRTI	IiB5	-130	-	-	µA	-

Note1: Inverter current wave is as follows.



Maximum luminance control : 100% (Duty)
Minimum luminance control : 20% (Duty)
Luminance control frequency : 285±14 Hz (typ.)

Luminance control frequency indicate the input pulse frequency, when select the luminance control with external pulse. See "**4.6.2 Luminance control with external pulse** ".

Note2: The power supply lines (VDDB and GNDB) occurs large ripple voltage (See "4.3.3 Power supply voltage ripple".) while luminance control. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000μF) between the power source lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit. 6

4.3.3 Supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Supply voltage (Acceptable level)	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD (for LCD panel signal processing board; 5.0V)	≤ 100	mVp-p
VDDB (for backlight inverter; 12.0V)	≤ 200	mVp-p

Note1: The permissible ripple voltage includes spike noise.

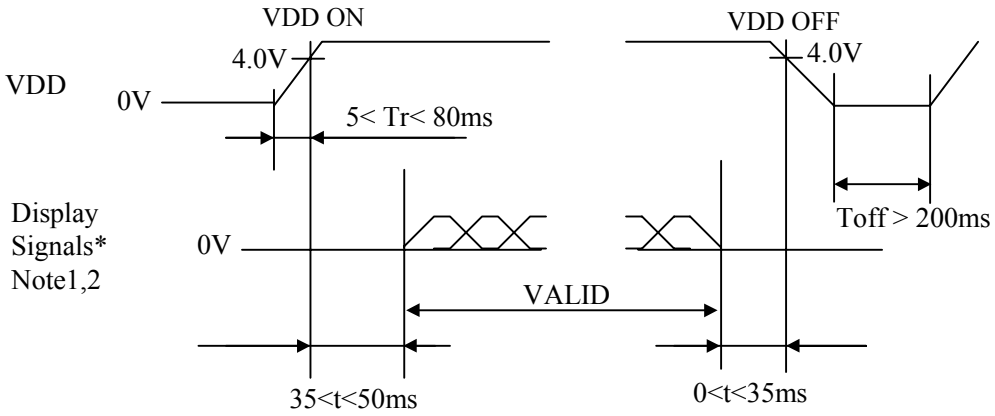
4.3.4 Fuses 6

Item	Fuse		Rating	Unit	Remark
	Type	Supplier			
VDD	FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	4	A	Fusing current Note1
			32	V	-
VDDB	MMCT 5A	SOC Corporation	10	A	Fusing current Note1
			63	V	-

Note1: The power capacity should be more than the fusing current rating. If the power capacity is less than the criteria value, the fuse may not blow, and then nasty smell, smoking and so on may occur.

4.4 SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board



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Note1: Display signals (DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7) must be "0" voltage (V), exclude the VALID period (See above sequence diagram). If input voltage to display signals is higher than 0.3V, the internal circuits might be damaged.

Note2: In terms of fall-off-potential while VDD leading edge is below 4.0V, protection circuits may work and then the module may not work.

Note3: If some of display signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display signals, they should be cut VDD.

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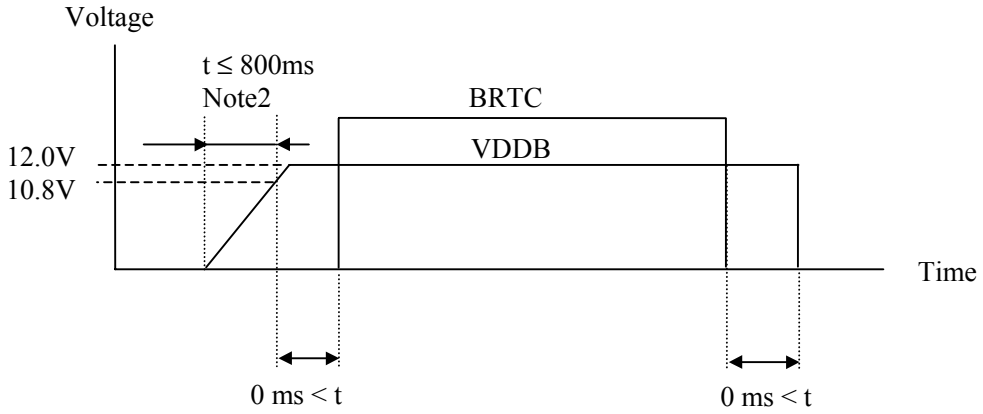
4.4.2 Sequence for backlight inverter



Note1: Backlight ON/OFF should be controlled, while display signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data may be displayed when the backlight power is turned ON/OFF during display signals out.

Note2: Only when BRTC is Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

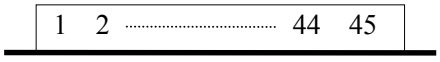
4.5.1 LCD panel signal processing board

CN1 socket (Module side): IL-FHR-F45S-HF (JAE) or FH12S-45S-0.5SH (HIROSE)

Pin No.	Symbol	Function	Description
1	GND	Ground	Connect to system ground.
2	CLK	Dot clock	Dot clock input
3	GND	Ground	Connect to system ground.
4	DE	Data enable	Data enable input
5	GND	Ground	Connect to system ground.
6	N.C.	Non-connection	Keep the terminal open
7	GND	Ground	Connect to system ground.
8	N.C.	Non-connection	Keep the terminal open
9	GND	Ground	Connect to system ground.
10	N.C.	Non-connection	Keep the terminal open
11	GND	Ground	Connect to system ground.
12	BA7	Odd pixel data B	Odd pixel data B input BA7: Most significant bit
13	BA6		
14	BA5		
15	BA4		
16	GND	Ground	Connect to system ground.
17	BA3	Odd pixel data B	Odd pixel data B input BA0: Least significant bit
18	BA2		
19	BA1		
20	BA0		
21	GND	Ground	Connect to system ground.
22	GA7	Odd pixel data G	Odd pixel data G input GA7: Most significant bit
23	GA6		
24	GA5		
25	GA4		
26	GND	Ground	Connect to system ground.
27	GA3	Odd pixel data G	Odd pixel data G input GA0: Least significant bit
28	GA2		
29	GA1		
30	GA0		
31	GND	Ground	Connect to system ground.
32	RA7	Odd pixel data R	Odd pixel data R input RA7: Most significant bit
33	RA6		
34	RA5		
35	RA4		
36	GND	Ground	Connect to system ground.
37	RA3	Odd pixel data R	Odd pixel data R input RA0: Least significant bit
38	RA2		
39	RA1		
40	RA0		
41	VDD	Power Supply	+5V±10%
42	VDD		
43	VDD		
44	VDD		
45	N.C.	Non-connection	Keep the terminal open

Note1: Do not keep pins free (except N.C. Pin) to avoid noise issue.

CN1: Figure of socket

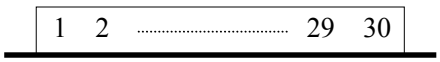


CN2 socket (Module side): IL-FHR-F30S-HF (JAE) or FH12S-30S-0.5SH (HIROSE)

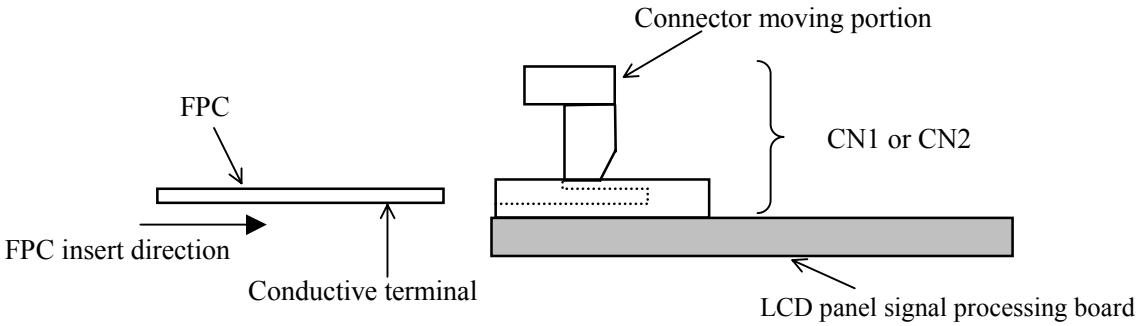
Pin No.	Symbol	Function	Description
1	GND	Ground	Connect to system ground.
2	BB7	Even pixel data B	Even pixel data B input BB7: Most significant bit
3	BB6		
4	BB5		
5	BB4		
6	GND	Ground	Connect to system ground.
7	BB3	Even pixel data B	Even pixel data B input BB0: Least significant bit
8	BB2		
9	BB1		
10	BB0		
11	GND	Ground	Connect to system ground.
12	GB7	Even pixel data G	Even pixel data G input GB7: Most significant bit
13	GB6		
14	GB5		
15	GB4		
16	GND	Ground	Connect to system ground.
17	GB3	Even pixel data G	Even pixel data G input GB0: Least significant bit
18	GB2		
19	GB1		
20	GB0		
21	GND	Ground	Connect to system ground.
22	RB7	Even pixel data R	Even pixel data R input RB7: Most significant bit
23	RB6		
24	RB5		
25	RB4		
26	GND	Ground	Connect to system ground.
27	RB3	Even pixel data R	Even pixel data R input RB0: Least significant bit
28	RB2		
29	RB1		
30	RB0		

Note1: Do not keep pins free to avoid noise issue.

CN2: Figure of socket



Note2: Insert the FPC into the CN1 and CN2 with conductive terminal down.



Sectional drawing of CN1 and CN2

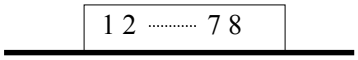
4.5.2 Backlight inverter

CN201 socket (Module side): DF3-8P-2H (HIROSE ELECRIC Co., Ltd.)
Adaptable plug: DF3-8S-2C (HIROSE ELECRIC Co., Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	Ground for backlight	Connect to system ground.
2	GNDB		
3	GNDB		
4	GNDB		
5	VDDB	Power supply for backlight	+12V±5%
6	VDDB		
7	VDDB		
8	VDDB		

Note1: Do not keep pins free to avoid noise issue.

CN201: Figure of socket

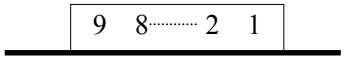


CN202 socket (Module side): IL-Z-9PL1-SMTY (JAE)
Adaptable plug: IL-Z-9S-S125C3 6

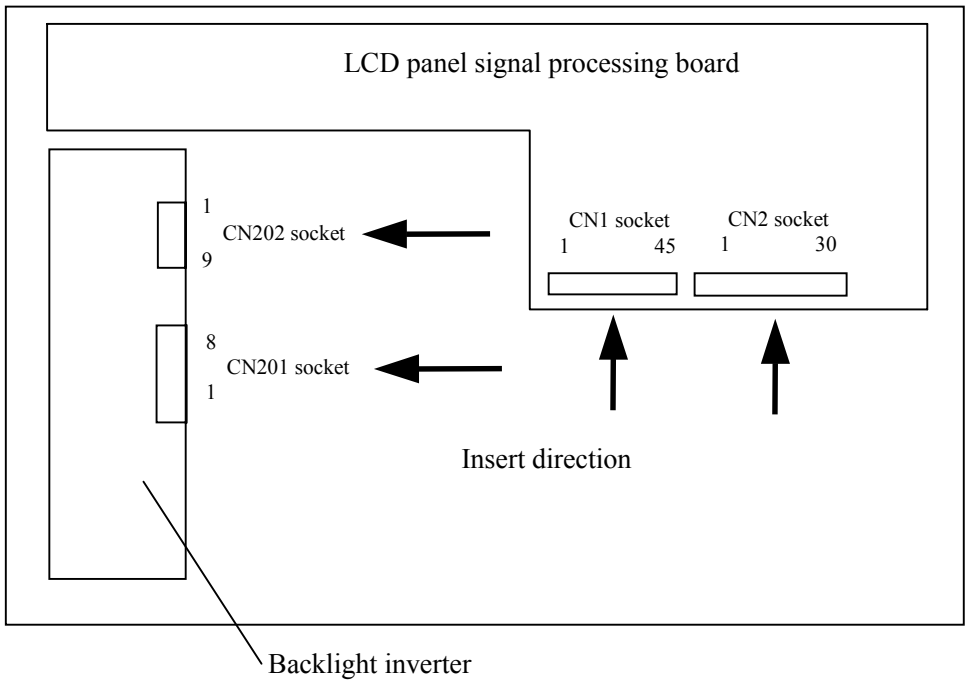
Pin No.	Symbol	Function	Description
1	GNDB	Ground for backlight	Connect to system ground.
2	GNDB		
3	ACA	Luminance control signal	"High" or "Open" : Normal luminance 100% "Low" : Low luminance mode (63% typ.) Note1 6
4	BRTC	Backlight ON/OFF control signal	"High" or "Open" : Backlight ON "Low" : Backlight OFF
5	BRTH	Luminance control signal	See "**4.6 LUMINANCE CONTROLS**". 6
6	BRTI		
7	BRTP		
8	GNDB	Ground for backlight	Connect to system ground.
9	PWSEL	Luminance control select signal	See "**4.6 LUMINANCE CONTROLS**".

Note1: ACA function works, when a resistor is inserted between BRTI and BRTH terminal or BRTI voltage is inputted (See 4.6.1 Luminance control method). In case BRTI terminal is open, ACA function does not work. 6

CN202: Figure from socket view



4.5.3 Position of sockets



4.6 LUMINANCE CONTROLS

4.6.1 Luminance control methods

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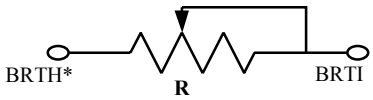
<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL signal</th><th>BRTP signal</th></tr>
<tr><td>Resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, B curve, 1/10W. Minimum point of the resistor is the minimum luminance. Also maximum point of the resistor is the maximum luminance.
 

*BRTH terminal is connected to GNDB in the LCD module.
• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0 kΩ</td><td>30% (Minimum)</td></tr><tr><td>10 kΩ</td><td>100% (Maximum)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment

This control method can carry out continuation adjustment of luminance, if it is adjusted within the rated voltage for BRTI signal (ViB5).
• Luminance ratio Note3
<table><tr><th>BRTI Voltage (ViB5)</th><th>Luminance ratio</th></tr><tr><td>0V</td><td>30% (Minimum)</td></tr><tr><td>1.0V</td><td>100% (Maximum)</td></tr></table></td></tr>
<tr><td>Pulse width modulation
Note1
Note2</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL signal is Low and PWM signal (BRTP signal) is inputted into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.
• Luminance ratio Note3
<table><tr><th>Duty ratio Note4</th><th>Luminance ratio</th></tr><tr><td>0.3</td><td>30% (Minimum)</td></tr><tr><td>1.0</td><td>100% (Maximum)</td></tr></table></td><td>Low</td><td>PWM signal</td></tr>
</table>

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Note1: In case of the resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.

Use PWM method, if interference noises appear on the display image!

Note2: In case BRTC signal is High or Open, the inverter will stop work when BRTP signal is fixed to Low. In this case, backlight will not turn on, even if BRTP signal is inputted again. This is not out of order. Backlight inverter will start to work when power is supplied again.

Note3: These data are the target values.

Note4: See "4.6.2 Detail of PWM timing".

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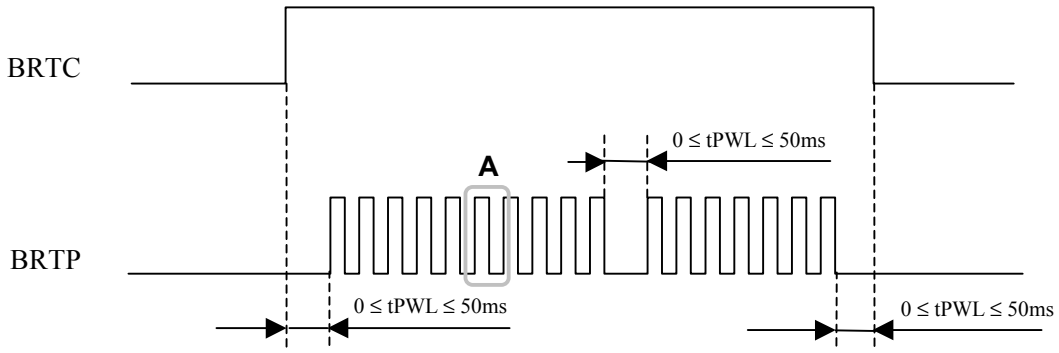
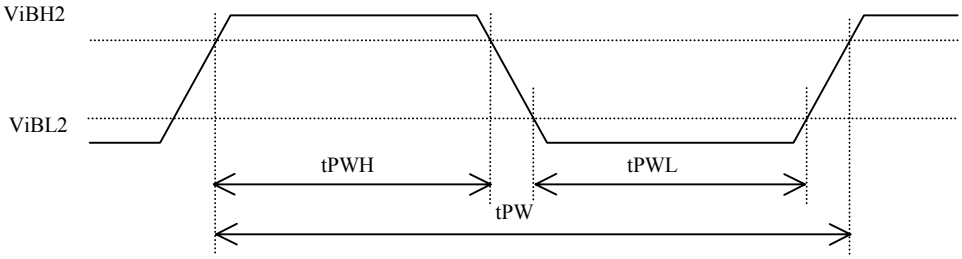
4.6.2 Detail of PWM timing

(1) Timing diagrams

• Outline chart



• Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
Luminance control frequency	FL	185	-	325	Hz	Note1, Note2
Duty ratio	DL	0.2	-	1.0	-	Note1, Note3
Non signal period	tPWL	0	-	50	ms	Note4

Note1:Definition of parameters is as follows.

$$FL = \frac{1}{tPW} \quad , DL = \frac{tPWH}{tPW}$$

Note2: See the following formula for luminance control frequency.
Luminance control frequency = tv × (n+0.25) [or (n + 0.75)]
n = 1, 2, 3 · · · · · ·
tv: See "4.10.4 Timing characteristics".

The interference noise of luminance control frequency and input signal frequency for LCD panel signal processing board may appear on a display. Set up luminance control frequency so that the interference noise does not appear!

Note3: See "4.6.1 Luminance control methods".
Note4: If tPWN is more than 50ms, the backlight will be turned off by a protection circuit for inverter.

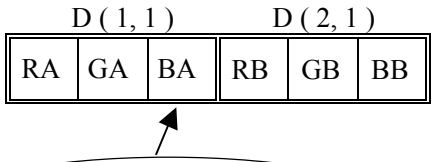
4.7 DISPLAY COLORS TO INPUT DATA SIGNALS

Display color		Data signal (0: Low level, 1: High level)																									
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:								:								:				
	↓				:								:								:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note1: Colors are developed in combination with 8-bit signals (256 steps in grayscale) of each primary red, green, and blue color. This process can result in up to 16,777,216 (256×256×256) colors.

4.8 DISPLAY POSITIONS

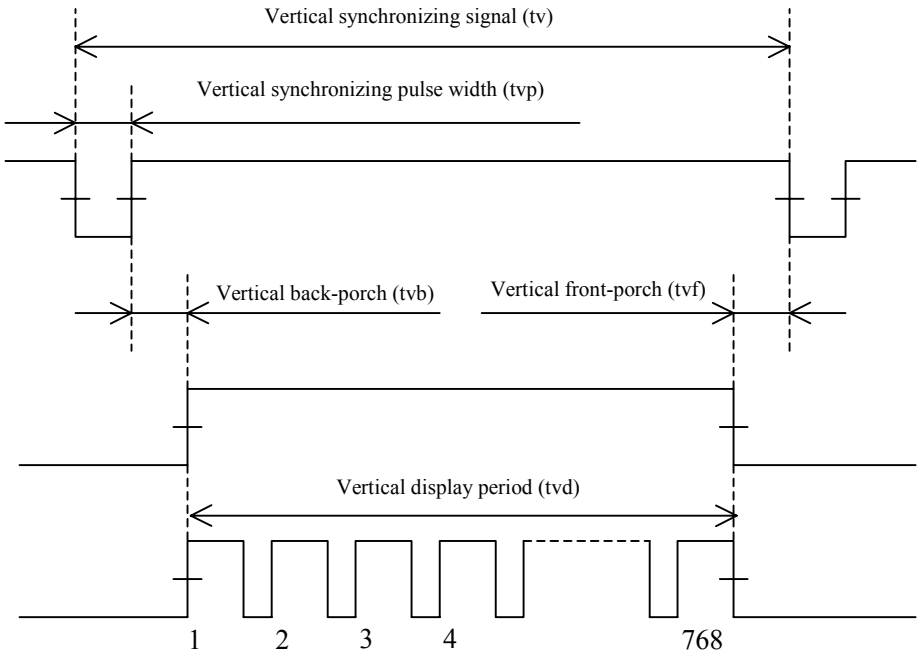
Odd Pixel: RA= R DATA Even Pixel : RB=R DATA
Odd Pixel: GA= G DATA Even Pixel : GB=G DATA
Odd Pixel: BA= B DATA Even Pixel : BB=B DATA

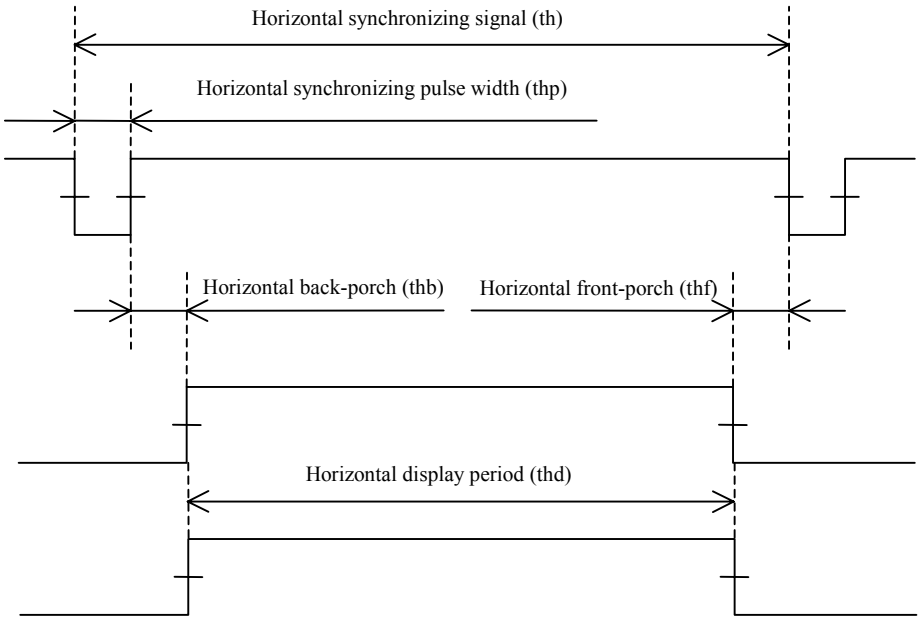


D(1, 1)	D(2,1)	•••	D(1024,1)
D(1,2)	D(2, 2)	•••	D(1024,2)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(1,768)	D(2,768)	•••	D(1024,768)

4.9 INPUT SIGNAL TIMINGS

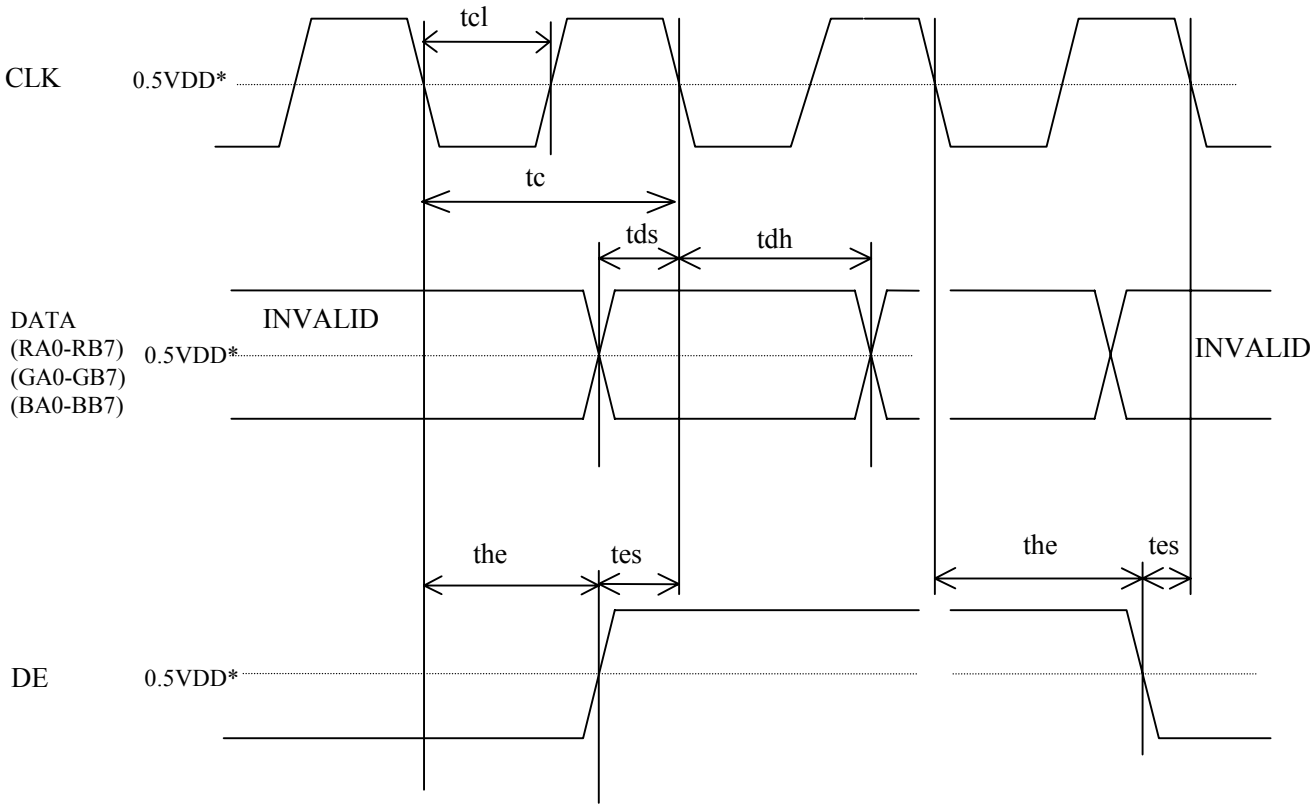
4.9.1 Definition of input signal timings



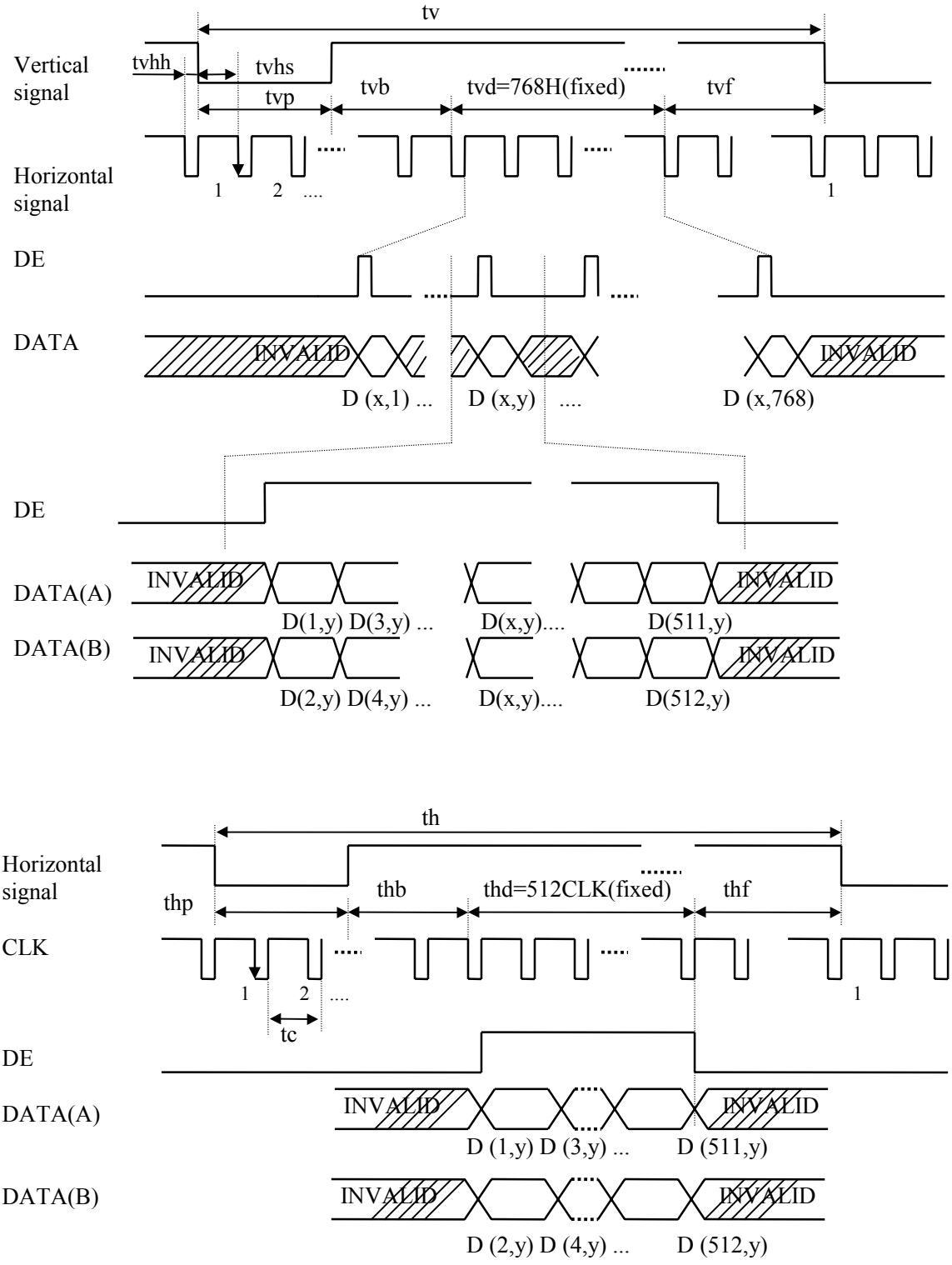


Note1: See "**4.9.4 Detailed input signal timing chart for numeration of pulse**".
Note2: These diagrams indicate virtual signal for set up to timing.

4.9.2 General input signal timing chart



4.9.3 Detailed input signal timing chart



DATA(A): RA0-RA7, GA0-GA7, BA0-BA7
DATA(B): RB0-RB7, GB0-GB7, BB0-BB7

4.9.4 Timing characteristics (2 port input)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	Vf=75Hz	1/ tc	38.5 -	39.375 25.397	40.0 -	MHz ns	-
		Vf=60Hz		31.5 -	32.500 30.769	33.5 -	MHz ns	
	Duty		tcl / tc	0.4	0.5	0.6	-	-
Horizontal	Period	Vf=75Hz	th	12.3 550	16.660 656	- 1000	μs CLK	Typ.=60.023kHz
		Vf=60Hz		12.3 550	20.677 672	- 1000	μs CLK	Typ.=48.363kHz
	Display period		thd		512		CLK	-
	Front-porch	Vf=75Hz	thf	-	8	-	CLK	-
		Vf=60Hz		-	12	-		
	Pulse width	Vf=75Hz	thp *	-	48	-	CLK	-
		Vf=60Hz		-	68	-		
	Back-porch	Vf=75Hz	thb *	-	88	-	CLK	-
		Vf=60Hz		-	80	-		
	* thp + thb			38	-	-	CLK	-
Vertical	Period	Vf=75Hz	tv	- 771	13.328 800	18.5 -	ms H	Typ=75.029Hz
		Vf=60Hz		- 771	16.666 806	18.5 -	ms H	Typ=60.0Hz
	Display period		tvd		768		H	-
	Front-porch	Vf=75Hz	tvf *	-	1	-	H	-
		Vf=60Hz		-	3	-		
	Pulse width		tvp *	-	3	-	H	-
				-	6	-		
	Back-porch		tvb *	-	28	-	H	-
				-	29	-		
	* tvp + tvb +tvf			3	-	-	H	-
	Vsync-Hsync timing		tvhs	1	-	-	CLK	-
	Hsync-Vsync timing		tvhh	1	-	-	CLK	-
DATA (RA0-RB7) (GA0-GB7) (BA0-BB7)	DATA-CLK (Set up)		tds	2	-	-	ns	-
	CLK-DATA (Hold)		tdh	2	-	-	ns	-
DE	DE-CLK timing		tes	2	-	-	ns	-
	CLK-DE timing		the	2	-	-	ns	-

Note1: All parameters should be kept within the specified range. Also Definition of unit is as follows.
1CLK = tc
1H = th

4.10 OPTICAL CHARACTERISTICS

(Ta= 25°C, VDD= 5V, VDDB=12V, Note1)

Parameter	Symbol	Condition	min.	typ.	max.	Unit	Remarks
Contrast ratio	CR	Note 3	250	300	-	-	Note2
Luminance	Lumax	Note 3	300	400	-	cd/m^2	-
Luminance uniformity	-	Max. / Min.	-	1.1	1.3	-	Note3,6
Chromaticity	W	White (x, y)	-	0.300, 0.315	-	-	Note3
	R	Red (x, y)	-	0.630, 0.351	-	-	
	G	Green (x, y)	-	0.322, 0.580	-	-	
	B	Blue (x, y)	-	0.146, 0.112	-	-	

6

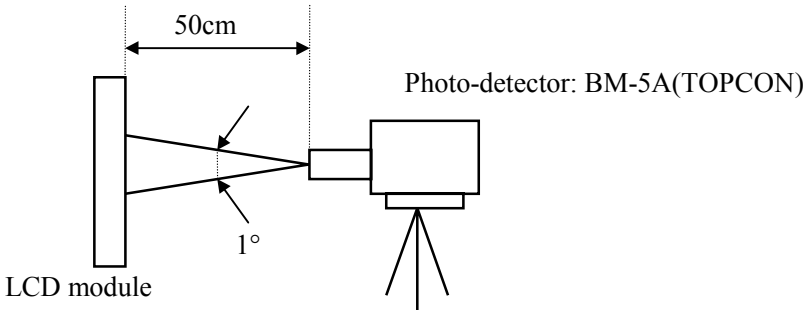
Reference data

(Ta= 25°C, VDD= 5V, VDDB=12V, Note1)

Parameter		Symbol	Condition		min.	typ.	max.	Unit	Remarks
Color gamut		C	To NTSC		50	60	-	%	Note3
Viewing angle (CR>10)	Horizontal	θx+	CR>10, θy = ±0°		70	85	-	deg.	Note4
		θx-			70	85	-	deg.	
	Vertical	θy+	CR>10, θx = ±0°		70	85	-	deg.	
		θy-			70	85	-	deg.	
Response time (Module front surface temperature = 34.5°C)		Ton	Black to white	10%→90%	-	20	30	ms	Note3,5
		Toff	White to black	90%→10%	-	10	20		

6

Note1: Optical characteristics are measured after 20 minutes from the module works. The typical value is measured after luminance saturation. The luminance is measured in dark room.
Input signal timing: XGA-60Hz mode

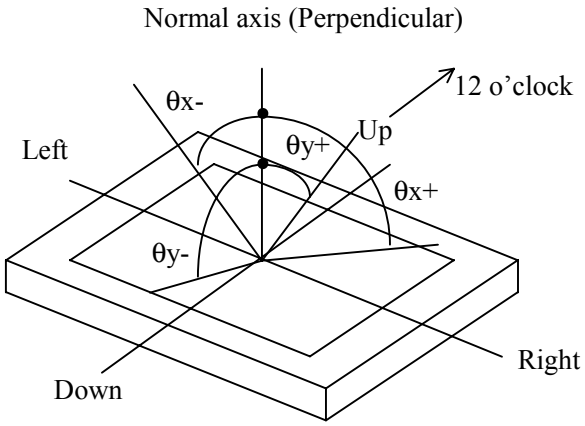


Note2: The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in white}}{\text{Luminance with all pixels in black}}$$

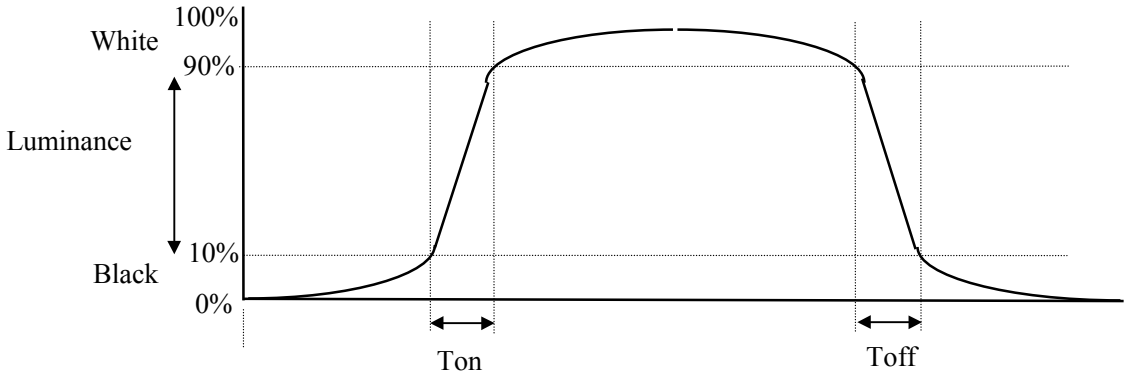
Note3: Viewing angle is θx = ±0°, θy = ±0° and at center.

Note4: Definitions of viewing angles are as follows



Note5: Definitions of response times are as follows.

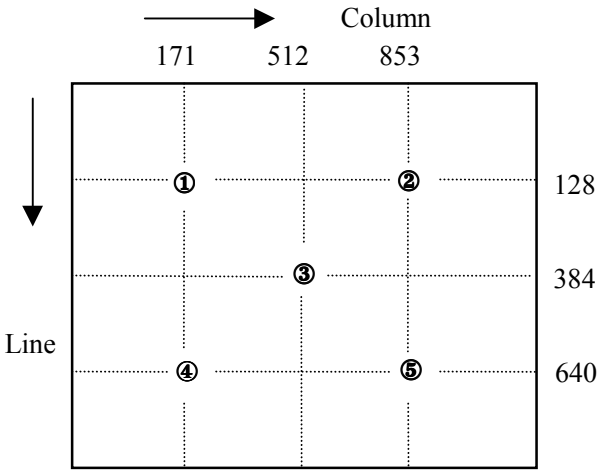
Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).



Note6: Luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

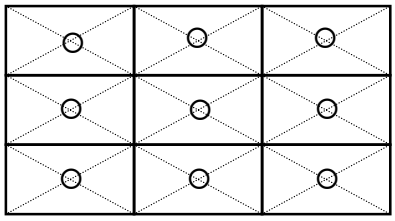
The luminance is measured at near the five points shown below.



5. RELIABILITY TEST

Test item		Test condition	Judgment
High temperature/humidity operation		① 60±2°C, RH=60%, 240 hours, ② Display data is white.	Note1
Heat cycle (operation)		① 0°C ±3°C…1 hour 55°C ±3°C…1 hour ② 50 cycles , 4 hours/cycle ③ Display data is white.	Note1
Thermal shock (non-operation)		① -20°C ±3°C…30 minutes 60°C ±3°C…30 minutes ② 100 cycles ③ Temperature transition time is within 5 minutes.	Note1
Vibration (non-operation)		① 5-100Hz, 11.76m/s^2, 1 minute/cycle, X,Y,Z direction ② 10 times each direction	Note1, Note2
Mechanical shock (non-operation)		① 294m/s^2, 11ms X,Y,Z direction ② 3 times each direction	Note1, Note2
ESD (operation)		150pF, 150Ω, ±10kV 9 places on a panel Note3 10 times each place at one-second intervals	Note1
Dust (operation)		Sample dust: No. 15 (by JIS-Z8901) Hourly 15 seconds stir, 8 times repeat	Note1
Low pressure	operation	53.3 kPa 0°C±3°C … 24 hours 55°C±3°C … 24 hours	Note 1
	non-operation	15 kPa -20°C ±3°C --- 24 hours -60°C±3°C --- 24 hours	

Note1: No display malfunctions (Display functions are checked under the same conditions as out-going inspection.)
Note2: Physical damage
Note3: See the following figure for discharge points.



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to understand following contents, respectively.**

⚠CAUTION	This sign has a meaning that customer will be injured himself and/or the module will sustain a damage, if he makes a mistake in operations.

This sign has a meaning that customer will get an electric shock if he makes a mistake in operations.

This sign has a meaning that customer will be injured himself if he makes a mistake in operations.

6.2 CAUTIONS

Do not touch HIGH VOLTAGE PART of the inverter while turn on. Customer will be in danger of an electric shock.

∗ Pay attention to handling for the working backlight. It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight. There will be in danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 (30G) and to be not greater 11ms, Pressure: To be not greater 19.6N (2kgf))

6.3 ATTENTIONS

(1) Handling the product

① When customer pulls out products from carton box, take hold of both ends without touch the circuit board. If customer touches it, products may be broken down and/or out of adjustment, because of stress to mounting parts.

② If customer places products temporarily, turn down the display side and place on a flat table.

③ Handle products with care and avoid electrostatic discharge (e.g. Decrease with earth band, ionic shower, etc.), because products (LCD modules) may be damaged by electrostatic.

④ The torque for mounting screws should never exceed 0.39N·m. Over torque may cause mechanical damage to the product.

⑤ Do not press or friction, because LCD panel surface is sensitive. If customer will clean the product surface, NEC Corporation or their supplier will recommend using the cloth with ethanolic liquid.

⑥ Do not push-pull the interface connectors while turn on, because wrong power sequence may break down the product.
⑦ Connection cables such as flexible cable, and so on, are danger of damage. Do not hook cables nor pull them.

(2) Environment
① Dewdrop atmosphere must be avoided.
② Do not operate and/or stores in high temperature and/or high humidity atmosphere. If customer store the product, keep in antistatic pouch in room temperature, because of avoidance for dusts and sunlight.
③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
④ Use an original protection sheet on product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color and/or properties of the polarizer.

(3) Specification for products
① Do not display the fixed pattern for a long time because it may cause image sticking. If the fixed pattern is displayed on the screen, use a screen saver.
② The product may be changed of color by viewing angle because of the use of condenser sheet for backlight unit.
③ The product may be changed of luminance by voltage variation, even if power source applies recommended voltage to backlight inverter.
④ Optical characteristics may be changed by input signal timings.

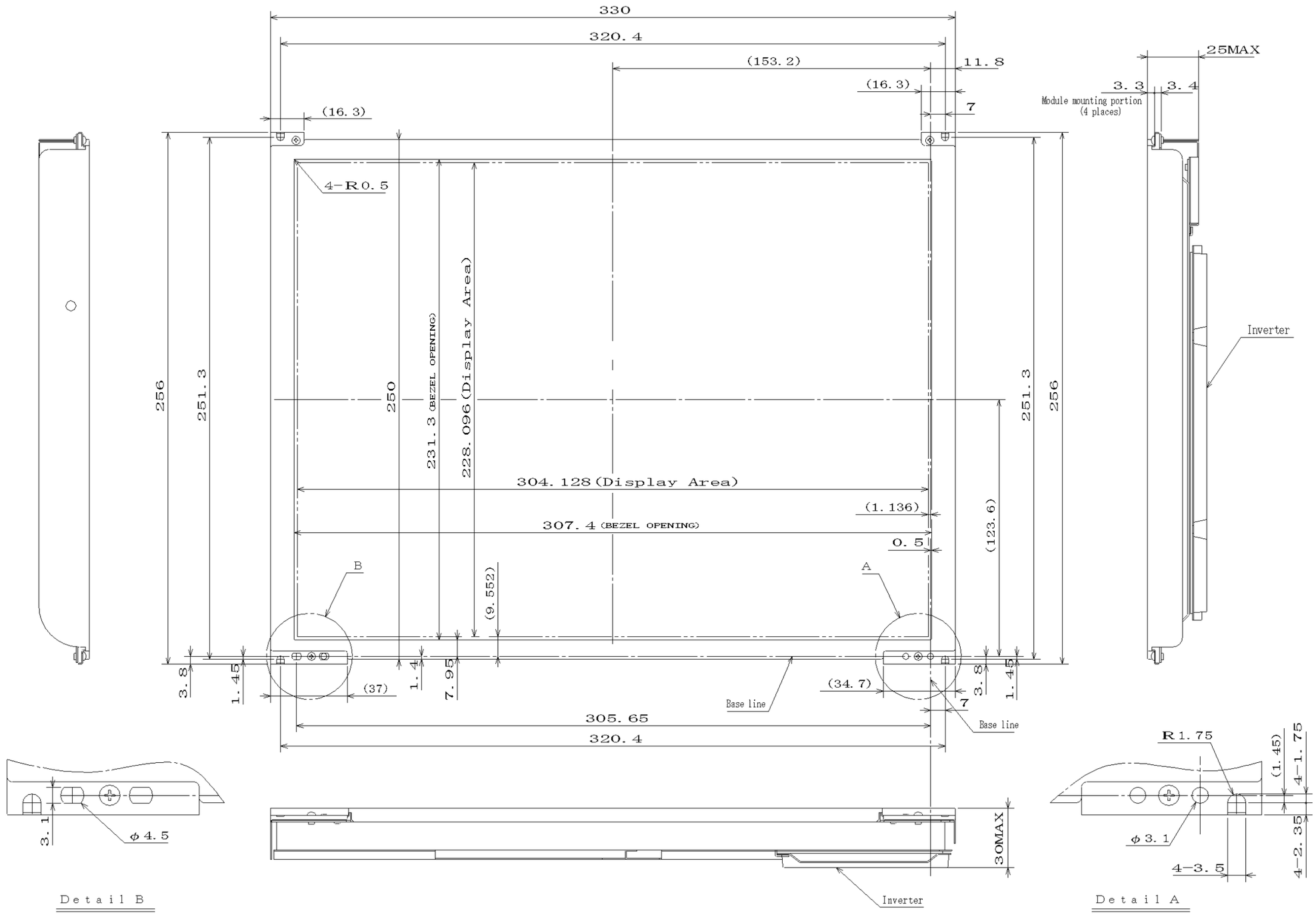
(4) Other
① All GND, GNDB, VDD and VDDB terminals should be connected without a non-connected signal line.
② Do not disassemble a product and/or adjust volume.
③ If customer would like to replace backlight lamps, see 'REPLACEMENT MANUAL FOR BACKLIGHT'.
④ If customer use screwnails, pay attention not to insert waste materials in inside of products.
⑤ When customer returns product for repair and so on, pack it with original shipping package because of avoidance of some damages during transportation.

General specifications for the LCD
The following items are neither defects nor failures.

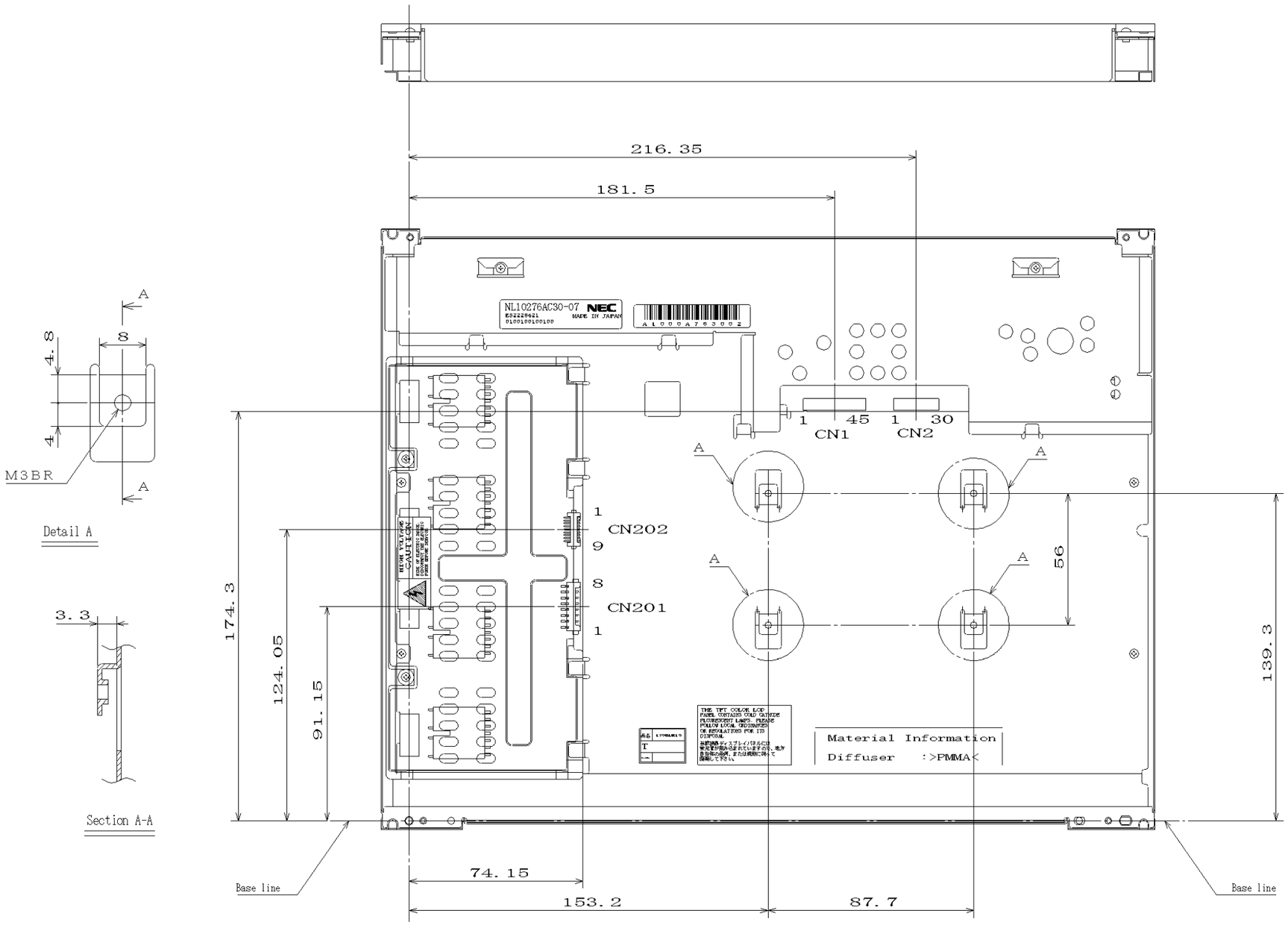
∗ Response time, luminance and color gamut may be changed by ambient temperature.
∗ The LCD may be seemed luminance uniformity, flicker, vertical seam and/or small spot by display patterns.
∗ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.

7. OUTLINE DRAWINGS(Unit: mm)

7.1 Front view



7.2 Rear view


216.35
181.5
NL10276AC30-07 NEC
MADE IN JAPAN
1 45 1 30
CN1 CN2
A
4.8
8
4
M3BR
Detail A
3.3
Section A-A
1
CN202
9
8
CN201
1
174.3
124.05
91.15
56
139.3
THE TFT COLOR LCD PANEL CONTAINS COLD CATHODE FLUORESCENT LAMP. PLEASE FOLLOW LOCAL ORDINANCES OR REGULATIONS FOR ITS DISPOSAL.
Material Information
Diffuser :>PMMA<
Base line
74.15
153.2
87.7
Base line

Rev.	prepared date	Revision contents	Signature of writer
1st edition	Jan. 25, 2001	DOD-M-0094(abstract)	*Approved by* A. OKAMOTO *Checked by* ——— *Prepared by* R.KAWASHIMA
2nd edition	Feb. 6, 2001	DOD-M-0140(abstract) P5 Outline of characteristics: Expression of viewing angle is revised. P7,8 Symbols: VCC→VDD, ICC→ IDD (correction) P7 ABSOLUTE MAXIMUM RATINGS: VDD is corrected. P14 (4) Luminance control: Expression of remark is revised. P15 Symbols: Luminance→Luminance ratio (correction) P23 Vibration: 50 times→10 times (collection) ESTIMATED LIFE TIME OF THE BARE LAMP is deleted.	*Approved by* A. OKAMOTO *Checked by* ——— *Prepared by* R.KAWASHIMA
3rd edition	Mar. 30, 2001	DOD-M-0276 Change part (Before-2nd edition → After-3rd edition) The inside of this document is revised the clerical error and unclear expression in previous one. The important changes such as specifications, characteristics and functions are as follows. P5,P7,P28 Module size (Vertical): 255.4mm→256.0mm P6 BLOCK DIAGRAM-Vertical resolution: 1024→768 P7 ABSOLUTE MAXIMUM RATINGS •VDDB: -0.3 to +16.0V → -0.3 to +15.0V •ACA is added. • Absolute humidity: Absolute humidity shall not exceed Ta=50°C, Relative humidity =70% level. → ≤ 78 g/m^3 P8 Driving for backlight inverter •Logic input voltage is added. •ACA is added. P13 Backlight inverter- CN202 socket-Pin No.2: N.C. →ACA P18 Definition of input signal timings are added. P24 RELIABILITY TEST: Low pressure is added. P27,P28 OUTLINE DRAWINGS are revised.	*Approved by* A. OKAMOTO *Checked by* ——— *Prepared by* R.KAWASHIMA

Rev.	prepared date	Revision contents	Signature of writer
4th edition	June 12, 2001	DOD-M-0433 Change part (Before-3rd edition → After-4th edition) The inside of this document is revised the clerical error and unclear expression in previous one. The important changes such as specifications, characteristics and functions are as follows. P4 Applications: PC monitor is deleted. P5, P7, P28 Module thickness: 32.0mm Max. → 30mm Max. P5, P7 Module weight: 1200g Typ., TBD Max. → 1100g Typ., 1200g Max. P5, P23 Contrast ratio is decided. P5, P23: Luminance is decided. P6 Block diagram: Note1 is changed. P7 Absolute maximum ratings BRTP, PWSEL, ACA, BRTL, Operating altitude and Storage altitude: Each parameter is decided. P8 Electrical characteristics IDD, BRTC, BRTP, PWSEL, ACA and BRTL: Each parameter is decided. P9 Luminance control frequency is decided. P9 Fuses are decided. P10 Sequence for LCD panel signal processing board is decided. P11 CN1 socket: "FH12S-45S-0.5SH (HIROSE)" is added. Adaptable plug is deleted. P12 CN2 socket: "FH12S-30S-0.5SH (HIROSE)" is added. Adaptable plug is deleted. Note2 is added. P28, P29: Outline drawings are changed.	*Approved by* A. OKAMOTO *Checked by* _____ *Prepared by* R.KAWASHIMA
5th edition	Oct. 5, 2001	DOD-M-0672 P5 Power consumption 24W→28W P6 Block diagram • Fuses are added. • Note2 is added. • "ACA" is added. P7 Absolute maximum ratings Note1 and Note2 are corrected. P8 Driving for backlight inverter - IDDB 1800mA typ., 2100mA max. → 1800mA typ., 2100mA max. P9 Supply voltage ripple • Examples of the power supply connections are deleted. Fuses • Fuse for VDDB: KE40 → MMCT 5A • Note1 is added. • Note2 is revised. P10 Sequence for LCD panel signal processing board Note2 is deleted. P22 Timing characteristics are revised.	*Approved by* T. ITO *Checked by* _____ *Prepared by* R. KAWASHIMA

Edition	Document number	Prepared date	Revision contents and writer
6th edition	DOD-M-0843	Jan. 18, 2002	**Revision contents** P4 ·Features: UL acquisition is added. P5 ·Polarizer pencil-hardness: 2H→3H ·Response time: Ton =10 ms (typ.)→ Ton =20 ms (typ.) ·Backlight: Replaceable parts are decided. ·Power consumption: 28W→25.1W P6 ·Block diagram ·Fusing currents are deleted. ·Inverter pin connection: BRTL→BRTI ·Note1 and Note2 are changed. P7 ·Display area: Tolerances are deleted. ·Input voltage: BRTL→BRTI ·Operating temperature Top2 is decided. ·Absolute humidity: ≤78 → ≤73 P8 ·IDD: 300mA typ., 600 mA max. → 210mA typ., 450 mA max. ·IDDB: 2200mA typ., 2600 mA max. → 2000mA typ., 2400 mA max ·BRTL → BRTI P9 ·Note2 is added. ·Expression of fuses is corrected. P10·VDD rising period: Tr< 80ms → 5< Tr< 80ms ·Note3 is revised. P13·Adaptable plug is decided. P14·Adaptable plug is decided. ·ACA: Value of low luminance is decided. Note1 is added. ·BRTL → BRTI P15·Expression of luminance control is revised. ·Luminance ratio is decided. ·BRTL → BRTI P23·Response time: Ton =10 ms (typ.)→ Ton =20 ms (typ.) ·Chromaticity (R, G and B) is decided. ·Viewing angle (CR>5) is deleted. ·Luminance control range is deleted. P24·Note5 is revised. P25·Dust: Test condition is corrected. **Signature of writer** *Approved by* T. ITO *Checked by* *Prepared by* R. KAWASHIMA