DATA SHEET

NEC

TFT COLOR LCD MODULE
NL10276AC28-01A

36 cm (14.1 inches), 1,024 × 768 pixels, Full-color, Multi-scan Function Incorporated backlight with inverter

DESCRIPTION

NL10276AC28-01A is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC28-01A has a built-in backlight with an inverter.

The 36 cm (14.1 inches) diagonal display area contains 1,024 × 768 pixels and can display full-color (more than 16 million colors simultaneously). Also, it has multi-scan function.

NL10276AC28-01A is a model which mounted the CRT interface board on NL10276AC28-01.

FEATURES

- High luminance (200 cd/m^2, TYP.)
- Low reflection
- CRT interface board
  - Auto recognition of input signal (Analog RGB signals, Synchronous signals (Hsync, Vsync, Composit))
  - Digital control: e.g., Brightness, Display position
  - Free supply voltage sequence
  - Corresponding to DDC™1 and DDC2B
  - Corresponding to VESA™, DPMS™
- Multi-scan function: e.g., XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Incorporated edge type backlight with an inverter (Two lamps into two lamp holders)
- Lamp holder replaceable (Part No.: 141LHS-1)

VESA : Video Electronics Standards Association
DPMS : Display Power Management Signaling
DDC1 : Display Data Channel 1
DDC2B : Display Data Channel 2B

APPLICATIONS

Desk-top type of PC
Engineering work station

The information in this document is subject to change without notice.

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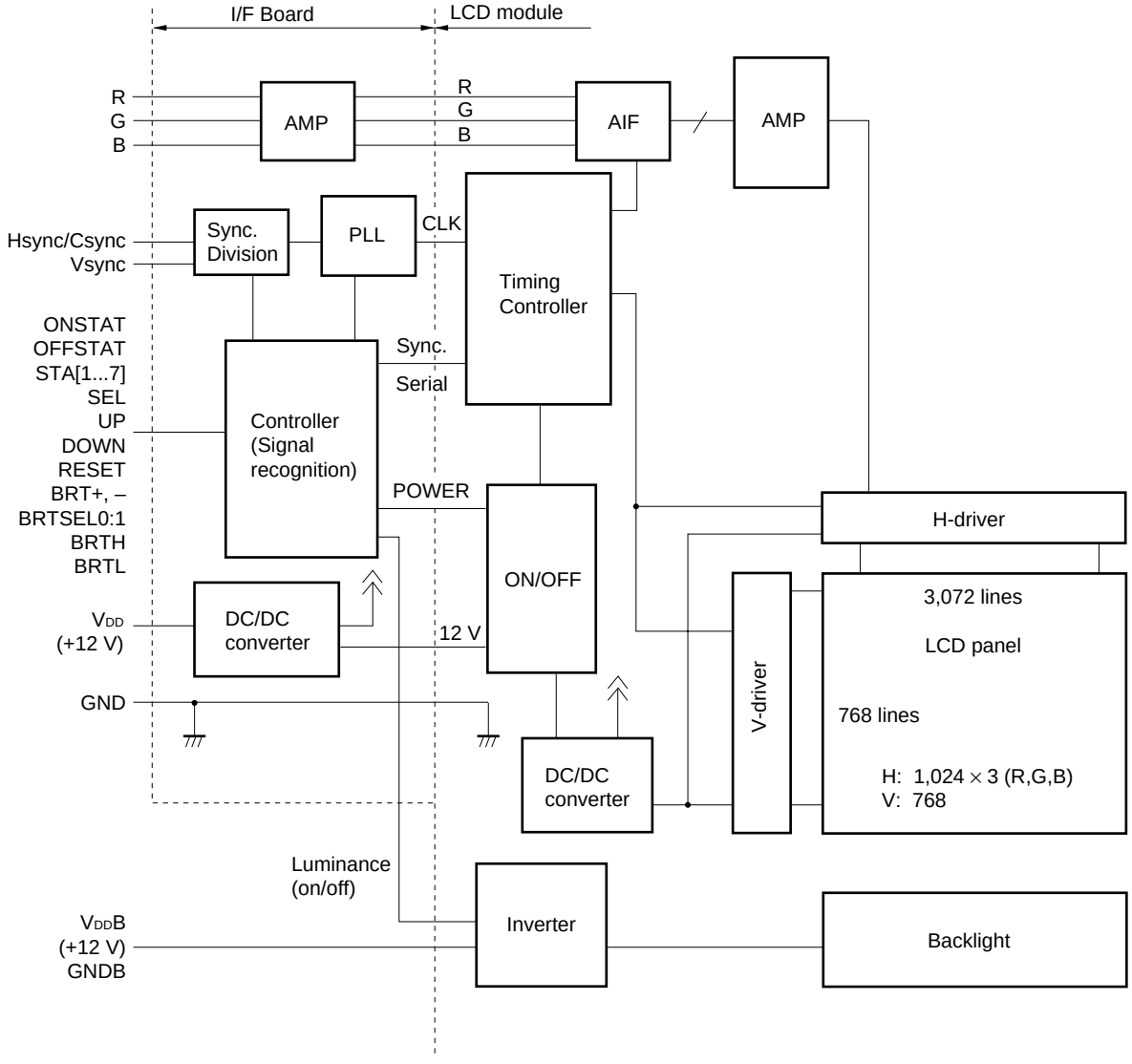
STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

BLOCK DIAGRAM



Remark Frame is not connected to GND and GNDB.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	285.696 (H) × 214.272 (V) mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1,024 × 768 pixels
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.279 (H) × 0.279 (V) mm
Module size	330.0 (H) × 255.0 (V) × 19.0 (TYP.) (D) mm
Weight	1,320 g (TYP.)
Contrast ratio	150 : 1 (TYP.)
Viewing angle (more than the contrast ratio of 10 : 1)	
	Horizontal : 50° (TYP., left side, right side)
	Vertical : 15° (TYP., up side), 30° (TYP., down side)
Designed viewing direction	Wider viewing angle with contrast ratio : down side (6 o'clock)
	Wider viewing angle without image reversal : up side (12 o'clock)
	Optimum grayscale (γ = 2.2) : down side 5° (TYP.)
Color gamut	35% (TYP., center, to NTSC)
Response time	15 ms (TYP.), white to black
Luminance	200 cd/m^2 (TYP.)
Signal system	Analog RGB signals, Synchronous signals (Hsync and Vsync or Composit)
Supply voltages	12 V (Logic/LCD driving), 12 V (Backlight)
Backlight	Edge light type, two cold cathode fluorescent lamps with an inverter
Power consumption	17.5 W (TYP.)

GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	330.0 ± 0.5 (H) × 255.0 ± 0.5 (V) × 20.0 (MAX.) (D)	mm
Display area	285.696 (H) × 214.272 (V)	mm
Number of dots	1,024 × 3 (H) × 768 (V)	dot
Number of pixels	1,024 (H) × 768 (V)	pixel
Dot pitch	0.093 (H) × 0.279 (V)	mm
Pixel pitch	0.279 (H) × 0.279 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	–
Display colors	full color	color
Weight	1,380 (MAX.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks	
Supply voltage	V_{DD}	–0.3 to +14	V	T_a = 25°C	
	$V_{DD}B$	–0.3 to +14	V		
Logic input voltage	V_{IN1}	–0.3 to +5.5	V	T_a = 25°C V_{DD} = 12 V	
R,G,B input voltage	V_{IN2}	–4.0 to +4.0	V		
BRTL input voltage	V_{IN4}	–0.3 to +1.5	V		
Storage temp.	T_{ST}	–20 to + 60	°C	–	
Operating temp.	T_{OP}	0 to 50	°C	Module surface **Note**	
Humidity	–	≤ 95% relative humidity	–	T_a ≤ 40°C	No condensation
	–	≤ 85% relative humidity	–	40 < T_a ≤ 50°C	
	–	≤ (T_A = 50°C, 85 % relative humidity) Absolute humidity	–	T_a > 50°C	

Note Measured at the display area

ELECTRICAL CHARACTERISTICS

T_a = 25°C

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply voltage	$V_{DD}B$	11.4	12.0	12.6	V	for backlight
	V_{DD}	11.4	12.0	12.6	V	for logic and LCD driving
Logic input Low voltage	V_{IL}	0	–	0.8	V	Hsync/Csync, Vsync, UP, DOWN, RESET, SEL, BRTSEL0, 1, BRT+, BRT–, DDCCLK, DDCDAT, WPRT
Logic input High voltage	V_{IH}	2.2	–	5.25	V	
Logic output Low voltage 1	V_{OL1}	–	–	0.4	V	CNTCLK, CNTDAT, CNTSTB, DDCDAT
Logic output High voltage 1	V_{OH1}	2.4	–	–	V	
Logic output Low current 1	I_{OL1}	–	–	1	mA	CNTCLK, CNTDAT, CNTSTB
Logic output High current 1	I_{OH1}	–1	–	–	mA	
Logic output High current 2	I_{OH2}	–	–	50	mA	STA1-STA8, ONSTAT, OFFSTAT, V_{OH} = 4.45 V
Logic output Low current 3	I_{OL3}	–	–	3	mA	DDCDAT
Logic output High current 3	I_{OH3}	–1	–	–	mA	
Maximum amplitude (white-black)	V_{IRGB}	0 (black)	–	0.7 (white)	Vp-p	RGB input
DC input level (black)	V_{IDCRGB}	–0.5	–	+2.5	V	
Supply current **Note**	$I_{DD}B$	–	710	900	mA	$V_{DD}B$ = 12.0 V (MAX. Luminance)
	I_{DD}	–	750	1100	mA	V_{DD} = 12.0 V
	$I_{DD}B$	–	1	10	mA	Power saving mode, $V_{DD}B$ = 12.0 V
	I_{DD}	–	60	300	mA	Power saving mode, V_{DD} = 12.0 V

Note Checkered flag pattern

SUPPLY VOLTAGE SEQUENCE

(1) Power supply sequence

This module does not have the power supply sequence.
The supply voltage must not be applied while the control signals (SEL, UP, DOWN, RESET, BRT+ and BRT–) are connected to GND. Otherwise the module may cause malfunction.

(2) Ripple of supply voltage

	V_{DD} (for logic and LCD driver)	$V_{DD}B$ (for backlight)
Acceptable range	≤ 100 mVp-p	≤ 200 mVp-p

Remark The acceptable range of ripple voltage includes spike noise.

INTERFACE PIN CONNECTION

(1) Interface signals, power supply

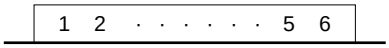
CN101

Part No. : MRF03-6R-SMT
Adaptable socket : MRF03-2 × 6P-1.27 (For cable type) or MRF03-6PR-SMT (For board to board type)
Supplier : HIROSE ELECTRIC CO., LTD. (coaxial type)

Remark A coaxial cable shield should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync/Csync
3	R	6	N.C. **Note**

Figure from socket view



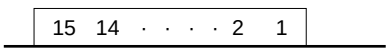
Note N.C. (No connection) should be open.

CN102

Part No. : IL-Z-15PL1-SMTY
Adaptable socket : IL-Z-15S-S125C3
Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	SEL	9	GND
2	UP	10	BRT+
3	DOWN	11	BRT–
4	RESET	12	GND
5	GND	13	BRTSEL0
6	CNTCLK	14	BRTSEL1
7	CNTDAT	15	GND
8	CNTSTB		

Figure from socket view



CN103

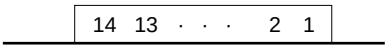
Part No. : IL-Z-14PL1-SMTY

Adaptable socket : IL-Z-14S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GND	8	STA4
2	ONSTAT	9	GND
3	OFFSTAT	10	STA5
4	GND	11	STA6
5	STA1	12	STA7
6	STA2	13	N.C. **Note**
7	STA3	14	GND

Figure from socket view



Note N.C. (No connection) should be open.

CN104

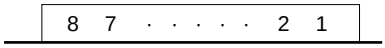
Part No. : IL-Z-8PL1-SMTY

Adaptable socket : IL-Z-8S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V_{DD}	5	GND
2	V_{DD}	6	GND
3	V_{DD}	7	GND
4	V_{DD}	8	GND

Figure from socket view



CN105

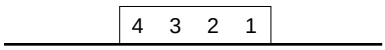
Part No. : IL-Z-4PL1-SMTY

Adaptable socket : IL-Z-4S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	DDCCLK	3	WPRT
2	DDCDAT	4	GND

Figure from socket view



CN107

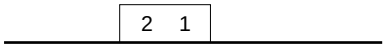
Part No. : IL-Z-2PL1-SMTY

Adaptable socket : IL-Z-2S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	BRTH **Note**	2	BRTL **Note**

Figure from socket view



Note When you do not use, these terminal should be open.

CN3

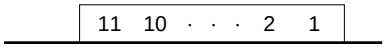
Part No. : IL-Z-11PL1-SMTY

Adaptable socket : IL-Z-11S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	V_{DD}B	7	N.C. **Note**
2	V_{DD}B	8	N.C. **Note**
3	V_{DD}B	9	N.C. **Note**
4	GNDB	10	N.C. **Note**
5	GNDB	11	N.C. **Note**
6	GNDB		

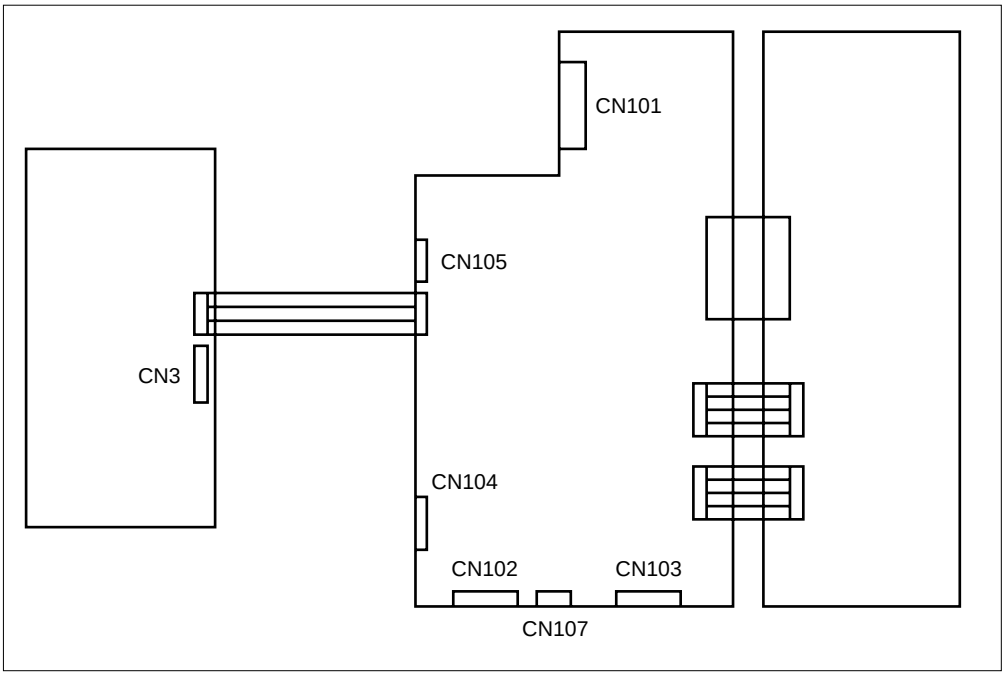
Figure from socket view



Note N.C. (No connection) should be open.

<Connector location>

Rear view



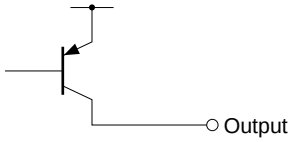
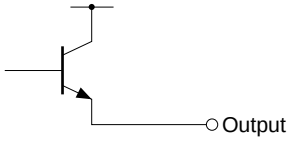
(2) Pin function

Symbol	I/O	Logic	Description
Hsync/ Csync	Input	Positive Negative	Horizontal synchronous signal input or composite synchronous signal input (TTL level), Positive/Negative auto recognition
Vsync	Input	Positive Negative	Vertical synchronous signal input (TTL level) Positive/Negative auto recognition
R	Input	–	Red video signal input (0.7 Vp-p, 75 Ω)
G	Input	–	Green video signal input (0.7 Vp-p, 75 Ω)
B	Input	–	Blue video signal input (0.7 Vp-p, 75 Ω)
SEL	Input	Negative	Control function select signal (TTL level) SEL is pulled up in the module. Detail of the functions are mentioned in **CONTROL FUNCTIONS**. High or open: SEL off, Low: SEL on
UP	Input	Negative	Control signal (TTL level) The signal increases the value of the functions selected. UP is pulled up in tha module. High or open: UP off, Low: UP on
DOWN	Input	Negative	Control signal (TTL level) The signal decreases the value of the functions selected. DOWN is pulled up in the module. High or open: DOWN off, Low : Down on
RESET	Input	Negative	Control signal (TTL level) The signal initializes the selected function. RESET is pulled up in the module. High or open: RESET off, Low: RESET on
BRT+	Input	Negative	Control signal (TTL level) The signal increases the luminance value. BRT+ is pulled up in the module. High or open: BRT+ off, Low: BRT+ on
BRT–	Input	Negative	Control signal (TTL level) The signal decreases the luminance value. BRT– is pulled up in the module. High or open: BRT– off, Low: BRT– on
BRTSEL0 BRTSEL1	Input	Negative	Luminance control select signal (TTL level) The signals determines how to control the luminance. Detail of the functions are mentioned in **CONTROL FUNCTIONS**.
CNTCLK	Output	Positive	CLK for display control (TTL level) Detail of CNTCLK is mentioned in **STATUS READ FUNCTIONS**.
CNTDAT	Output	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **STATUS READ FUNCTIONS**.
CNTSTB	Output	Positive	Latch pulse for display control (TTL level) Detail of CNTSTB is mentioned in **STATUS READ FUNCTIONS**.
ONSTAT	Output	Positive	Power status signal High: Normal operation, Low: Other status
OFFSTAT	Output	Positive	Power status signal High: Power saving, Low: Other status
STA1	Output	Positive	Indicator for luminance control High: Luminance select, Low: Other status
STA2	Output	Positive	Indicator for horizontal total count High: Horizontal total count select, Low: Other status

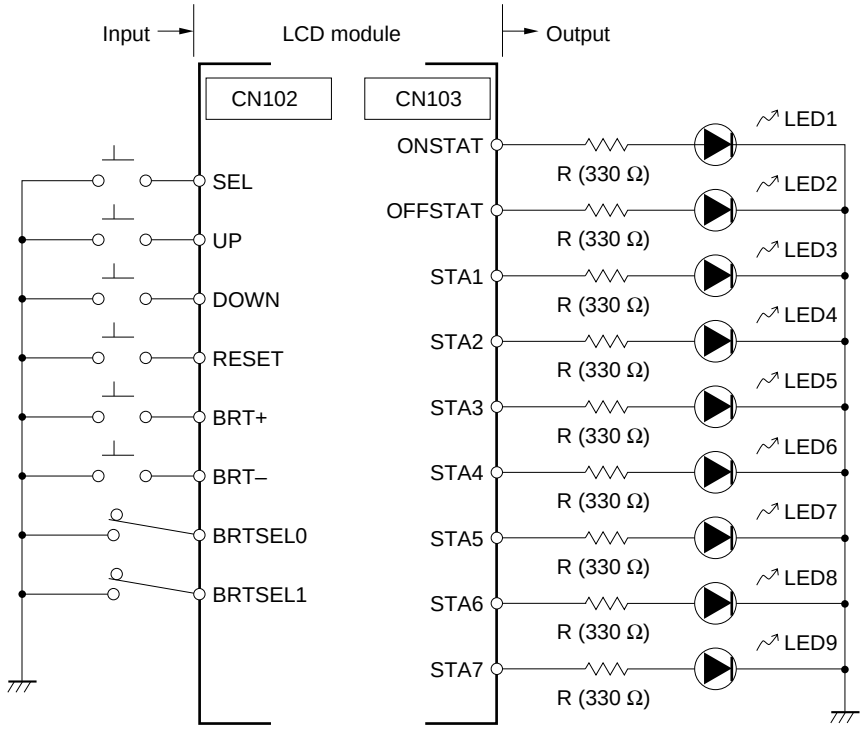
Symbol	I/O	Logic	Description
STA3	Output	Positive	Indicator for CLK delay High: CLK delay select, Low: Other status
STA4	Output	Positive	Indicator for vertical position High: Vertical position select, Low: Other status
STA5	Output	Positive	Indicator for horizontal position High: Horizontal position select, Low: Other status
STA6	Output	Positive	Indicator for initialization High: Reset select, Low: Other status
STA7	Output	Positive	Reserved
DDCCLK	Input	Positive	CLK for DDC
DDCDAT	Input /output	Positive	Data for DDC Read/Write
WPRT	Input	Positive	Select signal for DDC High or open: Reading mode, Low: Writing mode
BRTH	Input	–	Luminance control signal with variable resistor (TTL level) Detail of the control is mentioned in **CONTROL FUNCTIONS**.
BRTL			
V_{DD}	–	–	Power supply for Logic and LCD driving +12 V (±5 %)
$V_{DD}B$	–	–	Power supply for backlight. +12 V (±5 %)
GND	–	–	Ground for system.
GNDB	–	–	Ground for backlight.

Remark Frame ground, system ground and backlight ground are not connected into the module.

(3) Equivalent circuit

Symbol	I/O	Equivalent circuit
ONSTAT	Output	
OFFSTAT	Output	
STA1	Output	 Product: Rohm DTC143ZUA or equivalent
STA2	Output	
STA3	Output	
STA4	Output	
STA5	Output	
STA6	Output	
STA7	Output	

<Recommendation circuit diagram>



Remark LED1: Normal operation, LED2: Power saving, LED3: Luminance select, LED4: Horizontal total count select, LED5: CLK delay select, LED6: Vertical position select, LED7: Horizontal position select, LED8: Reset select

INPUT SYNCHRONOUS SIGNAL

This module can recognize the synchronous signals automatically as follows.

Auto recognition mode	Input Synchronous signal (CN101: 4 and 5 pins)		Output STAT signal (CN103: 2 and 3 pins)	
	Hsync/Csync	Vsync	ON STAT	OFF STAT
Separate synchronous signal mode (Hsync, Vsync)	Input	Input	H	L
Composite synchronous signal mode	Input	No input	H	L
Power save mode **Note**	No input	No input	L	H

Note Power save mode corresponds to VESA™, DPMS™.

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CONTROL FUNCTIONS

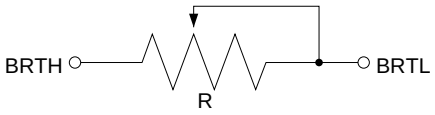
This module needs to adjust the next 4 items according to the using condition, environment temperature, and the input signal timing etc.

- Luminance: This function controls luminance.
- Horizontal total count:
  This function controls the horizontal total count. If the display is un-uniformity, should adjust this function using the display with the vertical stripe pattern (white line and black line).
- CLK delay: CLK delay should be adjusted when the contour of character fails.
- Display position (Horizontal and vertical):
  This function controls horizontal and vertical display position. The display position should be adjusted in the center of the screen.

(1) Luminance control

BRTSEL0	BRTSEL1	Function
L	L	Luminance can be controlled by BRT+ or BRT– signal.
L	H	Luminance is selected by SEL signal. And luminance can be controlled by UP or DOWN signal.
H	L	Luminance can be controlled by UP or DOWN signal without selecting SEL.
H	H	The variable resistor should connect to CN107. **Note**

Note The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor correspond to the minimum of luminance.



Maximum luminance (100%) : R = 10 kΩ
Minimum luminance (30%) : R = 0 Ω

Mating variable resistor: 10 kΩ ±5%, B curve

Remark Above settings should be done before the power switches on.

(2) Flow chart of control function

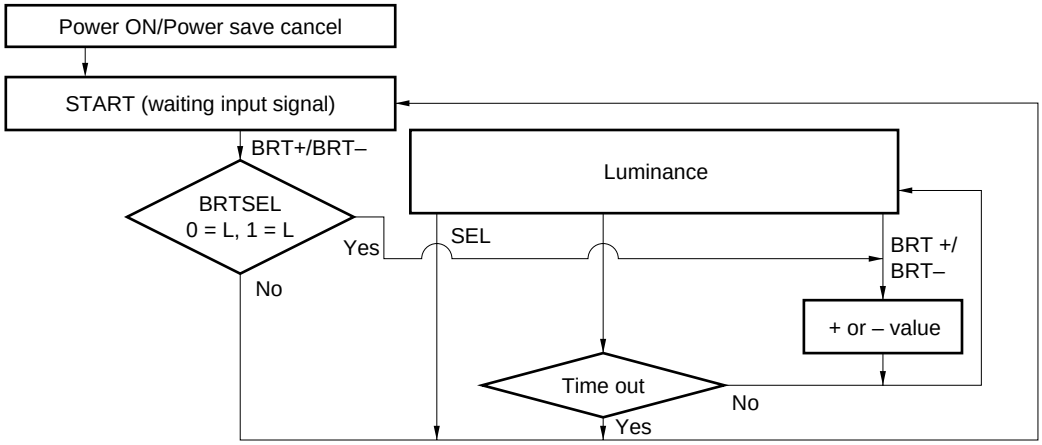
Each selected value is memorized into LCD memory after SEL signal input or time out. The memorized value are not affected even if a selected mode is changed another one or power is turned off. But the selected value is not memorized in case that a selected mode is changed another one before time out or power is turned off before time out.

This function does not work in the power save mode.

- If the input period of a signal is short, LCD memory may not accept the selected signal.
- The value of selected input signals (UP, DOWN, BRT+, BRT–) is continuously incremented if the input signal is held more than approx. one second.
- Each RESET signal initializes only the memorized input signal. RESET signal in All reset mode (STA6 = High) initializes all memorized input signal. RESET signal should be hold more than approx. two seconds.
- No input signals more than five seconds shall be regarded “Time out”.
- STA signals which do not mention should set STA = Low up.

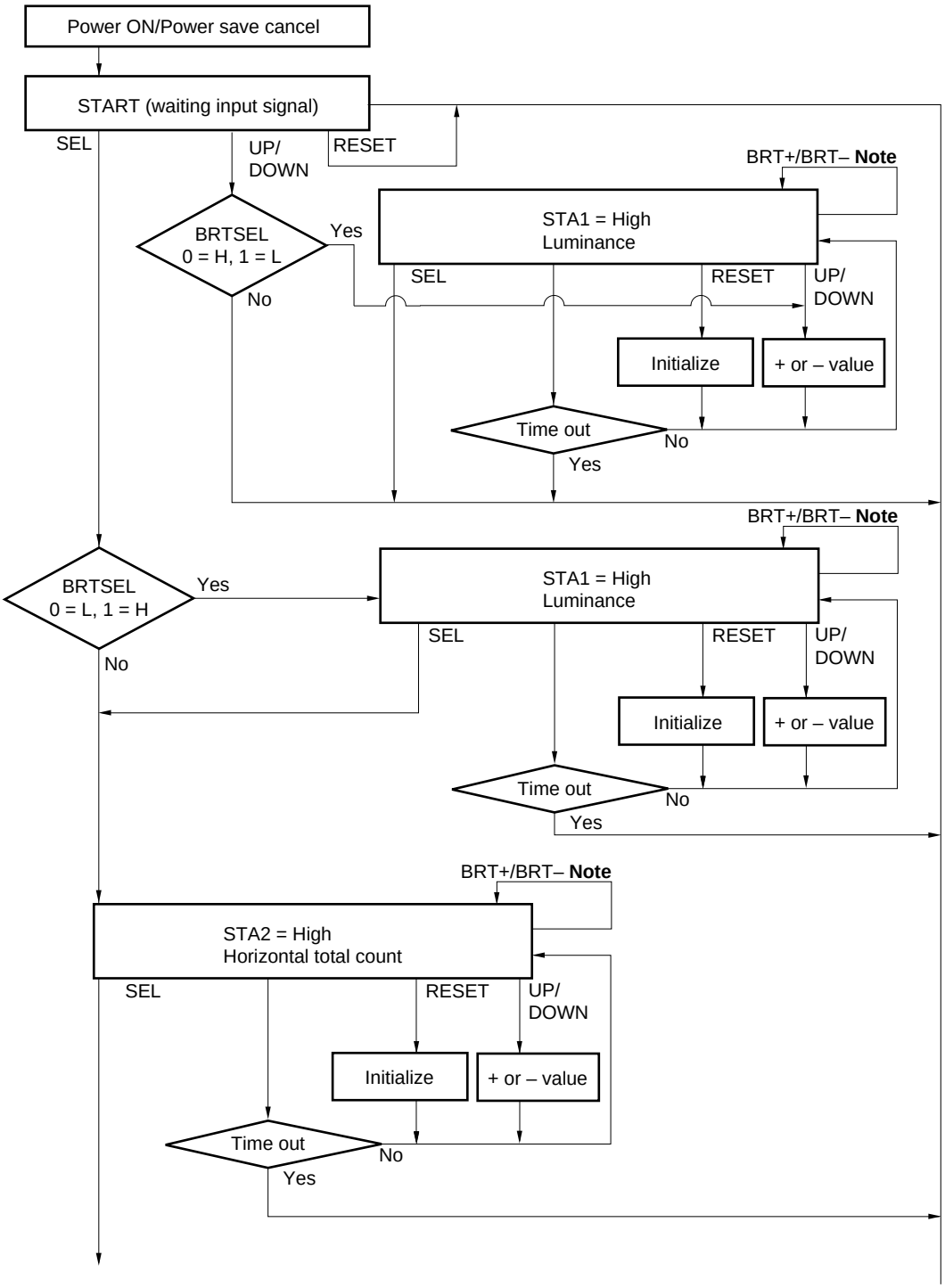
<Flow Chart 1>

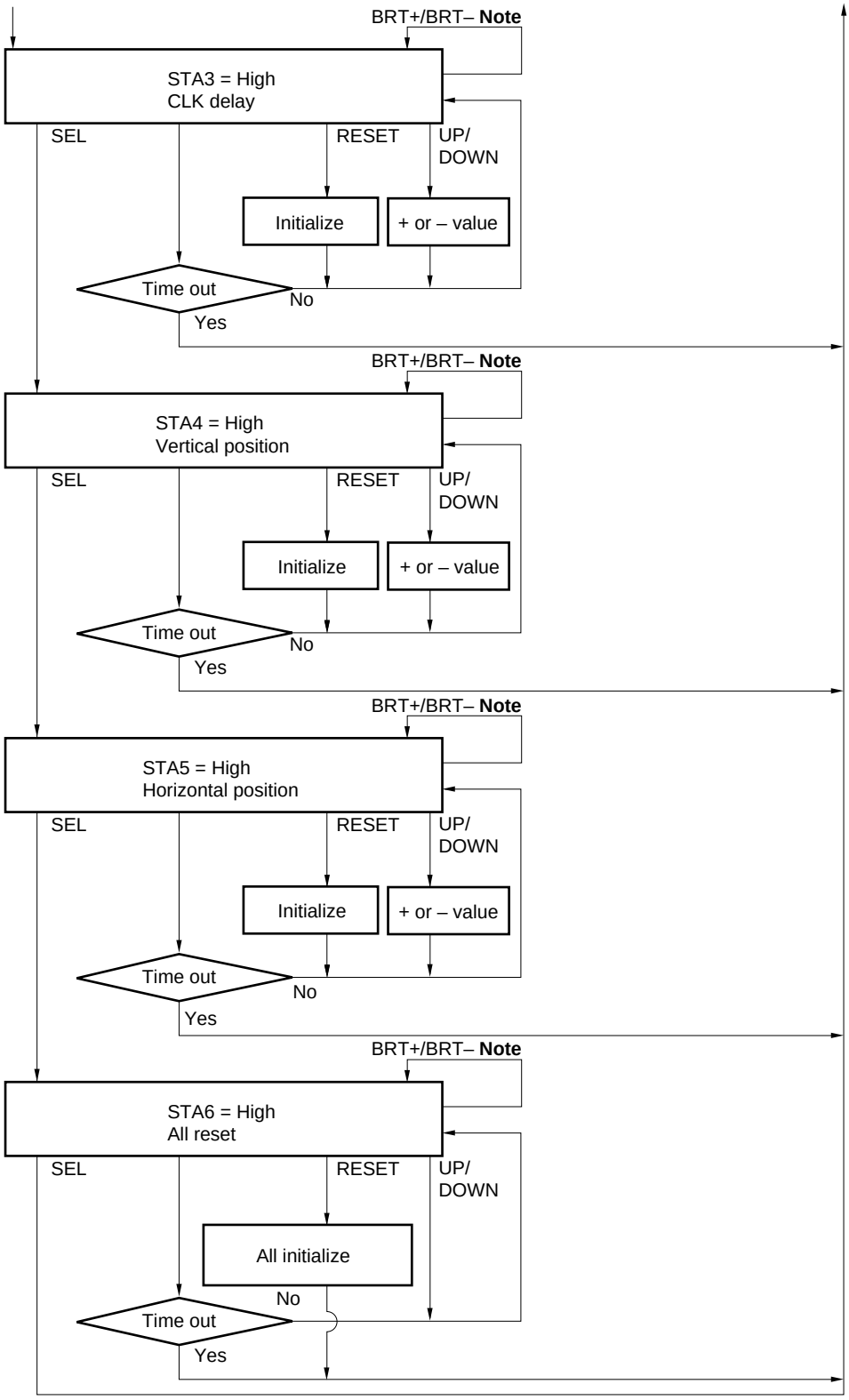
Flow chart of control way for BRT+ and BRT–



<Flow chart 2>

Flow chart of control way for SEL, UP, DOWN and RESET





Note Refer to <Flow chart 1>.

DDC FUNCTION

The usage of this function is based on VESA™, DDC™ and EDID™.

- Writing mode: WPRT = Low
- Reading mode: WPRT = High or Open

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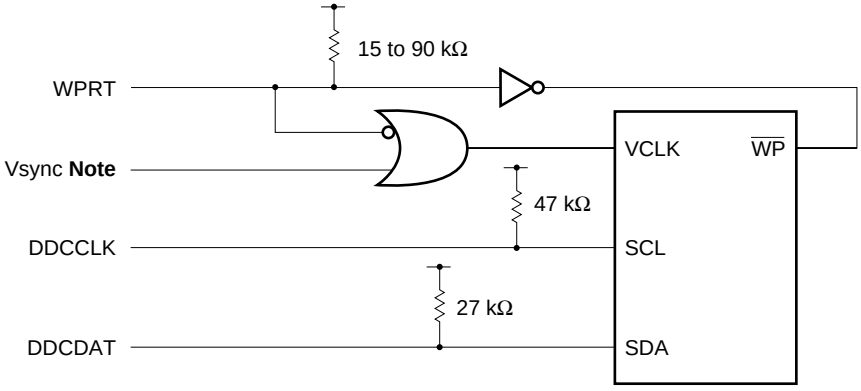
Please write data into necessary addresses in advance, when you use this function. Data “55H” is set in the address “00H” when the module is shipped. The input equivalent circuit diagram is as follows.



Product: Microchip
24LCS21 or equivalent

Note In the case of CS signal input, use Vsync that generated inside a module.

STATUS READ FUNCTIONS

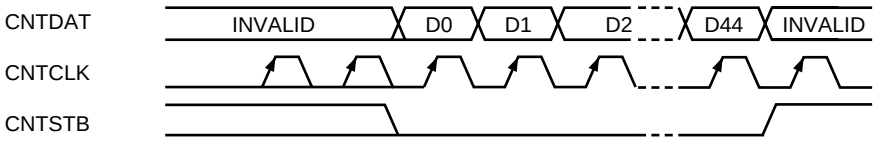
This LCD module can be monitored serial data of following functions (See **CNTDAT COMPOSITION**)

(1) Expansion mode : See **table 1** and **EXPANSION FUNCTION**
(2) Display position control (Vertical) : See **table 2**
(3) Display position control (Horizontal): See **table 5**
(4) CLK delay control : See **table 3**
(5) CLK fall/rise synchronous change : See **table 4**
(6) CLK counts of horizontal period : See **table 6**
(7) CLK frequency range : See **table 7**

SERIAL COMMUNICATION TIMING AND WAVEFORM

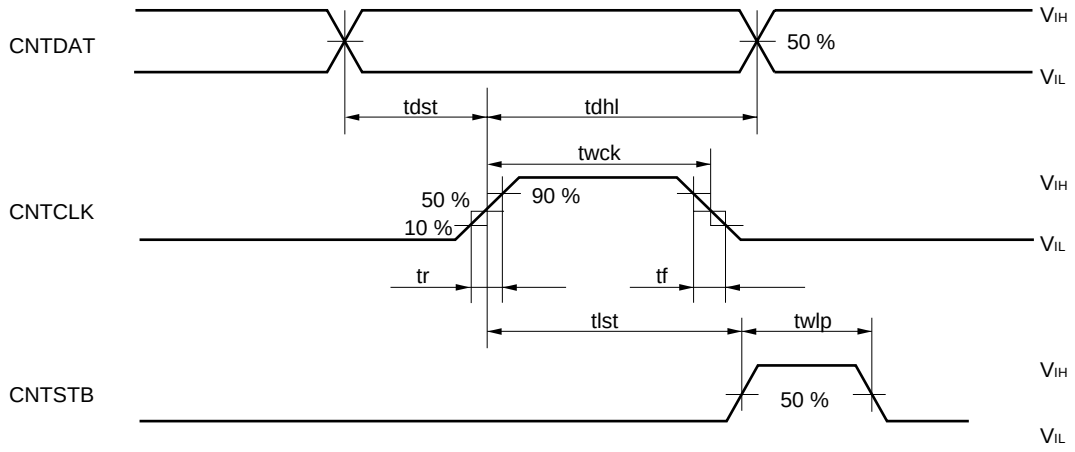
This LCD module can be read the following status data.

Serial Communication Timing



Parameter	Symbol	MIN.	MAX.	Unit	Remark
CLK pulse-width	twck	350	–	ns	CNTCLK
CLK frequency	fclk	–	1.25	MHz	
DATA set-up-time	tdst	50	–	ns	CNTDAT (C = 100 pF)
DATA hold-time	tdhl	350	–	ns	
Latch pulse-width	twlp	8	–	μs	CNTSTB
Latch set-up time	tlst	1.2	–	μs	
Rise/fall time	tr, tf	–	50	ns	CNT xxx

Serial Communication Waveform



CNTDAT COMPOSITION

DATA	DATA name	Function	Remark
D0	VEX3	Expansion mode	See **table 1**.
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Display position control (Vertical) (MSB)	See **table 2**.
D5	VD9	Display position control (Vertical)	
D6	VD8	Display position control (Vertical)	
D7	VD7	Display position control (Vertical)	
D8	VD6	Display position control (Vertical)	
D9	VD5	Display position control (Vertical)	
D10	VD4	Display position control (Vertical)	
D11	VD3	Display position control (Vertical)	
D12	VD2	Display position control (Vertical)	
D13	VD1	Display position control (Vertical)	
D14	VD0	Display position control (Vertical) (LSB)	
D15	DELAY6	CLK delay control (MSB)	See **table 3**.
D16	DELAY5	CLK delay control	
D17	DELAY4	CLK delay control	
D18	DELAY3	CLK delay control	
D19	DELAY2	CLK delay control	
D20	DELAY1	CLK delay control	
D21	DELAY0	CLK delay control (LSB)	
D22	CKS	CLK fall/rise synchronous charge	See **table 4**.
D23	HD8	Display position control (Horizontal) (MSB)	See **table 5**.
D24	HD7	Display position control (Horizontal)	
D25	HD6	Display position control (Horizontal)	
D26	HD5	Display position control (Horizontal)	
D27	HD4	Display position control (Horizontal)	
D28	HD3	Display position control (Horizontal)	
D29	HD2	Display position control (Horizontal)	
D30	HD1	Display position control (Horizontal)	
D31	HD0	Display position control (Horizontal) (LSB)	
D32	HSE10	CLK counts of horizontal period (MSB)	See **table 6**.
D33	HSE9	CLK counts of horizontal period	
D34	HSE8	CLK counts of horizontal period	
D35	HSE7	CLK counts of horizontal period	
D36	HSE6	CLK counts of horizontal period	
D37	HSE5	CLK counts of horizontal period	
D38	HSE4	CLK counts of horizontal period	
D39	HSE3	CLK counts of horizontal period	
D40	HSE2	CLK counts of horizontal period	
D41	HSE1	CLK counts of horizontal period	
D42	HSE0	CLK counts of horizontal period (LSB)	
D43	MOD1	CLK frequency range	See **table 7**.
D44	MOD0	CLK frequency range	

Table 1. Expansion mode (VEX3 to VEX0: 4 bits)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	XGA	Standard **Note**
0	0	0	1	1.25	SVGA	See **Expansion Function (3) Display Image**.
0	0	1	0	1.6	PC98, VGA, VGAtext	
0	0	1	1	–	Prohibit	
0	1	0	0	–	Prohibit	
0	1	0	1	–	Prohibit	
0	1	1	0	–	Prohibit	
0	1	1	1	–	Prohibit	
1	0	0	0	–	Prohibit	
1	0	0	1	1.2	832 × 624 (MAC)	
1	0	1	0	–	Prohibit	
1	0	1	1	–	Prohibit	
1	1	0	0	–	Prohibit	
1	1	0	1	–	Prohibit	
1	1	1	0	–	Prohibit	
1	1	1	1	–	Prohibit	

Note The number of horizontal line from tail of Vsync to head of Video signal.

Table 2. Display position control (Vertical) (VD10 to VD0: 11 bits)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] **Note 1**
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 **Note 2**

Notes 1. The number of horizontal line from tail of Vsync to head of Video signal.

2. The maximum number is based on horizontal line count of the display mode.

Table 3. CLK delay control (DELAY6 to DELAY0: 7 bits)

DELAY [6..0]	Delay Note	Unit
00H	7.0	ns
01H	7.6	ns
02H	8.2	ns
03H	8.8	ns
04H	9.4	ns
05H	10.0	ns
06H	10.5	ns
07H	11.2	ns
08H	11.8	ns
09H	12.4	ns
0AH	13.0	ns
0BH	13.7	ns
0CH	14.2	ns
0DH	14.8	ns
0EH	15.3	ns
0FH	15.9	ns
10H	16.6	ns
11H	17.2	ns
12H	17.8	ns
13H	18.4	ns
14H	18.9	ns
15H	19.5	ns
16H	20.1	ns
17H	20.7	ns
18H	21.4	ns
19H	22.0	ns
1AH	22.6	ns
1BH	23.2	ns
1CH	23.8	ns
1DH	24.4	ns
1EH	24.9	ns
1FH	25.6	ns
20H	26.3	ns
21H	26.9	ns
22H	27.4	ns
23H	28.1	ns
24H	28.5	ns
25H	29.1	ns
26H	29.7	ns
27H	30.3	ns
28H	31.0	ns
29H	31.6	ns
2AH	32.2	ns
2BH	32.8	ns
2CH	33.3	ns
2DH	33.9	ns
2EH	33.4	ns
2FH	35.1	ns
30H	35.6	ns
31H	36.1	ns
32H	36.8	ns
33H	37.5	ns
34H	37.9	ns
35H	38.5	ns
36H	39.1	ns
37H	39.7	ns
38H	40.4	ns
39H	41.0	ns
3AH	41.5	ns
3BH	42.1	ns
3CH	42.6	ns
3DH	43.2	ns
3EH	43.8	ns
3FH	44.4	ns
40H	45.0	ns
41H	45.6	ns
42H	46.2	ns
43H	46.8	ns
44H	47.3	ns
45H	47.8	ns
46H	48.4	ns
47H	49.0	ns
48H	49.6	ns
49H	50.2	ns
4AH	50.8	ns
4BH	51.4	ns
4CH	51.9	ns
4DH	52.6	ns
4EH	53.1	ns
4FH	53.7	ns
50H	54.5	ns
51H	55.0	ns
52H	55.6	ns
53H	56.3	ns
54H	56.8	ns
55H	57.4	ns
56H	57.9	ns
57H	58.5	ns
58H	59.2	ns
59H	59.8	ns
5AH	60.4	ns
5BH	61.1	ns
5CH	61.6	ns
5DH	62.2	ns
5EH	62.7	ns
5FH	63.3	ns
60H	64.0	ns
61H	64.7	ns
62H	65.3	ns
63H	66.0	ns
64H	66.5	ns
65H	67.1	ns
66H	67.7	ns
67H	68.3	ns
68H	68.9	ns
69H	69.5	ns
6AH	70.1	ns
6BH	70.7	ns
6CH	71.2	ns
6DH	71.9	ns
6EH	72.4	ns
6FH	73.1	ns
70H	73.6	ns
71H	74.2	ns
72H	74.8	ns
73H	75.4	ns
74H	75.9	ns
75H	76.5	ns
76H	77.0	ns
77H	77.7	ns
78H	78.3	ns
79H	79.0	ns
7AH	79.6	ns
7BH	80.2	ns
7CH	80.8	ns
7DH	81.4	ns
7EH	81.9	ns
7FH	82.5	ns

Note This delay value is typical value at T_a = 25°C. And the value varies by the ambient temperature and the module itself.

Please set up a preferable display position. See the following references.

<1> Variation of CLK delay by temperature drift (for reference). The temperature constant of CLK delay is 0.2 %/°C.

Calculated example:

In case of delay time is 20 ns at T_a = 25°C;

(a) In case T_a rising to 50°C.

Increase of delay time → (50°C – 25°C) × 0.002 × 20 ns = 1 ns

So, the total delay time is 21 ns at T_a = 50°C.

(b) In case T_a falling to 0°C.

Decrease of delay time → (0°C – 25°C) × 0.002 × 20 ns = –1 ns

So, the total delay time is 19 ns at T_a = 0°C.

<2> Variation of CLK delay time against each LCD module (for reference).

–10.5 % to +14.4 %

	MOD setting			
	0,0	0,1	1,0	1,1
The upper limit of CLK delay: DELAY [6..0]	Prohibit	59H	6BH	7FH

Table 4. Clock fall/rise synchronous change

CKS	Function
0 (fixed)	DATA is sampled on rising edge of CLK 

Table 5. Display position control (Horizontal) (HD8 to HD0: 9 bits)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] **Note**
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Note The number of dot clock from tail of Hsync to head of Video signal.

Table 6. CLK counts of horizontal period (HSE10 to HSE0: 11 bits)

HSE10	HSE 9	HSE 8	HSE 7	HSE 6	HSE 5	HSE 4	HSE 3	HSE 2	HSE 1	HSE 0	CLK count **Note**
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Note The number of CLK between Hsync signals.

In the case of the setting value and the actual input signal differ, it becomes the cause of a wrong action.

Table 7. CLK frequency range (MOD1 to MOD0: 2 bits)

MOD1	MOD0	CLK frequency [MHz]
0	0	Prohibit
0	1	65 to 79
1	0	50 to 65
1	1	20 to 50

EXPANSION FUNCTION

(1) Expansion mode

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can be expanded to 1.6 times vertically and horizontally,VGA screen image can be displayed fully on the screen of XGA resolution.

This LCD module has this function mentioned in the followings.

Please adopt this mode after evaluating display quality, because the appearance in the expansion mode is happened to become bad in some cases.

The followings show the display magnifications in each mode.

Input display	Number of pixels	Magnification	
		Vertical **Note**	Horizontal **Note**
XGA	1024 × 768	1	1
SVGA	800 × 600	1.25	1.25
VGA	640 × 480	1.6	1.6
VGA text	720 × 400	1.6	1.42
PC9801	640 × 400	1.6	1.6
MAC	832 × 624	1.2	1.2

Note The horizontal magnification multiples the input clock (CLK).
Input CLK = system CLK × horizontal magnification.

Example In case of XGA and VGA, CLK frequency can be decided as follows.
XGA: (system CLK (65 MHz)) × 1.0 = 65 MHz.
VGA: (system CLK (25.175 MHz)) × 1.6 = 40.28 MHz.

(2) Auto recognition data

Input signal													
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal					Vertical				
				Front Porch [CLK]	Pulse width [CLK]	Back porch [CLK]	Count num. [CLK]	P/N **Note**	Front porch [H]	Pulse width [H]	Back porch [H]	Count num. [H]	P/N **Note**
XGA (1024 × 768)	65	48.363	60.004	24	136	160	1344	N	3	6	29	806	N
	75	56.476	70.069	24	136	144	1328	N	3	6	29	806	N
	78.75	60.023	75.029	16	96	176	1312	N	1	3	28	800	N
MAC (832 × 624)	57.283	49.725	74.5	32	64	224	1152	N	1	3	39	667	N
SVGA (800 × 600)	36	35.156	56.25	24	72	128	1024	P	1	2	22	625	P
	40	37.879	60.317	40	128	88	1056	P	1	4	23	628	P
	50	48.077	72.188	56	120	44	1040	P	37	6	23	666	P
	49.5	46.875	75.0	16	80	160	1056	P	1	3	21	625	P
VGA (640 × 480)	25.175	31.469	59.94	16	96	48	800	N	10	2	33	525	N
	31.5	37.861	72.809	24	40	128	832	N	9	3	28	520	N
	31.5	37.5	75.0	16	64	120	840	N	1	3	16	500	N
	30.24	35.0	66.667	64	64	96	864	N	3	3	39	525	N
VGA-text (720 × 400)	28.322	31.469	70.087	27	108	45	900	N	12	2	35	449	P
	35.5	37.927	85.039	36	36	144	936	N	1	3	42	446	P
PC9801 (640 × 400)	21.053	24.827	56.424	64	96	48	848	N	7	8	25	440	N

Cautions 1. Horizontal and vertical display position should be adjusted properly.

2. Mistaken or other input signal cause malfunctions.

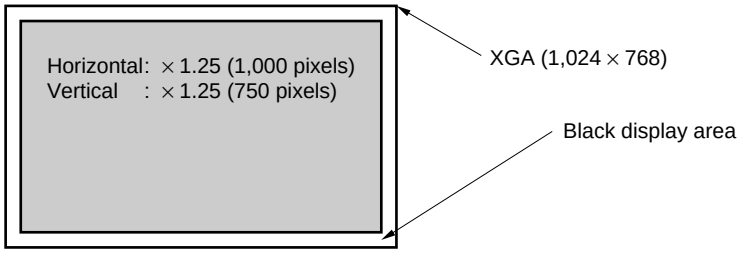
3. Any noises on RGB signals may cause the noise on the screen.

4. Even if the above timings are inputted the module correctly, any noises on Hsync and Vsync may cause un-uniformity display.

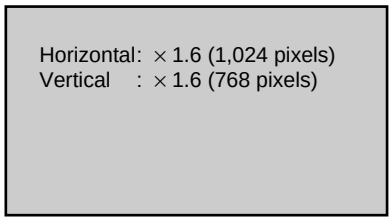
Note P/N is logic polarity of input synchronous signal.
"P": The logic is positive., "N": The logic is negative.

(3) Display Image

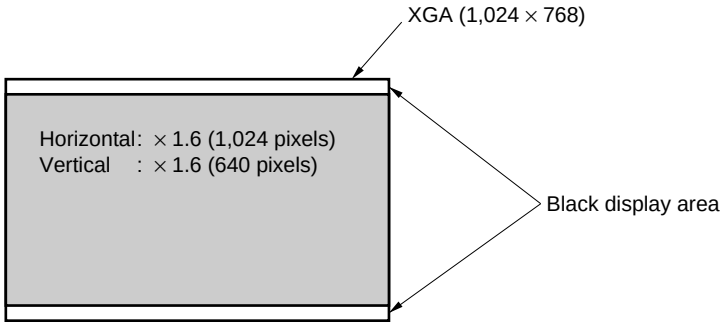
1. SVGA mode (800 × 600)



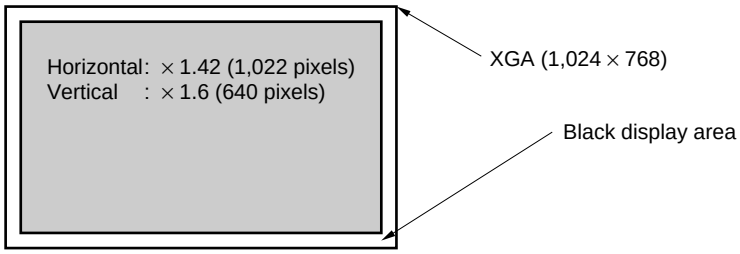
2. VGA mode (640 × 480)



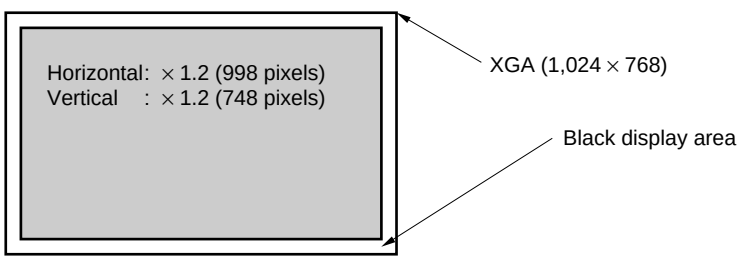
3. PC9801 mode (640 × 400)



4. VGA text mode (720 × 400)



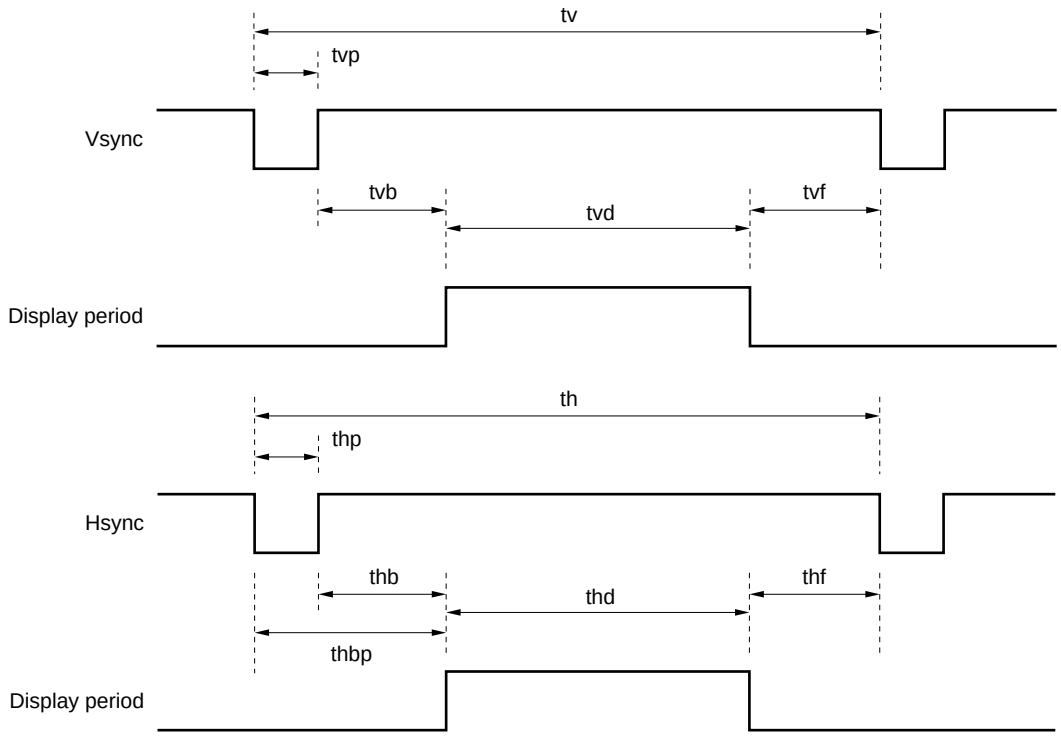
5. 832 × 624 MAC mode (832 × 624)



INPUT SIGNAL TIMING

(1) XGA Mode (Standard)

Name		Symbol	MIN.	TYP.	MAX.	Unit	Remark
Hsync	Period	th	20.47	20.677	22.33	μs	48.363 kHz (TYP.)
	Display	thd	–	15.754	–	μs	
	Front-porch	thf	–	0.369	–	μs	
	Pulse-width	thp	–	2.092	6.2	μs	
	Back-porch	thb	1.0	2.462	–	μs	
	Pulse-width +Back-porch	thbp	1.8	–	–	μs	
	Rise/Fall	thrf	–	–	10	ns	
Vsync	Period	tv	14.5 –	16.665 806	18.5 –	ms H	60.004 Hz (TYP.)
	Display	tvd	– –	15.880 768	– –	μs H	
	Front-porch	tvf	– 1	62.031 3	– –	μs H	
	Pulse-width	tvp	– 2	124.06 6	409 –	μs H	
	Back-porch	tvb	– 5	599.63 29	– –	μs H	

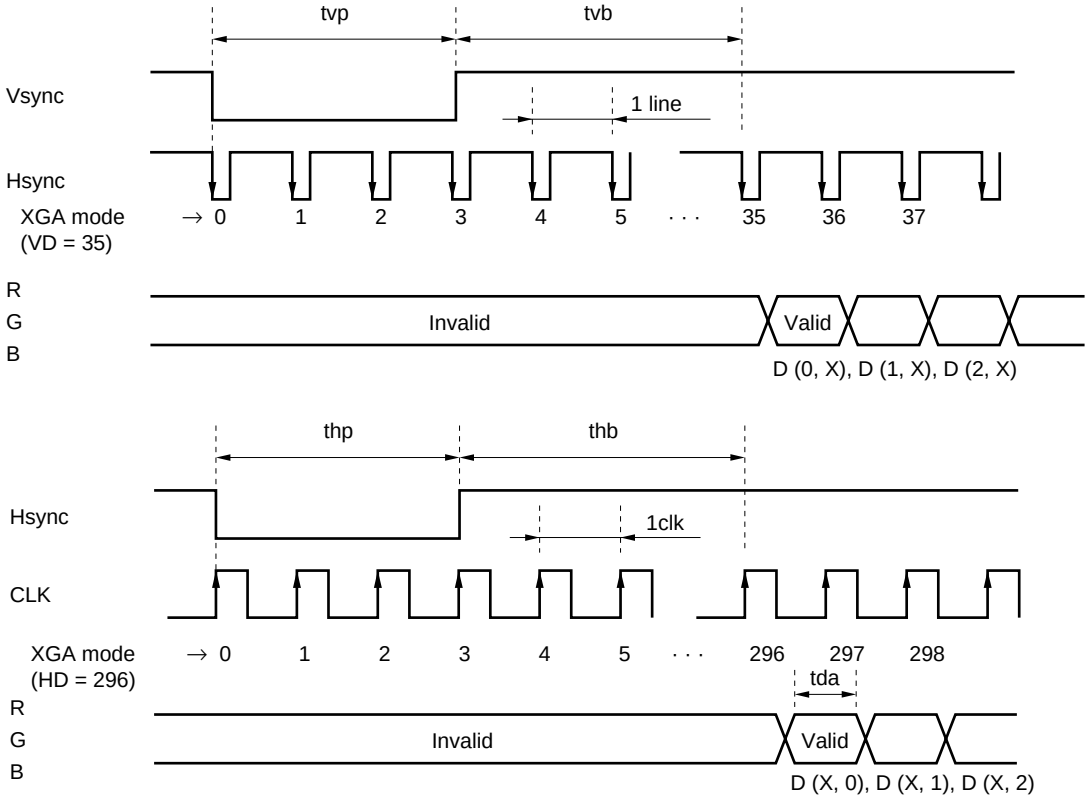


INPUT SIGNAL AND DISPLAY POSITION

(1) XGA Standard Timing

Pixels

D (0, 0)	D (0, 1)	D (0, 2)	• • •	• • •	D (0, 1023)
D (1, 0)	D (1, 1)	D (1, 2)	• • •	• • •	D (1, 1023)
D (2, 0)	D (2, 1)	D (2, 2)	• • •	• • •	D (2, 1023)
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
•	•	•	•		•
D (767, 0)	D (767, 1)	D (767, 2)	• • •	• • •	D (767, 1023)



Remark tda should be more than 4 ns.

OPTICAL CHARACTERISTICS

T_a = 25°C, V_{DD} = 12 V, $V_{DD}B$ = 12 V

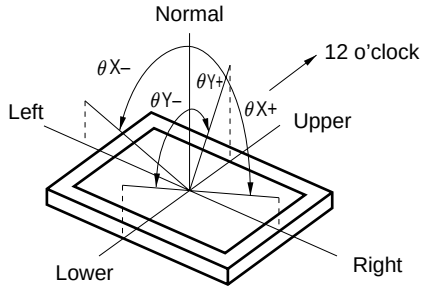
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Luminance		LVMAX	White	150	200	–	cd/m^2
Contrast ratio		CR	White/Black, at center	100	150	–	–
Viewing angle range	Horizontal	θX+	CR > 10, θY = ±0°, White/Black	30	50	–	deg.
		θX–	CR > 10, θY = ±0°, White/Black	30	50	–	deg.
	Vertical	θY+	CR > 10, θX = ±0° White/Black	10	15	–	deg.
		θY–	CR > 10, θX = ±0° White/Black	20	30	–	deg.
Color gamut		C	at center, to NTSC	35	–	–	%
Response time		ton	White to Black	–	15	–	ms
		toff	Black to White	–	18	–	
Luminance uniformity		–	$\frac{\text{Maximum luminance}}{\text{Minimum luminance}}$, White Refer to **Remark 5.**	–	–	1.30	–
Luminance control range by BRTH/BRTL		–	Maximum luminance: 100 %	–	30 to 100	–	%

Remarks 1. The contrast ratio is calculated by using the following formula.

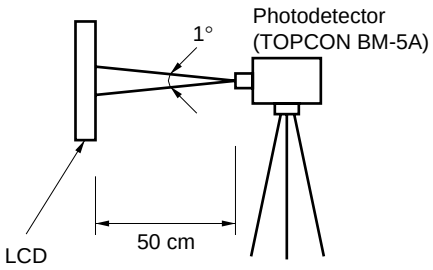
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in white}}{\text{Luminance with all pixels in black}}$$

The Luminance is measured in darkroom.

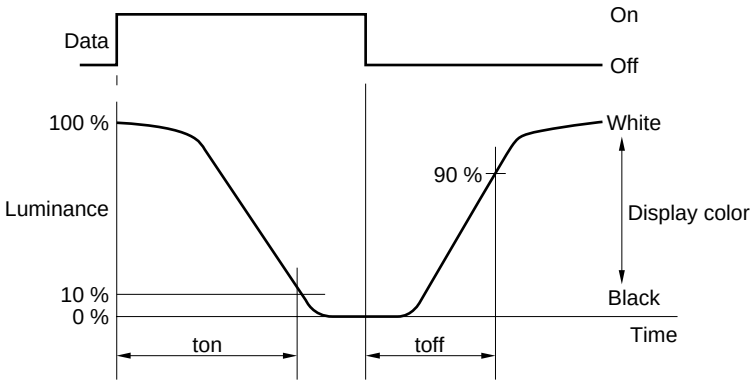
2. Definitions of viewing angle are as follows.



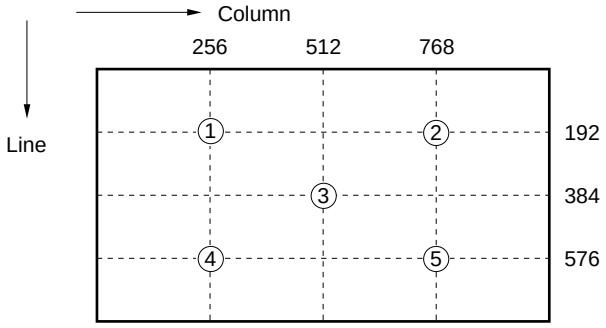
3. The luminance is measured after 20 minutes from the module works, with all pixels in white. Typical value is measured after luminance saturation.



4. Definition of response time is as follows.
Photo-detector output signal is measured when the luminance changes “white” to “black”.
Response time is the time between 100 % and 10 % of the photo-detector output amplitude.



5. The luminance is measured at near the five points shown below.



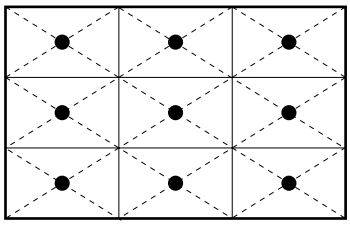
RELIABILITY TEST

Test item	Test condition
High temperature/humidity operation **Note 1**	50 ± 2°C, 85% relative humidity 240 hours Display data is black.
Heat cycle (operation) **Note 1**	<1> 0°C ± 3°C ⋯ 1 hour 55°C ± 3°C ⋯ 1 hour <2> 50 cycles, 4 hours/cycle <3> Display data is black.
Thermal shock (non-operation) **Note 1**	<1> –20°C ± 3°C ⋯ 30 minutes 60°C ± 3°C ⋯ 30 minutes <2> 100 cycles <3> Temperature transition time within 5 minutes
Vibration (non-operation) **Notes 1, 2**	<1> 5 - 100 Hz, 2G 1 minute/cycle X, Y, Z direction <2> 50 times each direction
Mechanical shock (non-operation) **Notes 1, 2**	<1> 55 G, 11 ms X, Y, Z direction <2> 3 times each direction
ESD (operation) **Notes 1, 3**	150 pF, 150 Ω, ±10 kV 9 places on a panel 10 times each place at one-second intervals
Dust (operation) **Note 1**	15 kinds of dust (JIS Z 8901) Hourly 15 seconds stir, 8 times repeat

Notes 1. Display function is checked by the same condition as LCD module out-going inspection.

2. Physical damage.

3. Discharge points "●" are shown in the figure.



GENERAL CAUTIONS

Next figures and sentence are very important. Please understand these contents as follows.

 CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate

 CAUTION

Do not touch an inverter, on which is stuck a caution label, while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module

a) Pick the pouch only, in taking out module from a carrier box.

(2) Cautions for handling the module

a) As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.

b)  As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.

c) As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.

d) Do not pull the interface connectors in or out while the LCD module is operating.

e) Put the module display side down on a horizontal plane.

f) Handle connectors and cables with care.

g) When the module is operating, do not lose CLK, Hsync or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.

h) The torque to mounting screw should never exceed 0.392 N·m (4 kgf·cm).

(3) Cautions for the atmosphere

a) Dew drop atmosphere should be avoided.

b) Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

c) This module uses cold cathod fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

d) Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

a) Do not apply fixed pattern data signal for a long time to the LCD module. It may cause image sticking. Please use screen savers if the display pattern is fixed more than one hour.

(5) Other cautions

a) Do not disassemble and/or reassemble LCD module.

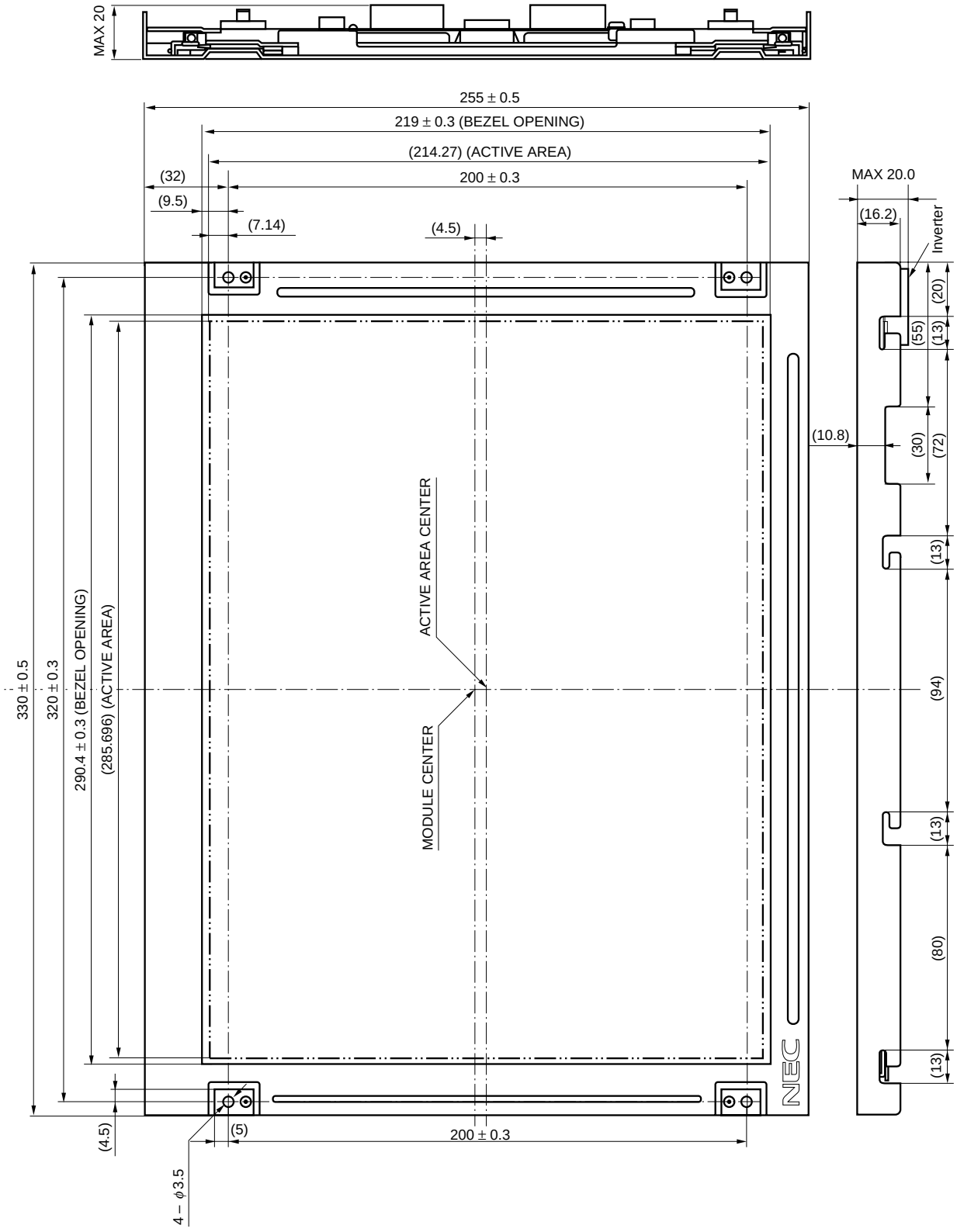
b) Do not readjust variable resistors etc.

c) When returning the module for repair or etc, please pack the module not to be broken. We recommend to the original shipping packages.

Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

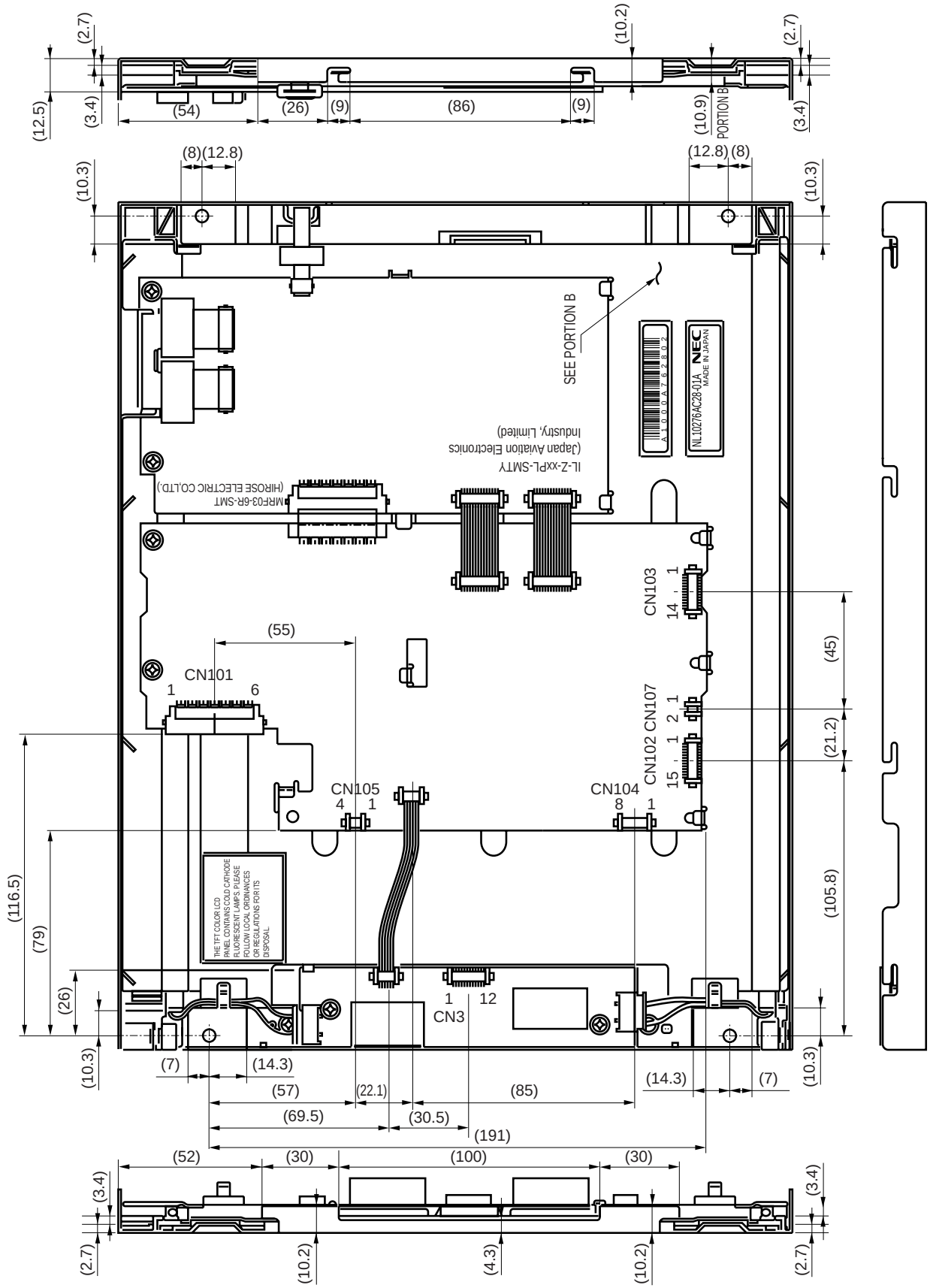
- The display condition of LCD module may be affected by the ambient temperature.
- The LCD module uses cold cathode tube for backlighting. Optical characteristics, like luminance or uniformity, will change during time.
- Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING: Front View (Unit: mm)



Remark The torque to mounting screw should never exceed 0.392 · Nm (4 kgf · cm).

OUTLINE DRAWING: Rear View (Unit: mm)



Remark The torque to mounting screw should never exceed 0.392 · Nm (4 kgf · cm).

[MEMO]

[MEMO]