NEC

TFT COLOR LCD MODULES

NL10276AC20-03

26 cm (10.4 inches), 1024 × 768 pixels, 4096 colors, incorporated backlight

DESCRIPTION

NL10276AC20-03 is a TFT (thin film transistor) active matrix color LCD (liquid crystal display) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit, and a backlight.

The 26 cm (10.4 inches) diagonal display area contains 1024 × 768 pixels and can display 4096 colors simultaneously.

By utilizing an edge-light type backlight, a very thin profile design and low power consumption was achieved.

FEATURES

- ○ Low reflection
- ○ Thin and light weight
- ○ Low power consumption
- ○ High resolution and high quality screen
- ○ Incorporated edge-light type backlight
- ○ DE (Data Enable) function

APPLICATIONS

- ○ Notebook personal computer, Word processor
- ○ Display terminals for control system
- ○ Control board for NC machine
- ○ Monitor for process controller

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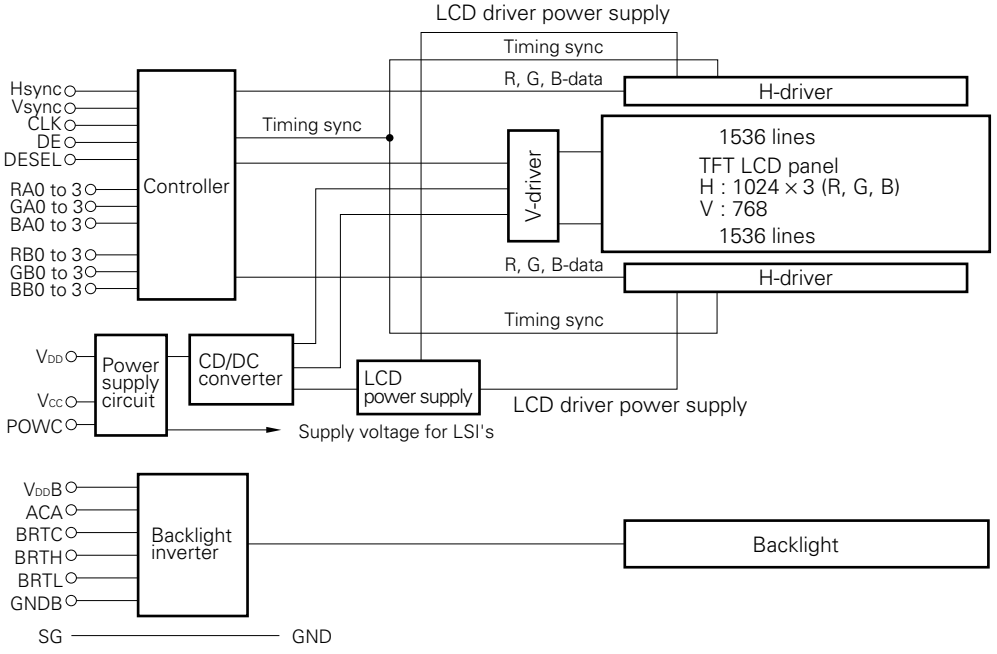
STRUCTURE AND FUNCTIONS

A TFT color LCD module comprises a TFT LCD panel, LSIs for driving liquid crystal, and the backlight. The TFT LCD panel is composed of a TFT array glass substrate superimposed on a color filter glass substrate with liquid crystal filled in the narrow gap between two substrates. The backlight apparatus is located on the backside of the LCD panel.

RGB (Red, Green, Blue) data signals are sent to LCD panel drivers after modulation into suitable forms for active matrix addressing through signal processor.

Each of the liquid crystal cells acts as an electro-optical switch that controls the light transmission from the backlight by a signal applied to a signal electrode through the TFT switch.

BLOCK DIAGRAM



OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	211.968 (H) × 158.976 (V) mm (diagonal size 10.4 inches)
Drive system	a-Si TFT active matrix
Display colors	4096 colors
Number of pixels	1024 × 768 pixels
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.207 (H) × 0.207 (V) mm
Module size	282.0 (H) × 190.0 (V) × 13.0 (D) mm
Weight	680 g (typ.)
Contrast ratio	100 : 1 (typ.)
Viewing angle (within the contrast ratio of 10 : 1)	
	Horizontal : 45° (typ. Left side, Right side)
	Vertical : 25° (typ. Up side), 25° (typ. Down side)
Designed viewing direction	• Wider viewing angle with contrast ratio : down side (6 o'click)
	• Wider viewing angle without image reversal : up side (12 o'click)
	• Optimum grayscale (γ = 2.2) : perpendicular
Color gamut	40 % (min. center, to NTSC)
Response time	40 ms (min.)

Luminance	85 cd / m^2 (typ. ac adapter mode), 50 cd / m^2 (typ. battery mode)
Signal system	4-bit digital signals for each of RGB primary colors, synchronous signals (Hsync, Vsync), Dot clock (CLK)
Supply voltages	5, 12 , 12 V (ac adapter mode) or 6.0 V (battery mode)
Backlight	Edge-light type backlight
Power consumption	5.5 W (typ. ac adapter mode), 4.3 W (typ. battery mode)

GENERAL SPECIFICATIONS

Item	Specification	Unit
Module size	282.0±1(H) × 191.0±1 × 13.0 max. (D)	mm
Display area	211.968 (H) × 158.976 (V) (diagonal size 10.4 inch)	mm
Number of pixels	1024 × 3 (H) × 768 (V)	pixel
Dot pitch	0.069 (H) × 0.207 (V)	mm
Pixel pitch	0.207 (H) × 0.207 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	—
Display colors	4096	color
Weight	700 (max.)	g

An inverter is incorporated within the module. (A luminance control variable resister is extra.)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Power supply	V_{CC}	–0.3 to 6.0	V	Ta = 25˚C
	V_{DD}	–0.3 to 21.0	V	
	$V_{DD}B$	–0.3 to 21.0	V	
Input logic	V_{in}	–0.3 to V_{CC} +0.3	V	
Storage temp.	T_{ST}	–20 to 60	˚C	—
Operating temp.	T_{OP}	0 to 50	˚C	Module surface*
Humidity	–	≤ 95 % relative humidity ≤ 85 % relative humidity Absolute humidity shall not exceed Ta = 50˚C / 85 % R.H. level.	% R.H.	Ta = 40˚C Ta = 50˚C Ta > 50˚C

* Measured at the display area

ELECTRICAL CHARACTERISTICS

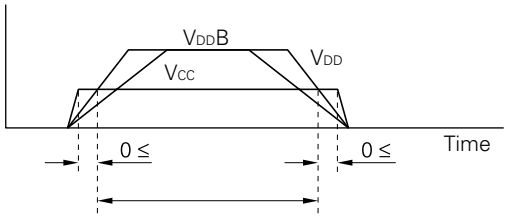
(1) Logic, LCD driving

Ta = 25°C

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	V_{CC}	4.75	5.0	5.25	V	Logic power supply
	V_{DD}	6.0	12.0	20.0	V	LCD drive power supply
	$V_{DD}B$	6.0	12.0	20.0	V	Backilight power supply
Logic input "L"	V_{IL}	0	—	0.8	V	TTL level
Logic input "H"	V_{IH}	2.0	—	V_{CC}	V	TTL level
Supply current	I_{CC}	—	83	100	mA	Logic power supply V_{CC} = 5.0 V *
	I_{DD}	—	120	150	mA	LCD drive power supply V_{DD} = 12.0 V *
	$I_{DD}B$	—	300	360	mA	Backlight power supply $V_{DD}B$ = 12.0 V ACA = L
		—	190	230	mA	Backlight power supply $V_{DD}B$ = 20.0 V ACA = L
		—	390	470	mA	Backlight power supply $V_{DD}B$ = 6.0 V ACA = H

* Dot checkered pattern

SUPPLY VOLTAGE SEQUENCE



Apply signals within this period *4
(In this period, CLK, Hsync, Vsync, DESEL and DE should be provided continuously.).

*1 The supply voltage for the module input signals should be the same as the module's V_{CC}.

*2 Apply $V_{DD}B$ within the LCD operation period. When the backlight turns on before LCD operation or LCD operation turns off before the backlight turns off, the display may momentarily become white.

*3 In the period of V_{CC} = off or the POWC = low, keep all signals (CLK, Hsync, Vsync, data, etc.) low (<0.5 V) or high impedance.

*4 Apply V_{DD} after V_{CC} works. If V_{DD} is applied before V_{CC} works, the module may be broken.

*5 If the backlight is controlled by the BRTC signal instead of $V_{DD}B$ on / off control, take the same sequence noted *2

INTERFACE PIN CONNECTION

(1) Interface signals, power supply

CN1 : LZ-10P-SL-SMT-E3000 (Japan Aviation Electronics industry, Limited)

Pin No.	Symbol	Function
1	BRTH	Luminance control input
2	GA0	Green data A0 (LSB)
3	SG	Signal ground
4	RB3	Red data B3 (MSB)
5	SG	Signal ground
6	RB2	Red data B2
7	SG	Signal ground
8	RB1	Red data B1
9	ACA	AC / BATT mode signal
10	RB0	Red data B0 (LSB)

CN2 : LZ-20P-SL-SMT-E3000 (Japan Aviation Electronics industry, Limited)

Pin No.	Symbol	Function
1	SG	Signal ground
2	GB2	Green data B2
3	SG	Signal ground
4	GB1	Green data B1
5	BRTL	Luminance control input
6	GB0	Green data B0 (LSB)
7	SG	Signal ground
8	BB3	Blue data B3 (MSB)
9	SG	Signal ground
10	BB2	Blue data B2
11	SG	Signal ground
12	BB1	Blue data B1
13	BRTC	Backlight control
14	BB0	Blue data B0 (LSB)
15	SG	Signal ground
16	GA3	Green data A3 (MSB)
17	SG	Signal ground
18	GA2	Green data A2
19	SG	Signal ground
20	GA1	Green data A1

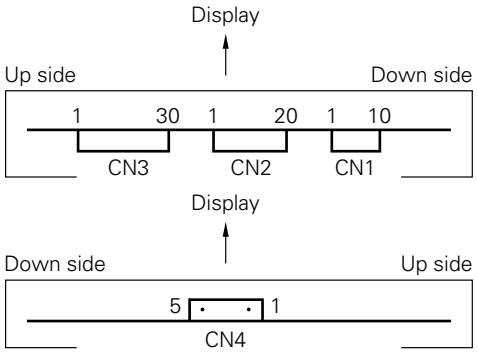
CN3 : LZ-30P-SL-SMT-E3000 (Japan Aviation Electronics industry, Limited)

Pin No.	Symbol	Function
1	GNDB	Ground for backlight
2	GNDB	Ground for backlight
3	V_{DD}B	V_{DD} for backlight
4	V_{DD}B	V_{DD} for backlight
5	V_{DD}	V_{DD} for LCD drive
6	Vsync	Vertical sync.
7	SG	Signal ground
8	CLK	Dot clock
9	V_{CC}	V_{CC} for logic
10	DE	Data enable
11	SG	Signal ground
12	Hsync	Horizontal sync.
13	SG	Signal ground
14	RA3	Red data A3 (MSB)
15	SG	Signal ground
16	RA2	Red data A2
17	SG	Signal ground
18	RA1	Red data A1
19	DESEL	Data enable select
20	RA0	Red data A0 (LSB)
21	SG	Signal ground
22	BA3	Blue data A3 (MSB)
23	SG	Signal ground
24	BA2	Blue data A2
25	SG	Signal ground
26	BA1	Blue data A1
27	POWC	Power control
28	BA0	Blue data A0 (LSB)
29	SG	Signal ground
30	GB3	Green data B3 (MSB)

Note : The pins for BRTH and BRTL of luminance control on the left side (CN1, CN2) and the right back (CN4) are connected through each in the module. Then, any one pair of the pins are available for luminance control variable resistor.

CN4 : LZ-5P-SL-SMT-E3000 (Japan Aviation Electronics industry, Limited)

Pin No.	Symbol	Function
1	N,C.	Non connection
2	BRTL	Luminance control input
3	BRTL	Luminance control input
4	BRTH	Luminance control input
5	BRTH	Luminance control input



CONNECTOR LOCATION (view from insert side)

(2) Pin Description

Pin Symbol	Function	Logic	Description
Vsync	Vertical sync.	Nega.	Vertical synchronous signal. Refer to the input signal timing.
Hsync	Horizontal sync.	Nega.	Horizontal synchronous signal. Refer to the input signal timing.
DE	Data enable	Posi.	When DESEL = L, the function of this pin is ignored. (keep DE high or low) When DESEL = H, the period of DE = H indicates the display period of the module.
DESEL	DE select	Posi.	DESEL = H : DE mode (Data enable function is active.) DESEL = L : Fixed mode (Data enable function is ignored.)
CLK	Dot clock	Nega.	Timing signal for display data. Module strobes the display data at the falling edge of the CLK.
RA0 to RA3 GA0 to GA3 BA0 to BA3 RB0 to RB3 GB0 to GB3 BB0 to BB3	Display data	Posi.	RA0 to RA3, GA0 to GA3, BA0 to BA3 are the data for even (X = 0, 2, 4 ••• 1022) pixels. RB0 to RB3, GB0 to GB3, BB0 to BB3 are the data for odd (X = 1, 3, 5 ••• 1023) pixels.
POWC	V_{CC} / V_{DD} on / off control signal	Posi.	POWC = H : Power on inside the module POWC = L : Power off inside the module
BRTC	Backlight on / off control signal	Nega.	BRTC = H : Backlight on BRTC = L : Backlight off
ACA	AC / Battery control signal	Nega.	ACA = H : Battery mode ACA = L : AC adapter mode
BRTH BRTL	Backlight brightness control	–	Connect a variable resistor (1 kΩ ±5 %, B curve) between BRTH and BRTL.
V_{CC} V_{DD} V_{DD}B SG GNDB	+5 V (±5 %) +6 to +20 V +6 to +20 V Signal ground Backlight ground	– – – – –	Power supply for logic Power supply for driving LCD Power supply for backlight Ground for signal / Connect to system ground. Ground for backlight / GNDB is separated from SG.

DISPLAY COLORS vs. INPUT DATA SIGNALS [Note]

	Display colors	Data signals (0 : Low level, 1 : High level)											
		RA3 RB3	RA2 RB2	RA1 RB1	RA0 RB0	GA3 GB3	GA2 GB2	GA1 GB1	GA0 GB0	BA3 BB3	BA2 BB2	BA1 BB1	BA0 BB0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	1	1	1	1
	Red	1	1	1	1	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	0	0	0	0	1	1	1	1
	Green	0	0	0	0	1	1	1	1	0	0	0	0
	Cyan	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	1	0	0	0	0	0	0	0	0
	Dark	0	0	1	0	0	0	0	0	0	0	0	0
	↑			⋮				⋮				⋮	
	↓												
	Bright	1	1	0	1	0	0	0	0	0	0	0	0
		1	1	1	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0
	↑			⋮				⋮				⋮	
	↓												
	Bright	0	0	0	0	1	1	0	1	0	0	0	0
		0	0	0	0	1	1	1	0	0	0	0	0
	Green	0	0	0	0	1	1	1	1	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1
	Dark	0	0	0	0	0	0	0	0	0	0	1	0
	↑			⋮				⋮				⋮	
	↓												
	Bright	0	0	0	0	0	0	0	0	1	1	0	1
		0	0	0	0	0	0	0	0	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	1	1	1	1

Note : Colors are developed in combination with 4-bit signal (16 steps in grayscale) of each primary red, green and blue color. This process can result in up to 4096 (16 × 16 × 16) colors.

FIXED TIMING MODE SPECIFICATIONS (DESEL = "L")

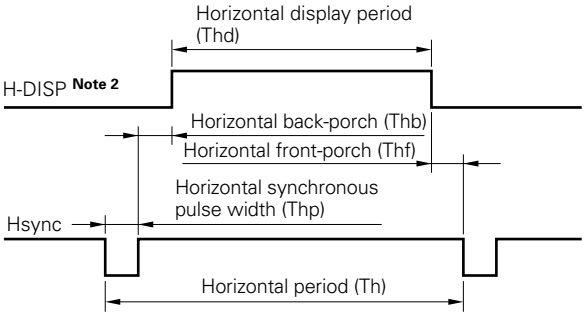
(1) Input signal specifications (fixed timing mode)

Parameter		min.	typ.	max.	Unit	Remarks
CLK	1 / Tc	–	32.5	–	MHz	30.769 ns (typ.)
	Tch /Tc	0.4	0.5	0.6	–	
	Tcrf	–	–	3	ns	
Hsync	Th	–	20.676	–	μs	48.363 kHz (typ.)
		–	672	–	CLK	
	Thd	–	15.754	–	μs	
		–	512	–	CLK	
	Thf	–	0.615	–	μs	
		–	20	–	CLK	
	Thp	–	3.2	–	μs	Thp + Thb = 140 CLK
		2	104	–	CLK	
	Thb	–	1.108	–	μs	
		–	36	138	CLK	
	Thch	2.0	–	–	ns	
	Thcs	7.0	–	–	ns	
	Tvh	7.0	–	–	ns	
	Tvs	7.0	–	–	ns	
	Thrh	–	–	4.0	ns	
Vsync	Tv	–	16.666	–	ms	60.004 Hz (typ.)
		–	806	–	H	
	Tvd	–	15.880	–	ms	
		–	768	–	H	
	Tvf	–	62.031	–	μs	
		–	3	–	H	
	Tvp	–	62.031	–	μs	Tvp + Tvb = 35 H
		2	3	–	H	
	Tvb	–	661.66	–	μs	
		–	32	33	H	
	Tvrf	–	–	10	ns	
DATA RA3 - 0, RB3 - 0	Tds	7.0	–	–	ns	
GA3 - 0, GB3 - 0	Tdh	2.0	–	–	ns	
BA3 - 0, BB3 - 0	Tdrf	–	–	4.0	ns	

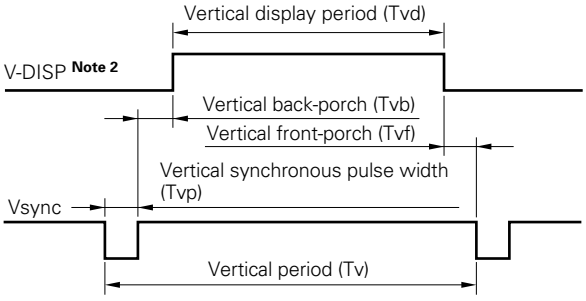
All of parameters should be kept in the specified range.

(2) Definition of input signal timing (fixed timing mode)

<Horizontal>

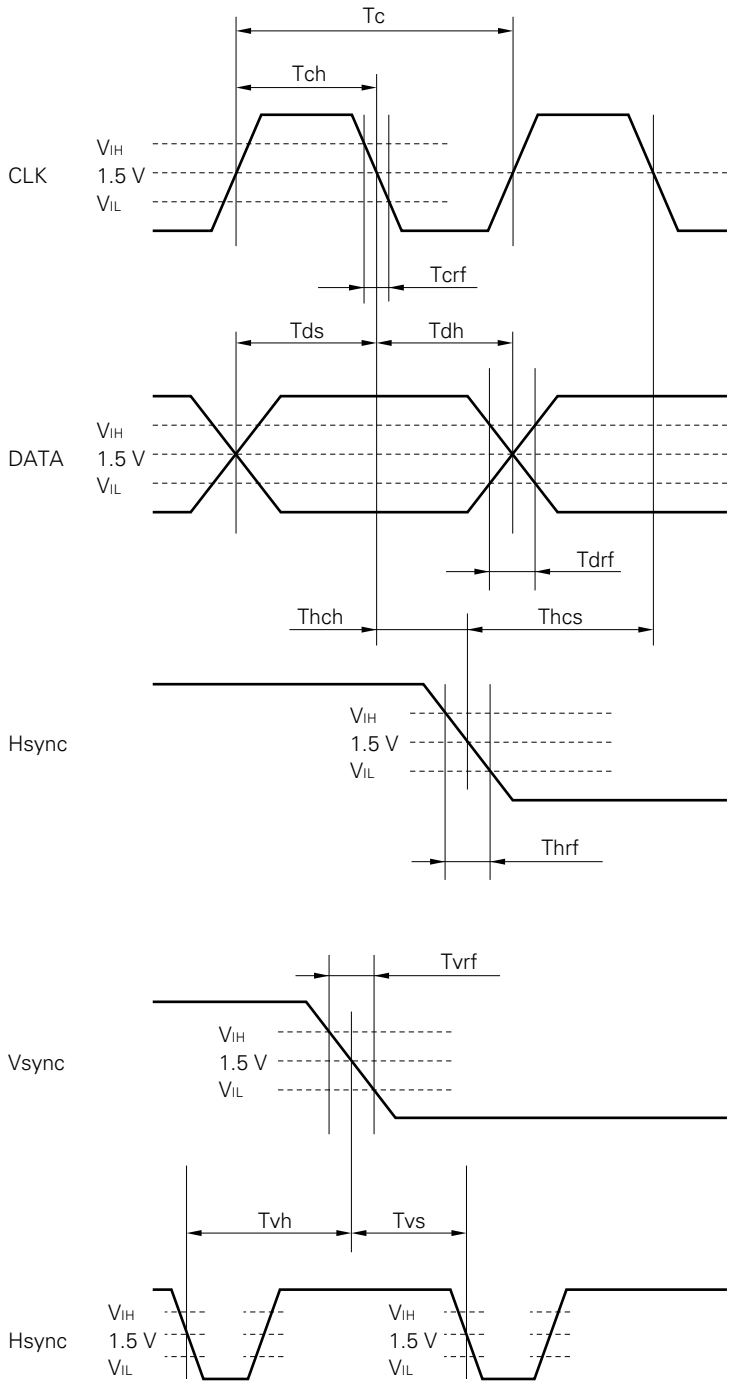


<Vertical>



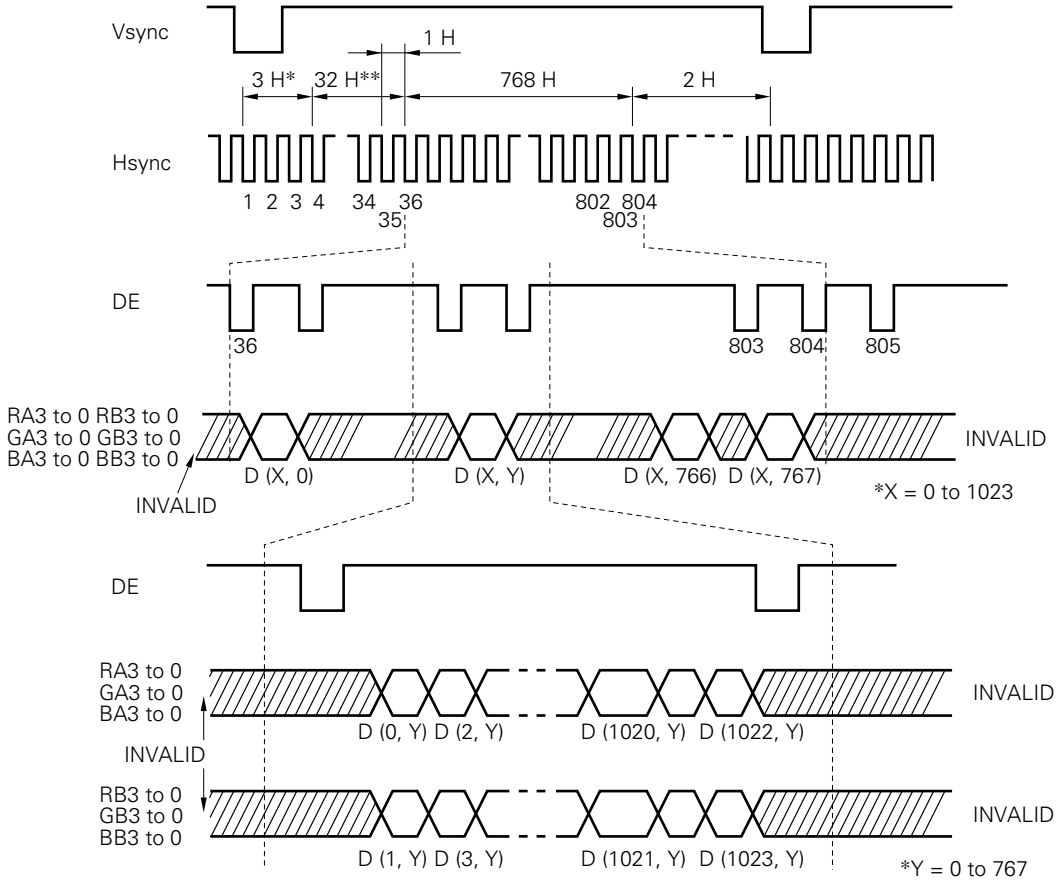
Note 1: Regarding how to count H / CLK, refer to the input signal timing chart (fixed timing mode). Thp + Thb and Tvp +Tvb are fixed. The display position will be wrong when different values are selected.

2: These do not exist as signals.

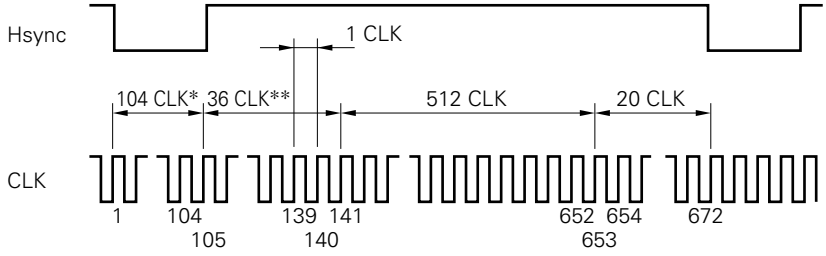


- V_{IH} = 2.2 V (min.) to V_{CC} (max.)
- V_{IL} = 0 V (min.) to 0.8 V (max.)

(3) Input signal timing chart (fixed timing mode)



*) Tvp (min.) = 2 H
**) Tvp + Tvb = 35 H (fixed)



Display positon of input data

D (0, 0)	D (1, 0)	·····	D (X, 0)	·····	D (1022, 0)	D (1023, 0)
D (0, 1)	D (1, 1)	·····	D (X, 1)	·····	D (1022, 1)	D (1023, 1)
:	:	·····	:	·····	:	:
D (0, Y)	D (1, Y)	·····	D (X, Y)	·····	D (1022, Y)	D (1023, Y)
:	:	·····	:	·····	:	:
D (0, 766)	D (1, 766)	·····	D (X, 766)		D (1022, 766)	D (1023, 766)
D (0, 767)	D (1, 767)	·····	D (X, 767)	·····	D (1022, 767)	D (1023, 767)

*) Thp (min.) = 2 CLK
**) Thp + Thb = 140 CLK (fixed)

DE MODE SPECIFICATIONS (DESEL = "H")

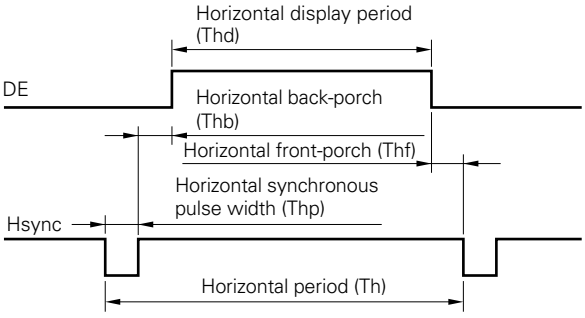
(1) Input signal specifications (DE mode)

Parameter		min.	typ.	max.	Unit	Remarks
CLK	1 / Tc	30.0	32.5	35.0	MHz	30.769 ns (typ.)
	Tch /Tc	0.4	0.5	0.6	–	
	Tcrf	–	–	3	ns	
Hsync	Th	19.2	20.676	–	μs	48.363 kHz (typ.)
		–	672	–	CLK	
	Thd	–	15.754	–	μs	
		–	512	–	CLK	
	Thf	–	0.615	–	μs	
		2	20	–	CLK	
	Thp	–	3.2	–	μs	3 ≦ Thp + Thb ≦ 158
		2	104	–	CLK	
	Thb	–	1.108	–	μs	
		0	36	–	CLK	
	Thch	2.0	–	–	ns	
	Thcs	7.0	–	–	ns	
	Tvh	7.0	–	–	ns	
	Tvs	7.0	–	–	ns	
	Thrf	–	–	4.0	ns	
Vsync	Tv	15.5	16.666	–	ms	60.004 Hz (typ.)
		–	806	–	H	
	Tvd	–	15.880	–	ms	
		–	768	–	H	
	Tvf	–	62.031	–	μs	
		0	3	–	H	
	Tvp	–	62.031	–	μs	3 ≦ Tvp + Tvb ≦ 63
		2	3	–	H	
	Tvb	–	661.666	–	μs	
		0	32	–	H	
	Tvrf	–	–	10	ns	
DATA RA3 - 0, RB3 - 0	Tds	7.0	–	–	ns	
GA3 - 0, GB3 - 0	Tdh	2.0	–	–	ns	
BA3 - 0, BB3 - 0	Tdrf	–	–	4.0	ns	
DE	Tes	7.0	–	–	ns	
	Teh	2.0	–	–	ns	
	Terf	–	–	4.0	ns	

All of parameters should be kept in the specified range.

(2) Definition of input signal timing (DE mode)

<Horizontal>



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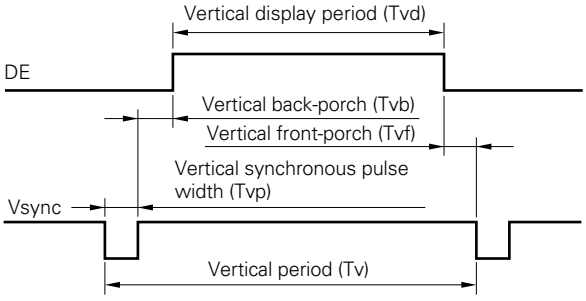
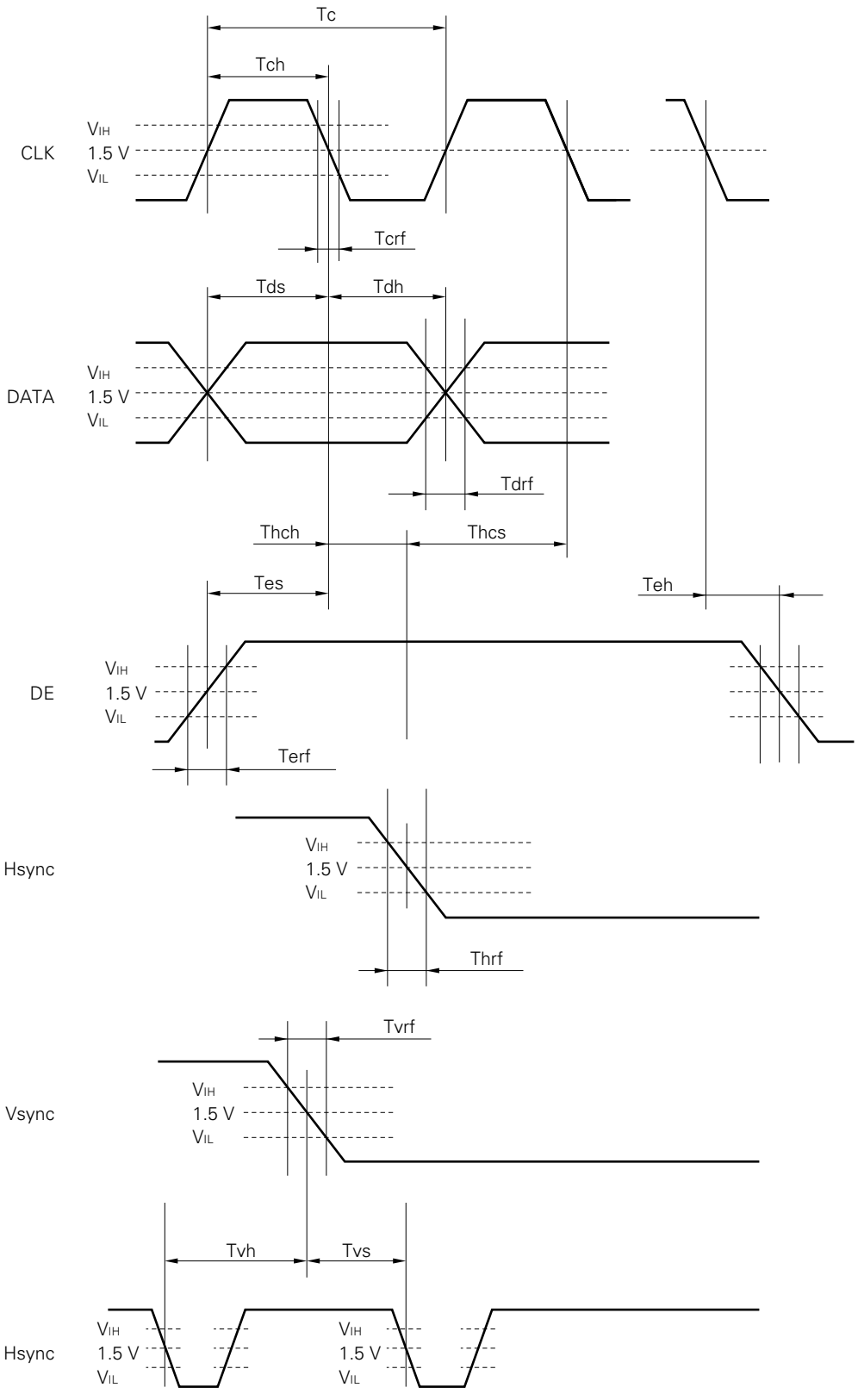
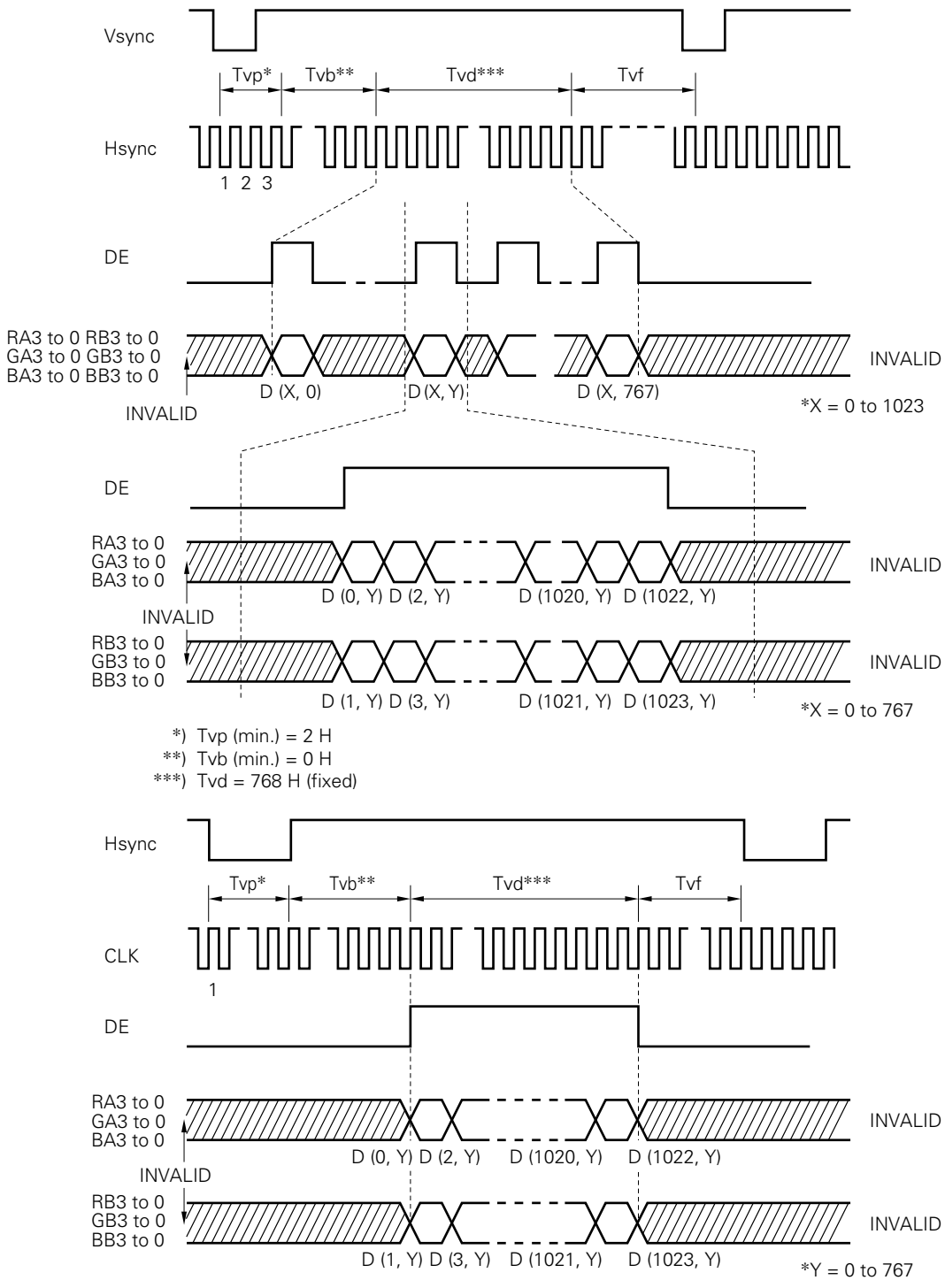


Note : Regarding how to count H / CLK, refer to the input signal timing chart (DE mode).



- V_{IH} = 2.2 V (min.) to V_{CC} (max.)
- V_{IL} = 0 V (min.) to 0.8 V (max.)

(3) Input signal timing chart (DE mode)



Display positon of input data

D (0, 0)	D (1, 0)	·····	D (X, 0)	·····	D (1022, 0)	D (1023, 0)
D (0, 1)	D (1, 1)	·····	D (X, 1)	·····	D (1022, 1)	D (1023, 1)
:	:	·····	:	·····	:	:
D (0, Y)	D (1, Y)	·····	D (X, Y)	·····	D (1022, Y)	D (1023, Y)
:	:	·····	:	·····	:	:
D (0, 766)	D (1, 766)	·····	D (X, 766)		D (1022, 766)	D (1023, 766)
D (0, 767)	D (1, 767)	·····	D (X, 767)	·····	D (1022, 767)	D (1023, 767)

*) Thp (min.) = 2 CLK
**) Thb (min.) = 0 CLK
***) Thd = 512 CLK (fixed)

GENERAL CAUTION

WARNING

Do not touch an inverter -- which is the circuit board that warning label is stuck on -- while the LCD module is operating, because of dangerous high voltage.

(1) Caution when taking out the module
   1) Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
   1) As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
   2) As the LCD panel and back-light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided. (Shock : $\leqq 50\ G \times 11$ ms)
   3) As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
   4) Do not pull the interface connectors in or out while the LCD module is operating.
   5) Put the module display side down on a flat horizontal plane.
   6) Handle connectors and cables with care.

(3) Cautions for the operation
   1) When the module is operating, do not lose CILK, Hsync or Vsync signals. If any one of these signals is lost, the LCD panel would be damaged.
   2) Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

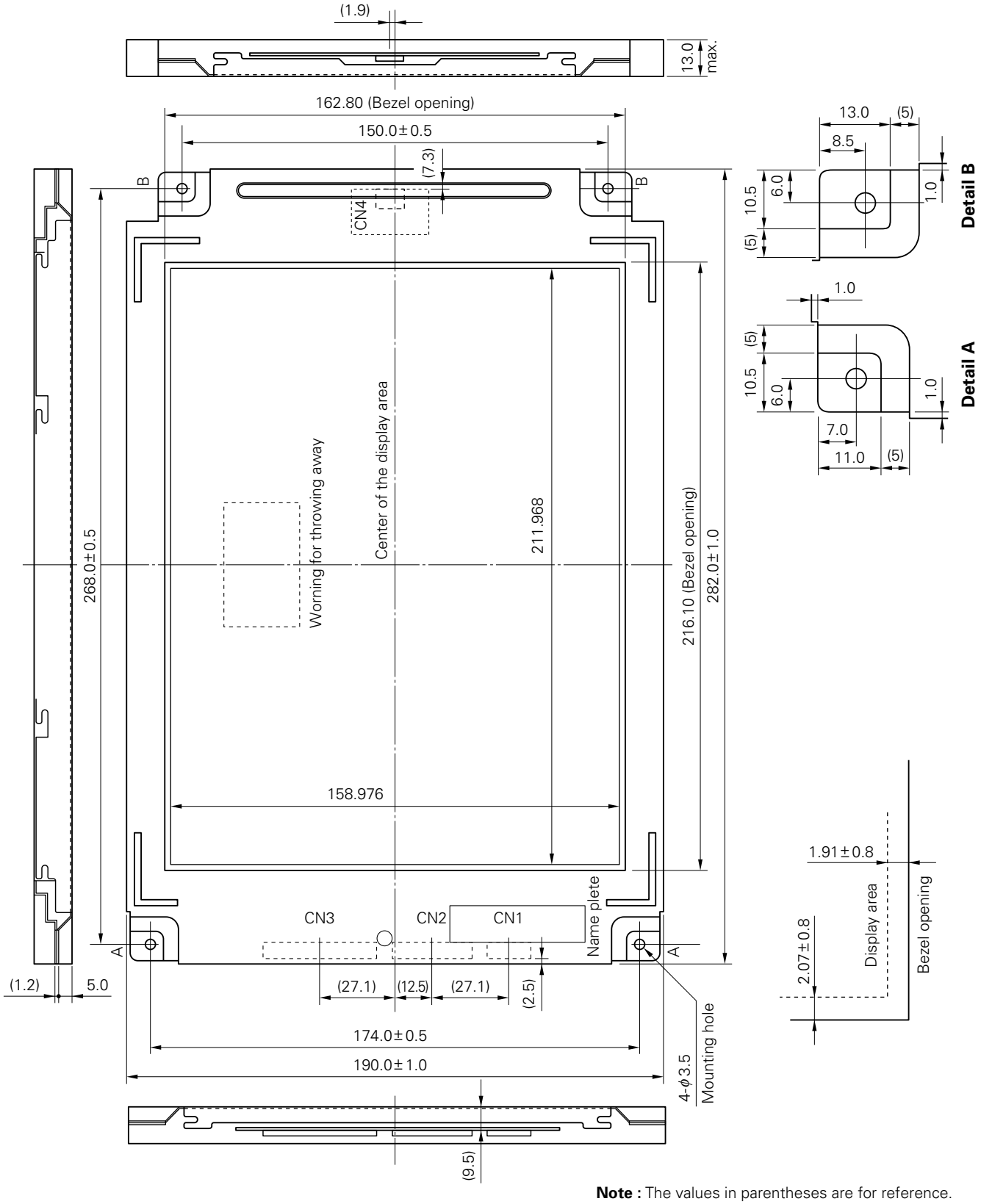
(4) Cautions for the atmosphere
   1) Dew drop atmosphere should be avoided.
   2) Do not store and / or operate the LCD module in a high temperature and / or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
   1) Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
   1) Do not disassemble and / or re-assemble LCD module.
   2) Do not re-adjust variable resistor or switch etc.
   3) When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

Liquid Crystal Display has the following specific characteristics. These are not defects or malfunctions.
The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tubes for backlighting. Optical characteristics, like luminance or uniformity, will change during time.
Uneven brightness and / or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING (Unit in mm)



Note : The values in parentheses are for reference.