REVISION HISTORY

Date.	Rev.No.	Page	Revision Description
07/30/12	V0.0		Initial Release

1. GENERAL DESCRIPTION

DESCRIPTION

LTL097QL01 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight unit. The resolution of 9.7" contains 2048 x 1536 pixels and can display up to 16,777,216.

FEATURES

High contrast ratio, Ultra wide viewing angle
QXGA (2048 x 1536 pixels) resolution
Low power consumption
Fast Response
LED Back Light
eDP Interface
3.3V eRVDS Interface

APPLICATIONS

Tablet PC
If the intent to use this product is for other purpose, please contact Samsung Display.

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	196.608(H) x 147.456(V) (9.7" diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	16,777,216		8bit
Number of pixel	2048 x 1536	pixel	4:3
Pixel arrangement	RGB vertical stripe		
Pixel pitch	96(H) X 96(V) typ	μm	
Display Mode	Normally black (PLS mode)		
Surface treatment	Low-reflection gloss surface, <1.45% Reflectance, 2H hardness		

MECHANICAL INFORMATION

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	208.58	208.88	209.18	mm	w/o flange
	Vertical (V)	166.82	167.12	167.42	mm	w/o flange
	Depth (D) Max	4.28	4.84	5.02	mm	(1)
Weight		-	-	135	g	

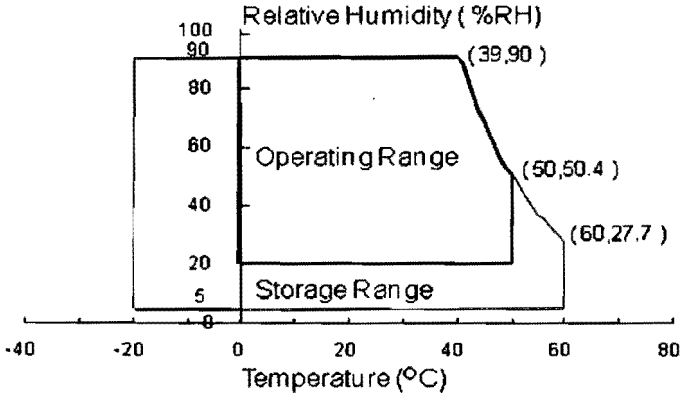
NOTE (1) Thickness Measuring Method
. Equipment : height gauge
. Measuring force : 200gf with Height Gauge

2. ABSOLUTE MAXIMUM RATINGS

2.1 ENVIRONMENTAL ABSOLTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperature (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop		240	G	(2), (4)
Vibration (non-operating)	Vnop		2.41	G	(3), (4)

Note (1) The range of temperature and relative humidity are shown in the graph below 90% RH Max. . (39℃ ≥ Ta) If the temperature is higher than 40 ℃, the maximum temperature of wet-bulb shall be less than 39℃. No condensation



(2) Vibrate ±X, ±Y, and ± Z axis in the shape of the half sine wave one time for 2ms .
(3) Vibrate the X, Y, and Z randomly within a 5 - 500 Hz range for 30min.
(4) When testing a vibration and a shock, the fixture, which holds the module to be tested shall be hard and rigid in order for the the module not to be twisted or bent by the fixture.

2.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

V_{LCD_VCC} =3.3V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	VSS - 0.3	4.0	V	(1),(2),(3)
eRVDS Input Voltage	VeRVDS	VSS - 0.3	2.0		

Note (1) Within Ta (25 ± 2 °C)
(2) Permanent damage to the device may occur if exceed maximum values.
(3) Functional operation should be restricted to the conditions described under normal operating conditions.

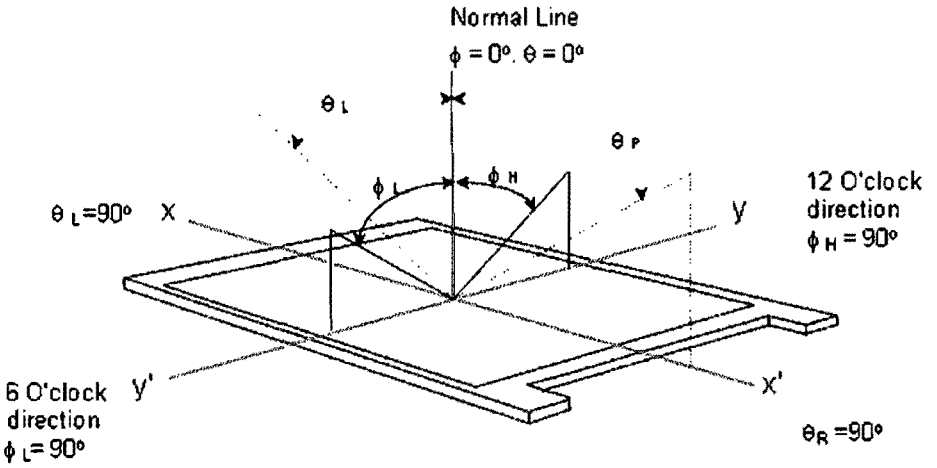
3. OPTICAL CHARACTERISTICS

The following items are measured under the stable conditions.* The optical characteristics should be measured in the dark room or the equivalent environment by the methods shown in the Note (5).
Measuring equipment : TOPCON SR-3

Ta = 25 ± 2 °C, V_{LCD_VCC} =3.3V, fv= 60Hz, fDCLK = 71.42MHz

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (5 points)		CR	Normal Viewing Angle $\phi = 0$ $\theta = 0$	700	1000	-	-	(1),(2),(5)
Response time (Rising + Falling)		T_{RT}		-	16	24	ms	(1),(3)
Average Luminance of White (5 Points)		$Y_{L,AVE}$		360	420	-	cd/m^2	IF=100% Duty (1),(4)
Color Chromaticity (CIE)	Red	R_X		-0.03	0.640	+0.03		(1),(5) SR-3
		R_Y			0.330			
	Green	G_X			0.300			
		G_Y			0.600			
	Blue	B_X			0.150			
		B_Y			0.060			
	White	W_X			0.308			
		W_Y			0.325			
Viewing Angle	Hor.	θ_L	CR ≥ 10 At center	-	85	-	Degrees	(1),(5)
		θ_H		-	85	-		
	Ver.	ϕ_H		-	85	-		
		ϕ_L		-	85	-		
White variation (13P)		δ_L		-	1.4	1.6	-	(6)

Note (1) The definition of viewing angle : The range of viewing angle (10 ≤ C/R)

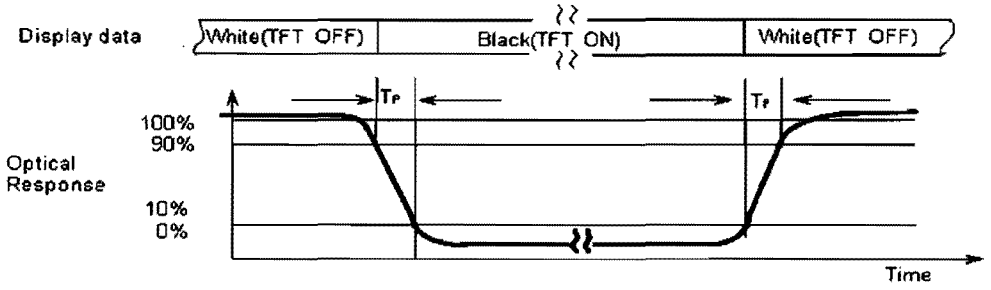


Note (2) The definition of contrast ratio (CR) : The ratio of max. gray and min gray at 5 points (4, 5, 7, 9, and10)

$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points = ④, ⑤, ⑦, ⑨, ⑩ at the figure of Note(6).

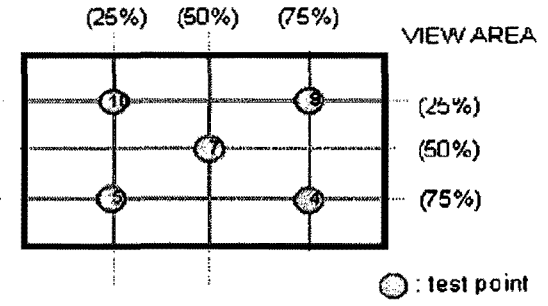
Note (3) The definition of Response time : Subtotal of the time, during which the transmission changes from 10% to 90% when the TFT turns on and off.



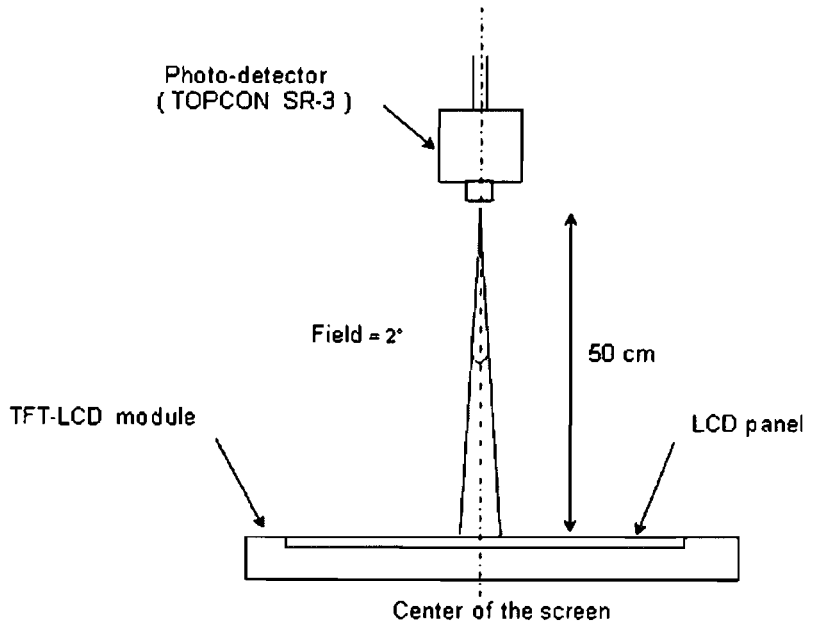
Note (4) The definition of average luminance of white : Measure the luminance of white at 5 points.

Average Luminance of White (Y_{LAVE})

$$Y_{LAVE} = \frac{Y_{L4} + Y_{L5} + Y_{L7} + Y_{L9} + Y_{L10}}{5}$$



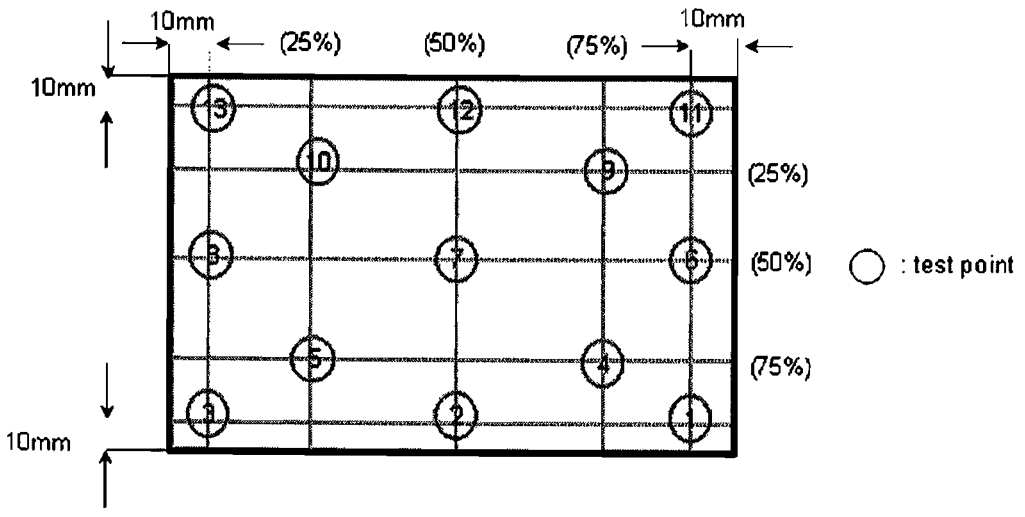
Note (5) Measure the panel, which is left for 30 min. at the normal temp. after leaving it for 30 min with turning the back light on at the rating. The measurement should be executed under the condition including the ambient temp., 25℃±2℃, the dark room, windless(removed the direct wind), and no vibration.
IF current : 35mA
Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

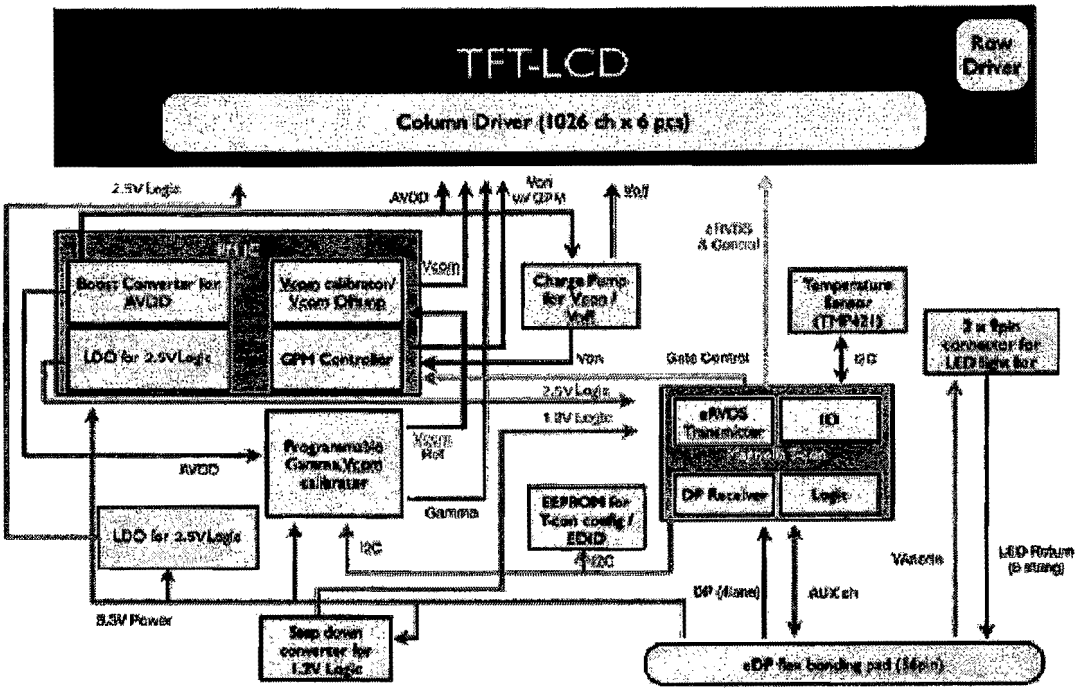
Note (6) The definition of white variation at 13 points (δ L)

$$\delta_L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



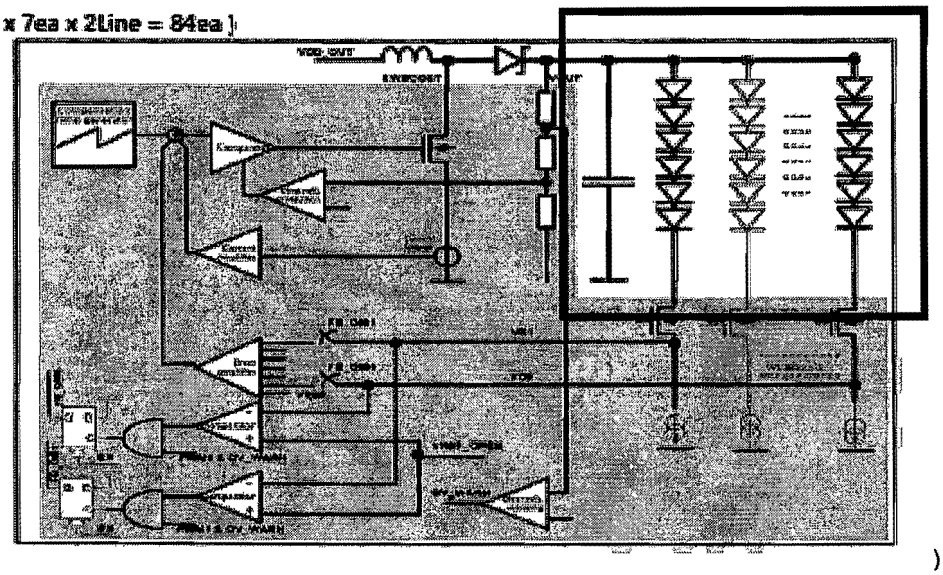
4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 THE STRUCTURE OF LED PLACEMENT

(6 String x 7ea x 2Line = 84ea)



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5. ELECTRICAL CHARACTERISTICS

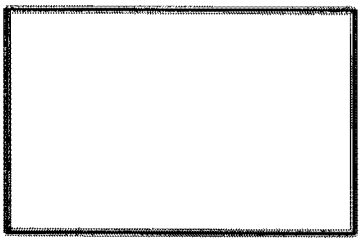
5.1 TFT LCD MODULE

* Ta = 25 ± 2 °C

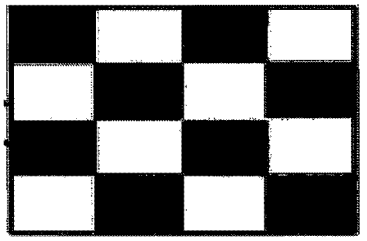
Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		VDD	3.0	3.3	3.6	V	
Vsync Frequency	60 Hz	fv	-	60	-	Hz	-
Rush Current		IRUSH	-	-	1.5	A	(4)
Current of Power Supply	White	IDD	-	324	356	mA	(2),(3)*a
	Mosaic		-	331	364	mA	(2),(3)*b
	Red		-	429	493	mA	(2),(3)*e

Note (1) The data pins for display and signal pins for timing should be connected.(GND= 0V)
(2) fV = 60Hz, V_{LCD_VCC} = 3.3V , DC Current.
(3) Power dissipation pattern
(4) The dissipation pattern for power

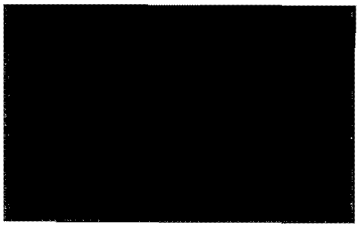
(a) White screen



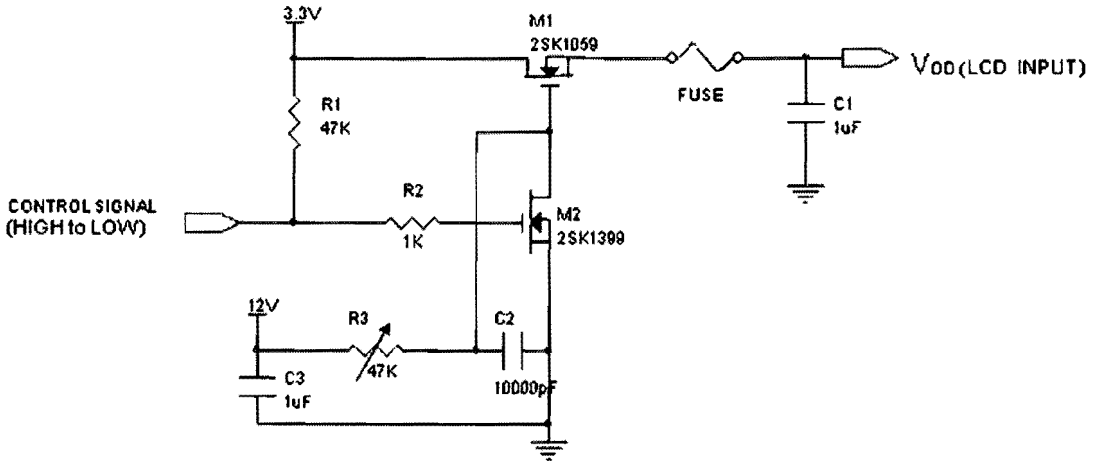
(b) Mosaic (or checker) pattern

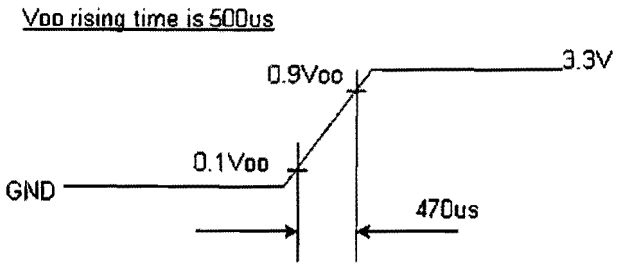


(c) Red



(4) Rush current measurement condition





5.2 BACK LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Current	IF	-	35	-	mA	
LED Forward Voltage	VF	2.7	2.8	2.9	V	IF = 21mA
LED Array Voltage	VP	-	16.8	-	V	VF X LED Counts
LED Power Consumption	P	-	0.12	-	W	
Operating Life Time	Hr	12,000	-	-	Hour	(1)
LED Counts	Q	-	84	-	EA	

Note (1) Life time (Hr) of LEDs can be defined as the time in which it continues to operate under the condition Ta= 25 ± 2 °C and IF = 21.0 mArms until one of the following event occurs.
When the brightness becomes 50% or lower than the original.

5.3 eDP INTERFACE

5.3.1 eDP DC/ I/O Characteristics

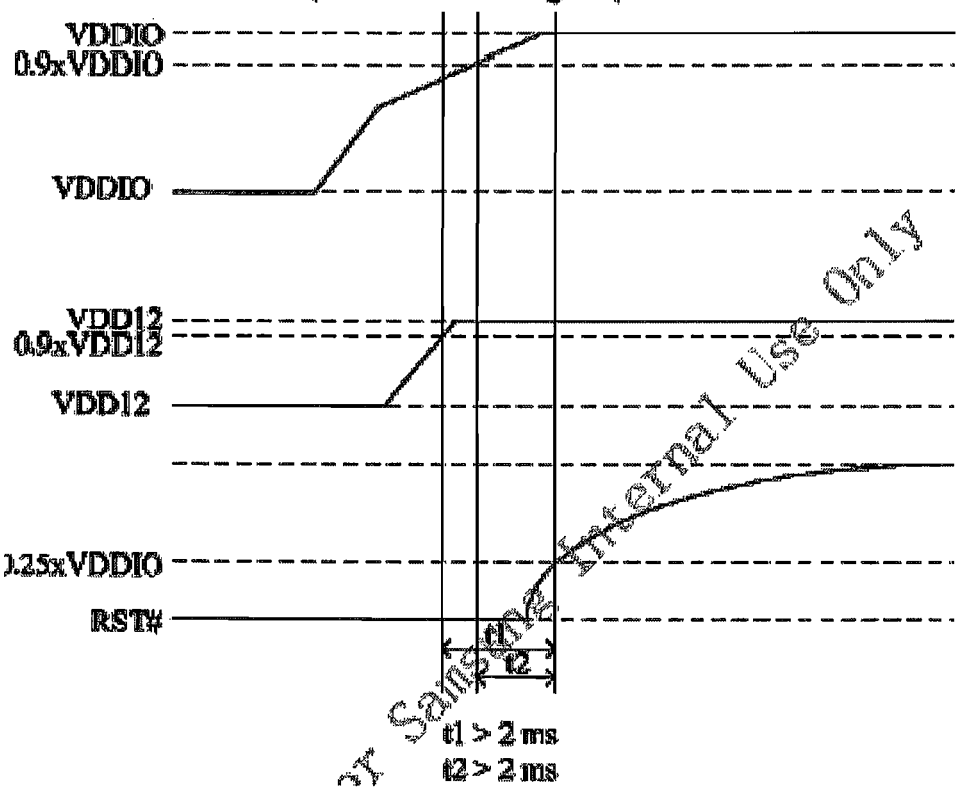
Parameter	Test Conditions	Min	Typ[2]	Max	Unit
I2C pins: xSCL, xSDA					
V_{OH} High-level output voltage	External 1.2kΩ pull-up to VCC		VCC		V
V_{OL} Low-level output voltage	2.5V to 2.8V I_{OL} = 8 mA			0.15VCC	V
SPI pins: IROMx					
V_{IH} LVCMOS input High-level voltage		0.7VDDIO			V
V_{IL} LVCMOS input Low-level voltage				0.25VDDIO	V
V_{OH} High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V
LCD control pins:					
V_{OH} High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V
General I/O pins					
V_{IH} LVCMOS input High-level voltage		0.7VDDIO			V
V_{IL} LVCMOS input Low-level voltage				0.25VDDIO	V
V_{OH} High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDDIO			V
V_{OL} Low-level output voltage				0.15VDDIO	V

5.3.2 eDP AC/ I/O Characteristics

Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Supply ramp up time:					
$t_{2.5}$ VDDIO supply ramp up time	10% to 90% of the VDDIO supply voltage			10	ms
$t_{1.2}$ 1.2V supply ramp up time	10% to 90% of the 1.2V supply voltage			10	ms
Power ramp delay					
Δt_{POWER} Delay time from VDDIO supply to 1.2V VDD12 & VDDRX supply	90% of VDDIO supply to 90% of 1.2V supply	-10		10	ms
$\Delta t_{POWER-RSTN}$ Delay from 1.2V power ready & VDDIO power ready to RST_N pin de-assertion	90% of 1.2V supply & 90% of VDDIO supply (all power supplies ready) to 25% of the RST_N (pin D4) de-assertion (rising edge)				ms
CMOS output pins: GPIOx	C_L = 10 pF				
t_r Output rise time				6	ns
t_f Output fall time				6	ns

SPI pins: IROMx						
thi	Clock high time		9			ns
tlo	Clock low time		9			ns
tsetup	Data in setup time reference to clock rising edge		5			ns
thold	Data in hold time reference to clock rising edge		5			ns
tv	Data out valid time reference to clock falling edge				9	ns
tho	Data out hold time reference to clock falling edge		0			ns
tcss	Chip select setup time reference to clock rising edge		25			ns
tcsh	Chip select hold time reference to clock falling edge		10			ns
Master I2C pins: MSCL, MSDA						
t_{rise}	Master I2C bus 10% to 90% rise time				150	ns

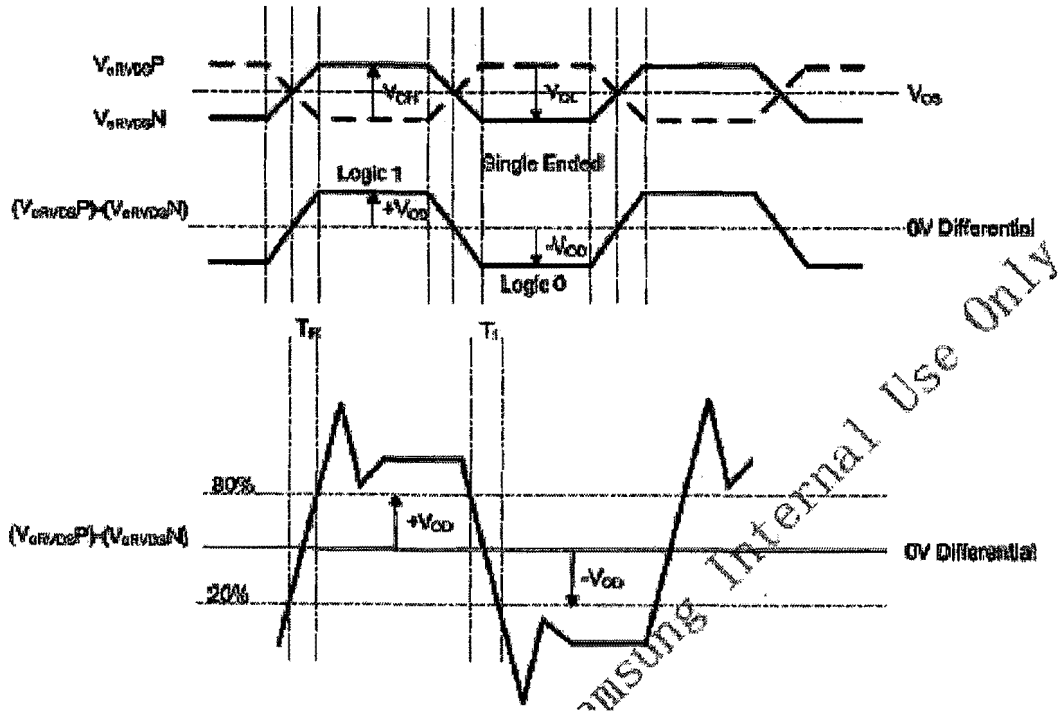
Power up and reset timimg sequence



5.3.3 eRVDS transmitter characteristics

Symbol and Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Transmitter Characteristics					
V_{OD}: Differential output voltage at default setting	COG LV driver test set-up as shown in the below figure Rterm=100Ω	320	400	480	mV
Minimum programmable swing (8 programmable levels)			200		mV
Maximum programmable swing (8 programmable levels)			600		mV
V_{CM}: Output common-mode voltage		500	600	700	mV
Minimum programmable V_{CM} (8 programmable steps)			500		mV
Maximum programmable V_{CM} (8 programmable steps)			700		mV
ΔV_{OD}: Variation in V_{OD} between 0 and 1				30	mV
ΔV_{CM}: Variation in V_{CM} between 0 and 1				30	mV
T_R/T_F: Rise and Fall Transition Time (20% - 80%)	V_{CM} = 600mV V_{OD} = 400mV		430		ps
R_{TX}: Transmitter Differential Output Impedance			100		Ω
Minimum programmable output impedance			70		Ω
Maximum programmable output impedance			500		Ω

Power up and reset timing sequence



5.3.4 Displayport Aux channel characteristics

Symbol and Parameter	Test Conditions	Min	Typ[2]	Max	Unit
UI: Unit Interval for AUX channel		0.4	0.5	0.6	μs
$V_{AUX-DIFF-p-p}$: AUX differential peak-to-peak voltage at TP1 when driving the bus		500		1000	mV
$V_{AUX-DC-CM-TX}$: AUX common mode voltage when receiving			GND		V
$V_{AUX-DC-CM-RX}$: AUX common mode voltage when transmitting			0.15		V
$I_{AUX-SHORT}$: AUX channel short circuit current				20	mA
$R_{AUX-DIFF}$: Differential termination resistance		80	100	120	Ω
R_{AUX-SE}: Single-ended termination resistance		40	50	60	Ω
C_{AUX}: AUX AC coupling capacitor		75		200	nF

5.3.5 Displayport Main link receiver characteristics

Symbol and Parameter	Test Conditions	Min	Typ[2]	Max	Unit
Spread spectrum clock, down-spreading by SOURCE			0.5		%
Additional spread spectrum clock by SINK, Modulation frequency		10		40	kHz
Center spreading amplitude (programmable)		-1.0%		1.0	%
$V_{RX-DIFFp-p}$: Differential peak-to-peak input voltage at package pins		100		1320	mV
Maximum adaptive(programmable equalization level at 1.35GHz			9		dB
$V_{RX\_DC\_CM}$: Rx input DC common mode voltage			GND		V
$R_{RX-DIFF}$: Differential termination resistance		80		100	Ω
R_{RX-SE}: Single-ended termination resistance		40		60	Ω
I_{RX_SHORT}: Rx short circuit current limit				20	mA
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (HBR)					
RX intra-pair skew tolerance at HBR				150	ps
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (RBR)					
RX intra-pair skew tolerance at RBR				300	ps

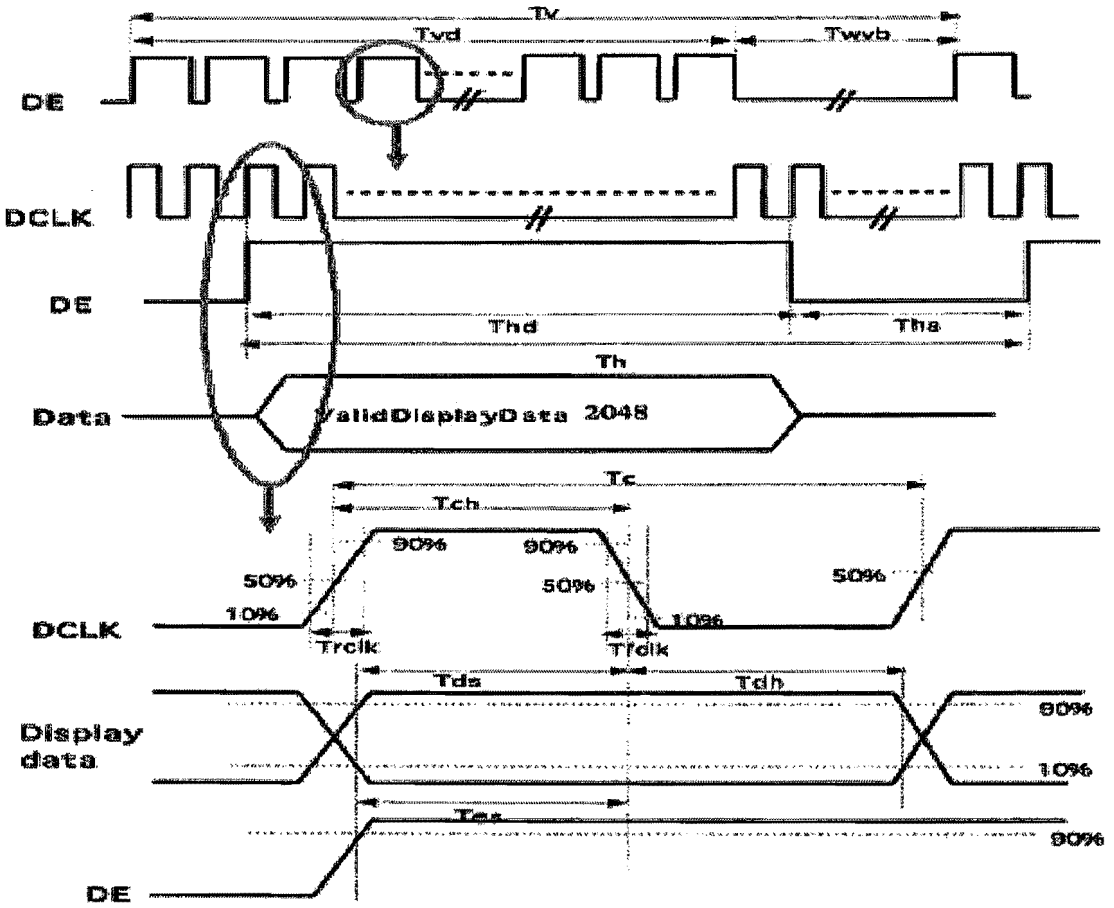
Receiver Jitter Tolerance for High Bit Rate (HBR) Total jitter tolerance at 2MHz Total jitter tolerance at 10MHz Total jitter tolerance at 20MHz Total jitter tolerance at 100MHz Receiver Jitter Tolerance for Reduced Bit Rate (RBR) Total jitter tolerance at 2MHz Total jitter tolerance at 10MHz Total jitter tolerance at 20MHz Note: Jitter Tolerance Testing follows *VESA DisplayPort™ PHY Compliance Testing Standard, Version 1.1.*		 1227 548 505 491 1648 778 747			 mUI mUI mUI mUI mUI mUI mUI
Symbol Error Rate, normal link data transmission, HBR, 4 lane operation	1. TJ at Receiver Connector (TP3) ≤ 0.491UI @ Bit Error Rate (BER) = 10^{-12} 2. Eye Height at TP3 ≥ 150mVpp 3. Max lane to lane mismatch of insertion loss at TP3: 20*log |max(eye height)/min(eye height)| ≤ 2.3dB 4. Max source pre-emphasis level at level 0 (0dB) ≤ 0.25dB	10^{-13}			

5.4 INTERFACE TIMING

5.4.1 TIMING PARAMETERS

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	TV	-	60	-	Hz	
Vertical Active Display Term	Display Period	TVD	-	1536	-	Lines	
One Line Scanning Time	Cycle	TH	-	2208	-	Clocks	
Horizontal Active Display Term	Display Period	THD	-	2048	-	Clocks	

5.4.2 TIMING DIAGRAMS OF INTERFACE SIGNAL



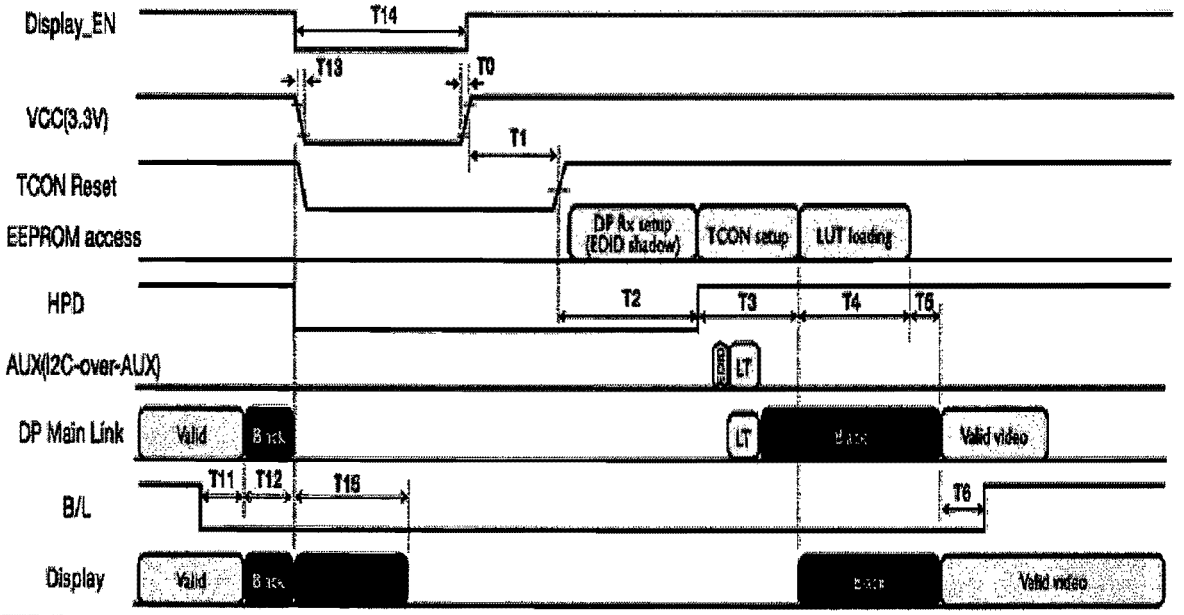
5.5 INPUT COLOR DATA MAPPING

Color		Input Color Data																							
		Red								Green								Blue							
		MSB						LSB		MSB						LSB		MSB						LSB	
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Mageuta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(01)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(02)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
		1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(253)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255) Bright																								
Green	Green(00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Green(02)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green(255) Bright																								
Blue	Blue(00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(02)	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Blue(255) Bright																								

Note) Input signal: 0 =Low level voltage, 1=High level voltage

5.6 POWER ON/OFF SEQUENCE

To prevent the product from being latched up or the DC in the LCD module from starting an operation, the order to turn the power on and off should be changed to the order as shown in the diagram below.



Time	Description	Min.	Typ.	Max.	Time	Description	Min.	Typ.	Max.
T0	VCC rise time (10% - 90%)	0.1	-	2	T11	One full valid frame after B/L OFF	-	-	17
T1[1][2]	Reset assertion delay from VCC rising	2	-	15	T12	One full black frame after valid frame	-	-	17
T2[1][2][3]	HPD assertion time	2	30	50	T13	VCC falling time (below 0.1xVCC)	-	-	TBD
T3	TCON initialization (DP Rx is up prior to this)	-	17	30	T14[2]	Minimum power-off duration requirement	125	-	-
T4	LUT loading completion	-	30	45	T15	Pixel discharge time	-	-	TBD
T5	Full black frame	17	17	17					
T6	Full valid frame	17	17	34					
CPU Info	Max. power-on delay		193		Display EN Restart	Min. power off duration requirement		125	

1. EDID(vendor ID) is cached to internal register during this period
2. Minimum time for panel and power-rail discharge
3. HPD assertion max. from VCC will be T1 + T2

Unit : ms

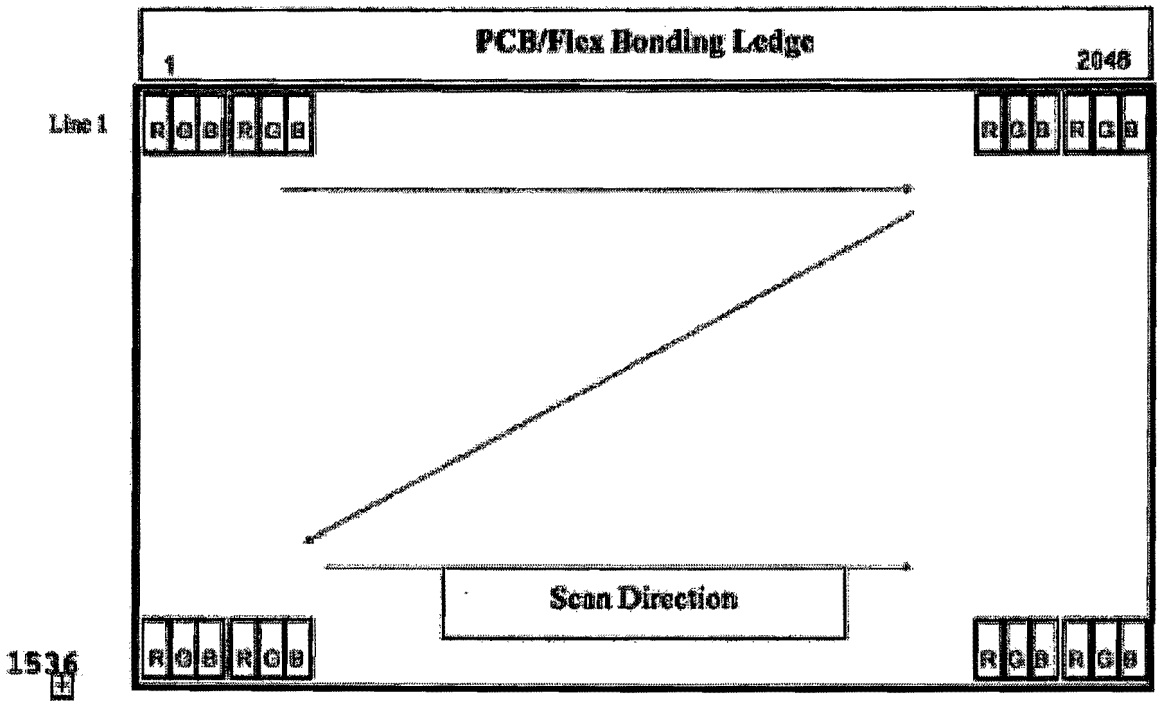
5.8 INPUT TERMINAL PIN ASSIGNMENT

5.8.1 INPUT SIGNAL & POWER
(eDP, Connector : 20455-040E-0, I-PEX or the equipment with equivalent capability)

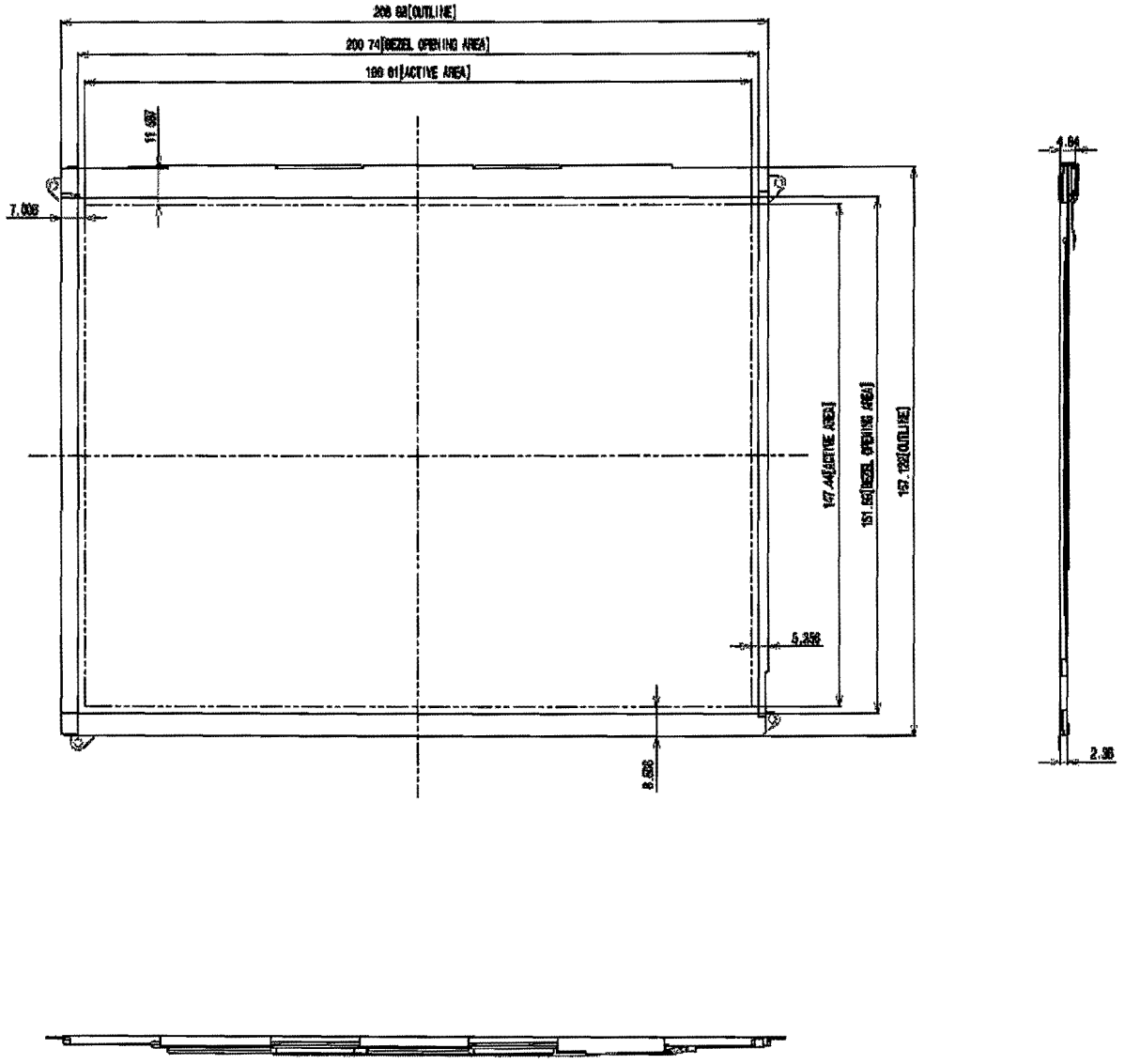
Pin No.	Symbol	Function	Remark
1	GND	Ground	
2	HPD	Hot Plug Detect	
3	GND	Ground	
4	PVDD	VCC	
5	PVDD	VCC	
6	PVDD	VCC	
7	PVDD	VCC	
8	GND	Ground	
9	AUX_P	Positive eDP AUX Data Input	
10	AUX_N	Negative eDP AUX Data Input	
11	GND	Ground	
12	LANE_0N	Negative eDP Differential Data Input	
13	LANE_0P	Positive eDP Differential Data Input	
14	GND	Ground	
15	LANE_1N	Negative eDP Differential Data Input	
16	LANE_1P	Positive eDP Differential Data Input	
17	GND	Ground	
18	LANE_2N	Negative eDP Differential Data Input	
19	LANE_2P	Positive eDP Differential Data Input	
20	GND	Ground	
21	LANE_3N	Negative eDP Differential Data Input	
22	LANE_3P	Positive eDP Differential Data Input	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	FB6_B	Current Feedback for Branch #6 of the LED Array	
27	FB5_B	Current Feedback for Branch #5 of the LED Array	
28	FB4_B	Current Feedback for Branch #4 of the LED Array	
29	FB3_B	Current Feedback for Branch #3 of the LED Array	

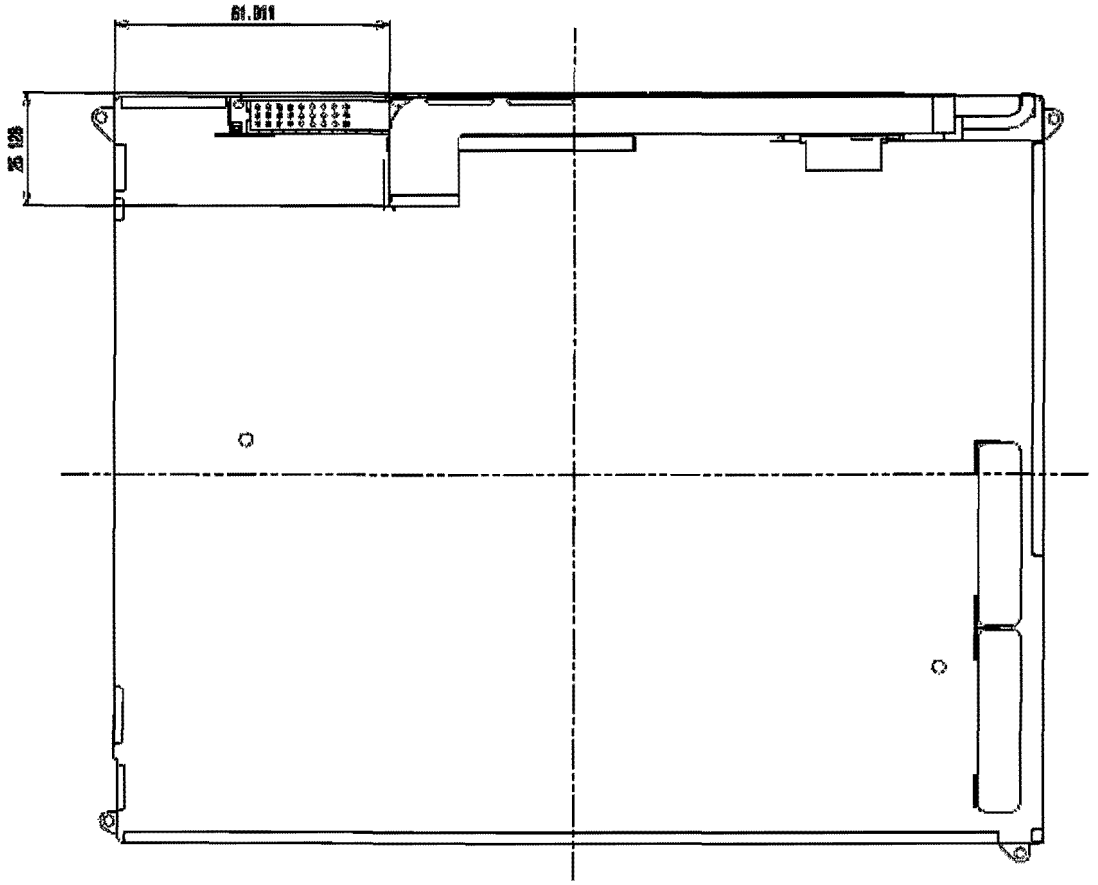
30	FB2_B	Current Feedback for Branch #2 of the LED Array	
31	FB1_B	Current Feedback for Branch #1 of the LED Array	
32	GND	Ground	
33	FB6_A	Current Feedback for Branch #6 of the LED Array	
34	FB5_A	Current Feedback for Branch #5 of the LED Array	
35	FB4_A	Current Feedback for Branch #4 of the LED Array	
36	FB3_A	Current Feedback for Branch #3 of the LED Array	
37	FB2_A	Current Feedback for Branch #2 of the LED Array	
38	FB1_A	Current Feedback for Branch #1 of the LED Array	
39	GND	Ground	
40	NC	NC	
41	VBLU_B	Power OF LED	
42	VBLU_B	Power OF LED	
43	VBLU_B	Power OF LED	
44	NC	NC	
45	GND	Ground	
46	NC	NC	
47	VBLU_A	Power OF LED	
48	VBLU_A	Power OF LED	
49	VBLU_A	Power OF LED	
50	NC	NC	
51	GND	Ground	

6. PIXEL FORMAT



7. OUTLINE DIMENSION

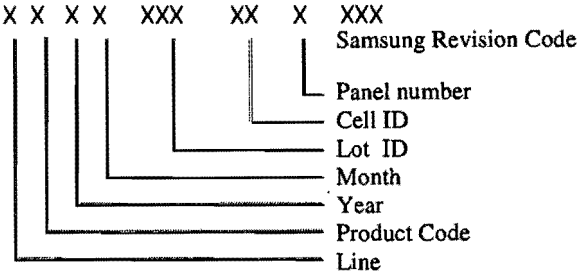



61.011

8 MARKING

A nameplate is affixed to the specified location on each product.

(1)Parts number : LTL097QL01
(2)Revision code : 3 letters
(3)Lot number : X X X X XXX XX X XXX



9. GENERAL PRECAUTIONS

9.1 HANDLING

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and CCFT back-light.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA (Isoprophyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth .In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.

(i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the LED FPC.

(l) Do not touch any component which is located on the back side.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

9.2 STORAGE

We highly recommend to comply with the criteria in the table below.

ITEM	Unit	Min.	Max.
Storage Temperature	(℃)	5	40
Storage Humidity	(%rH)	35	75
Storage Life	12 months		
Storage Condition	- The storage room should be equipped with a good ventilation facility, which has a temperature controlling system. - Products should be placed on the pallet, which is away from the wall not on the floor. - Prevent products from being exposed to the direct sunlight, moisture, and water.; Be cautious not to pile the products up. - Avoid storing products in the environment, which other hazardous material is placed. - If products are delivered or kept in the storage facility more than 3 months,we recommend you to leave products under the condition including a 20℃ temperature and a humidity of 50% for 24 hours. - If you store semi-manufactured products for more than 3 months, bake the products under the condition including the 50℃ temp. and the 10% humidity for 24hrs after being used.		

(a) Do not leave the module in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 5 to 40 C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module under the direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage.

(d) Storage period is recommended not to exceed 1 year.

9.3 OPERATION

(a) Do not connect, disconnect the module in the " Power On" condition.

(b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence ".

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The FPC cable between the LED chips and its converter power supply shall be a minimized length and be connected directly .The longer cable between the back-light and the converter may cause lower luminance of light source (LED).

(e) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

9.4 OTHERS

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, Variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time, it can be the situation when The image "sticks" to the screen.

(e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.