Technical Document

LCD Specification

LCD Group

LQ043T3DG02 LCD Module

Product Specification
May 2008

480 × 272 Wide Aspect LCD Module
featuring 480 nits brightness with
900:1 contrast. Full Specifications Listing.

SHARP

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APPROVED BY: T. Yamauchi		FILE No.
		ISSUED: May. 13. 2008
		PAGE : 31 pages
	MOBILE LIQUID CRYSTAL DISPLAY GROUP SHARP CORPORATION **SPECIFICATION**	APPLICABLE GROUP MOBILE LIQUID CRYSTAL DISPLAY GROUP

DEVICE SPECIFICATION FOR

TFT-LCD module

MODEL No. LQ043T3DG02

These parts have corresponded with the RoHS directive.

CUSTOMER'S APPROVAL

DATE

BY

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RECORDS OF REVISION

MODEL No：LQ043T3DG02

SPEC No ：LD－20503A

DATE	NO.	PAGE	SUMMARY	NOTE
2008. 5. 13		-	-	1st Issue

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1. Applicable Scope

This specification is applicable to TFT-LCD Module “LQ043T3DG02” .

2. General Description

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, Input FPC, a back light unit.

Graphics and texts can be displayed on a 480 x 272 x RGB dots panel with about 262k colors by supplying 18bit data signals (6bit x RGB), four timing signals, 3wires 9 / 24bit serial interface signals, logic (Typ. +3.15V),analog (Typ. +3.15V) supply voltages for TFT-LCD panel driving and supply voltage for back light.

3. Mechanical (Physical) Specifications

Item	Specifications	Unit
Screen size	10.9 (4.3” type) diagonal	cm
Active area	95.04(H)×53.856(V)	mm
Pixel format	480(H) x 272(V)	Pixel
	1Pixel =R+G+B dots	
Pixel pitch	0.198(H) x 0.198(V)	mm
Pixel configuration	R,G,B horizontal stripes	
Display mode	Normally white	
Unit outline dimensions	105.5(W) x 67.2(H) x 3.95(D)	mm
Mass	Approx.55	g
Surface hardness	2H	
Surface treatment	Anti glare	

*The above-mentioned table indicates module sizes without some projections and FPC.
For detailed measurements and tolerances, please refer to 18. Outline Dimensions..

4. Input Terminal Names and Functions

Recommendation CN：[HIROSE] FH26G-67S-0.3SHBW(05)

Pin No	Symbol	I/O	Description	Remarks
1	LED_C (-)	-	Power supply for LED (Cathode)	
2	LED_A(+)	-	Power supply for LED (Anode)	
3	DGND1	-	Digital Ground	
4	X1(R)	O	Touch Panel Right Electrode	
5	Y2(B)	O	Touch Panel Bottom Electrode	
6	X2(L)	O	Touch Panel Left Electrode	
7	Y1(T)	O	Touch Panel Top Electrode	
8	AGND1	-	Analog Ground	
9	V_{GH}	-	Connect to a Stabilizing capacitor	Note 3
10	C3P	-	Connect a Booster capacitor to C3N	Note 2
11	C3N	-	Connect a Booster capacitor to C3P	Note 2
12	C2P	-	Connect a Booster capacitor to C2N	Note 2
13	C2N	-	Connect a Booster capacitor to C2P	Note 2
14	V_{GL}	-	Connect a Stabilizing capacitor to GND	Note 3
15	C1P	-	Connect a Booster capacitor to C1N	Note 2
16	C1N	-	Connect a Booster capacitor to C1P	Note 2
17	AGND2	-	Analog Ground	
18	V_{CIX2}	-	Connect a Stabilizing capacitor to GND	Note 3
19	C11P	-	Connect a Booster capacitor to C11N	Note 2
20	C11N	-	Connect a Booster capacitor to C11P	Note 2
21	V_{CI}	-	Booster input voltage pin	Note 3
22	SDO	O	Data output pin in serial mode	
23	AGND3	-	Analog Ground	
24	V_{CIM}	-	Connect a Stabilizing capacitor to GND	Note 3
25	CXP	-	Connect a Booster capacitor to CXN	Note 2
26	CXN	-	Connect a Booster capacitor to CXP	Note 2
27	TEST	O	TEST	Note 1
28	RESB	I	System reset	
29	DGND2	-	Digital Ground	
30	V_{DDIO}	-	Voltage input pin for logic I/O	
31	V_{CORE}	-	Connect a Stabilizing capacitor to GND	Note 3
32	DGND3	-	Digital Ground	
33	DGND4	-	Digital Ground	
34	CSB	I	Chip select pin of serial interface	
35	SDI	I	Data input pin in serial mode	
36	SCK	I	Clock input pin in serial mode	
37	STYPE	I	9bit / 24bit select pin of serial interface	‘L’=24bit / ‘H’=9bit
38	DEN	I	Display enable	
39	B5	I	BLUE data signal(MSB)	
40	B4	I	BLUE data signal	
41	B3	I	BLUE data signal	

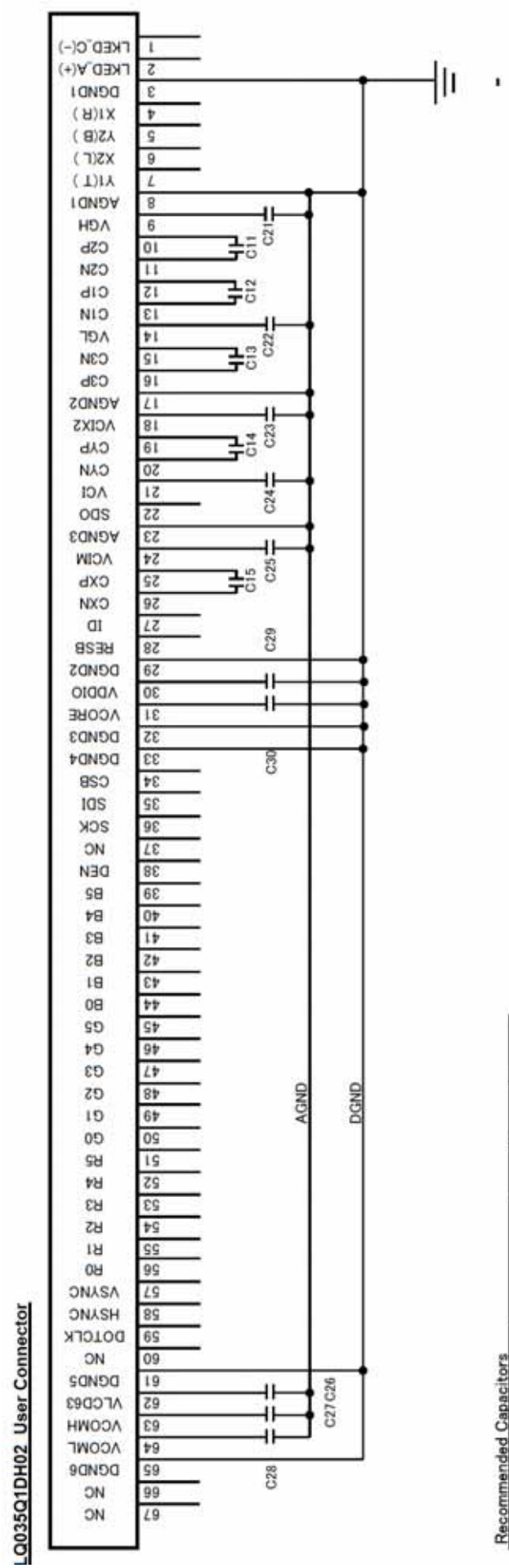
Pin No.	Symbol	I/O	Description	Remarks
42	B2	I	BLUE data signal	
43	B1	I	BLUE data signal	
44	B0	I	BLUE data signal(LSB)	
45	G5	I	GREEN data signal(MSB)	
46	G4	I	GREEN data signal	
47	G3	I	GREEN data signal	
48	G2	I	GREEN data signal	
49	G1	I	GREEN data signal	
50	G0	I	GREEN data signal(LSB)	
51	R5	I	RED data signal(MSB)	
52	R4	I	RED data signal	
53	R3	I	RED data signal	
54	R2	I	RED data signal	
55	R1	I	RED data signal	
56	R0	I	RED data signal(LSB)	
57	VSYNC	I	Frame synchronization signal	
58	HSYNC	I	Line synchronization signal	
59	DOTCLK	I	Dot-clock signal	
60	NC	-	Non connected	
61	DGND5	-	Digital Ground	
62	V_{LCD63}	-	Connect a Stabilizing capacitor to GND	Note 3
63	V_{COMH}	-	Connect a Stabilizing capacitor to GND	Note 3
64	V_{COML}	-	Connect a Stabilizing capacitor to GND	Note 3
65	DGND6	-	Digital Ground	
66	NC	-	Non connected	
67	NC	-	Non connected	

Note 1) this pin should be opened.

Note 2) Booster Capacitors

Note 3) Stabilization Capacitors

External recommended condenser



Recommended Capacitors

Ref No.	Capacitance	Rated Voltage	Temperature Characteristic
C11	0.22uF	16V	B(JIS) or X5R(EIA)
C12	0.22uF	16V	B(JIS) or X5R(EIA)
C13	0.22uF	16V	B(JIS) or X5R(EIA)
C14	0.22uF	10V	B(JIS) or X5R(EIA)
C15	0.22uF	10V	B(JIS) or X5R(EIA)
C21	2.2uF	25V	B(JIS) or X5R(EIA)
C22	2.2uF	16V	B(JIS) or X5R(EIA)
C23	2.2uF	10V	B(JIS) or X5R(EIA)
C24	2.2uF	6.3V	B(JIS) or X5R(EIA)
C25	2.2uF	6.3V	B(JIS) or X5R(EIA)
C26	2.2uF	10V	B(JIS) or X5R(EIA)
C27	2.2uF	6.3V	B(JIS) or X5R(EIA)
C28	2.2uF	6.3V	B(JIS) or X5R(EIA)
C29	2.2uF	6.3V	B(JIS) or X5R(EIA)
C30	2.2uF	6.3V	B(JIS) or X5R(EIA)

[Note]
C1N/P,C2N/P,C3N/P,CXN/P,CYN/P are high voltage switching lines on FPC.
Surround/shield by AGND to avoid noise coupling to other pins.
Also aware the PCB design to avoid other components to be affected by noise on those dcdc pins

5. Absolute Maximum Ratings

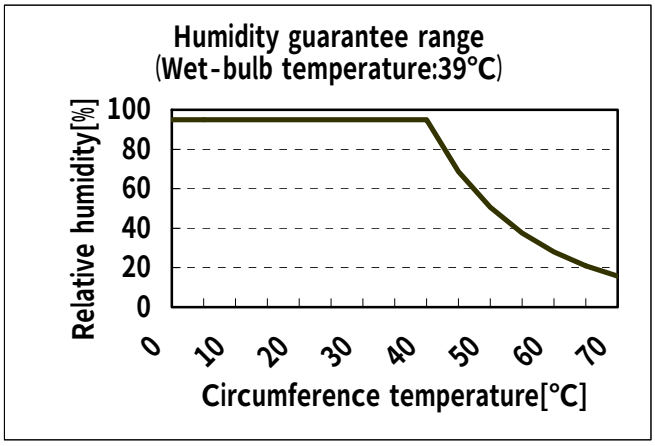
Item	Symbol	Conditions	Rated value	Unit	Remarks
Input voltage	VI	Ta = 25°C	-0.3 ~ V_{DDIO}+0.3	V	Note 1
Logic I/O power supply voltage	V_{DDIO}	Ta = 25°C	-0.3 ~ +4.0	V	
Analog power supply voltage	V_{CI}	Ta = 25°C	AGND-0.3 ~ +5.0	V	
Temperature for storage	Tstg	-	-30 ~ +85	°C	Note 2
Temperature for operation	Topr	-	-10 ~ +70	°C	Note 3
LED input electric current	I_{LED}	Ta = 25°C	35	mA	Note 4
LED electricity consumption	P_{LED}	Ta = 25°C	123	mW	Note 4

Note 1) RESB, CSB, SDI, SCK, DEN, B5 to B0, G5 to G0, R5 to R0, VSYNC, HSYNC, DOTCLK

Note 2) Humidity: 95%RH Max. (Ta≦40°C)

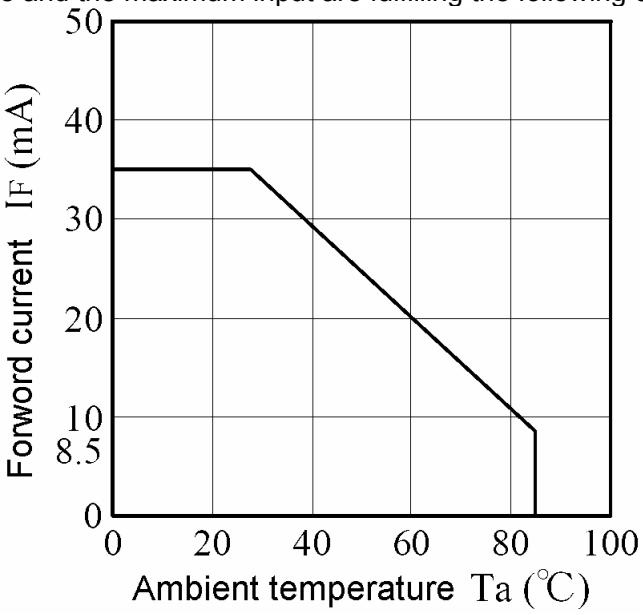
Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

Note 3) Ambient temperature prescribes.



Note 4) Power consumption of one LED (Ta = 25°C). (use 9 pieces LED)

Ambient temperature and the maximum input are fulfilling the following operating conditions.



Ambient temperature and the maximum input

6. Electrical Characteristics

6-1. TFT LCD Panel Driving

Ta = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Logic I/O power supply	DC voltage	V_{DDIO}	+3.0	+3.15	+3.3	V	
	DC current	I_{VDDIO}	-	1	2	mA	Note 1
Analog power supply	DC voltage	V_{CI}	+3.0	+3.15	+3.3	V	
	DC current	I_{VCI}	-	12.5	20.0	mA	Note 1
Permissive input Ripple voltage		$V_{RFVDDIO}$	-	-	100	mVp-p	Note 2
		V_{RFVCI}	-	-	100	mVp-p	Note 2
Logic Input Voltage	High	V_{IH}	0.8 x V_{DDIO}	-	V_{DDIO}	V	Note 3
	Low	V_{IL}	0	-	0.2 x V_{DDIO}	V	Note 3
Logic input Current		I_{IH} / I_{IL}	-1	-	1	μA	Note 3

Note 1) V_{DDIO} = V_{CI} = +3.3V, f_{VSYNC} = 60Hz
Current situation for I_{VDDIO}: Black & White checker flag pattern
Current situation for I_{CI}: All black pattern

Note 2) V_{DDIO} = V_{CI} = +3.3V

Note 3) RESB, CSB, SDI, SCK, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

6-2. Power up sequence

V_{DDIO} / V_{CI} ON (hold RESB = “L”)

↓

Wait min. 1us

↓

Hard Reset (RESB “L” → “H”)

↓

Wait min.1ns

↓

Enter the Sleep Mode

Reg. #	Register	Data	Remark
R28h	Power control 1	0006 h	
R29h	Power control 2	8000h	
R2Eh	Power control 3	B544h	
R2Dh	Power control 4	3F46 h	Note2

↓

Register setting

Reg. #	Register	Data	Remark
R01 h	Driver output control	230F h	Note 1
R02 h	LCD driving waveform control	0C02 h	
R03 h	Power control 5	(040E h)	
R0B h	Frame cycle control	D000 h	
R0C h	Power control 6	0005 h	
R0D h	Power control 7	000F h	
R0E h	Power control 8	2B00 h	
R16 h	Pixel per line	EF8E h	Note 3
R17 h	Vertical porch	0003 h	Note 4
R1E h	Power control 9	0000 h	
R30 h	Gamma control 1	0000 h	
R31 h	Gamma control 2	0107 h	
R32 h	Gamma control 3	0000 h	
R33 h	Gamma control 4	0201 h	
R34 h	Gamma control 5	0607 h	
R35 h	Gamma control 6	0005 h	
R36 h	Gamma control 7	0707 h	
R37 h	Gamma control 8	0203 h	
R3A h	Gamma control 9	0F0F h	
R3B h	Gamma control 10	0F02 h	
R10 h	Power control 10	02CC h	
R26 h	Power control 11	2800 h	
R15 h	Power control 12	0090 h	
R2C h	Power control 13	3BBD h	

↓

Wait min.200ns

↓

Display Data Start (VSYNC, HSYNC, DOTCLK)

↓

Exit the Sleep Mode

Reg. #	Register	Data	Remark
R2Dh	Power control 4	3F44 h	
R29h	Power control 2	FFFEh	

↓

Wait min.1s

↓

Back Light ON

↓

Display ON

Note 1)

Driver Output Control (R01h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RL	REV	0	0	0	TB	1	0	0	0	0	1	1	1	1
POR		0	0	1	0	0	0	1	1	0	0	0	0	1	1	1	1

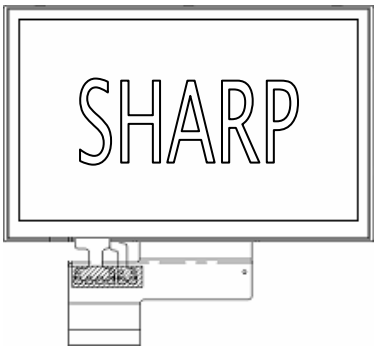
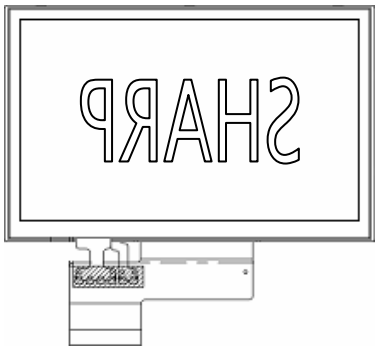
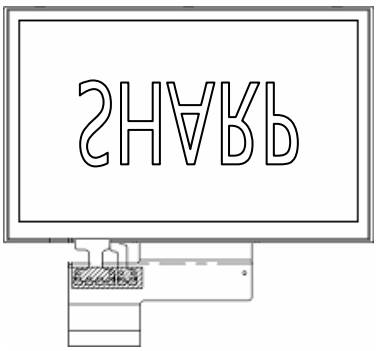
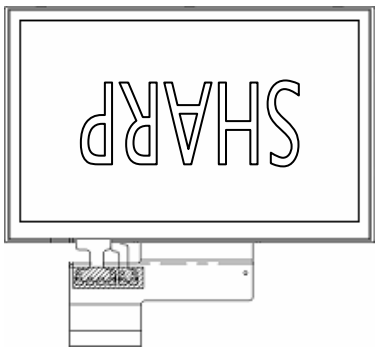
REV: Displays all character and graphics display sections with reversal when REV = “0”.

TB: Selects the output shift direction of the gate driver.

When TB = “”1”, Top shifts to Bottom. When TB = “0”, Bottom shifts to Top.

RL: Selects the output shift direction of the source driver.

When RL =”1”, Right shifts to Left. When TB = “1”, Left shifts to Right.

	RL = “0”	RL = “1”
TB = “1”		
TB = “0”		

Note 2)

Mode Control(R2Dh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	1	1	1	1	1	1	0	1	0	0	0	1	SHUT	0
POR		0	0	1	1	1	1	1	1	0	1	0	0	0	1	x	0

SHUT：SHUT=”0” : Normal Mode , SHUT=”1” : Sleep Mode.

Note 3)

Pixel per line (R16h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
POR		1	1	1	0	1	1	1	1	1	0	0	0	1	1	1	0

Note: Number of dotclk for hsync active low period must be smaller than that of HBP

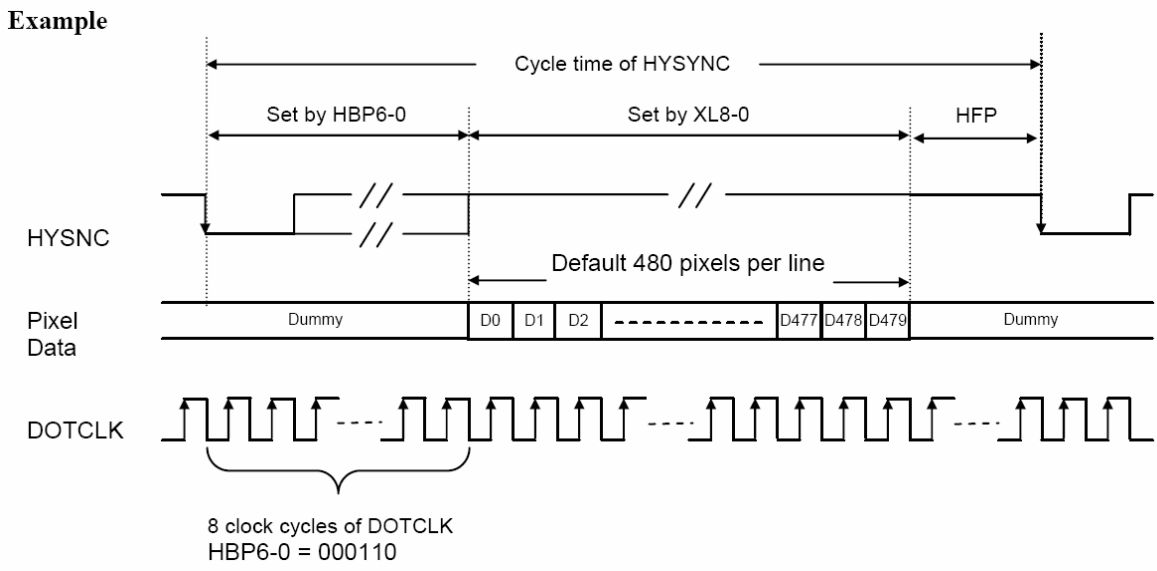
XL8-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				: : :					: Step = 1 :
1	1	1	0	1	1	1	1	0	479
1	1	1	0	1	1	1	1	1	480
1	1	1	1	*	*	*	*	*	Reserved

HBP6-0: Set the delay period from falling edge of HSYC signal to first valid data.

HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	0	2
0	0	0	0	0	0	1	3
0	0	0	0	0	1	0	4
				: : :			: Step = 1 :
1	1	1	1	1	0	1	127
1	1	1	1	1	1	0	128
1	1	1	1	1	1	1	129

Example



Note 4)

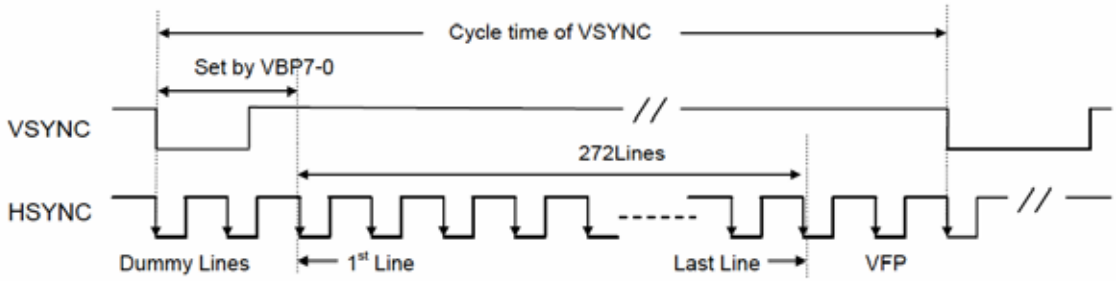
Vertical Porch (R17h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
POR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
				:				: Step = 1 :
1	1	1	0	0	0	0	0	224
1	1	1	0	0	0	0	1	225
1	1	1	1	*	*	*	*	Reserved

Example



6-3. Power down sequence

Back light OFF

↓

Write White Data (RGB Data: All “H” level)

↓

Wait min. 1 frame time

↓

Enter the Sleep Mode

Reg. #	Register	Data	Remark
R28h	Power control 1	0006 h	
R29h	Power control 2	8000h	
R2Eh	Power control 3	B544h	
R2Dh	Power control 4	3F46 h	

↓

Wait min. 3 frames time

↓

Display Data Stop (VSYNC, HSYNC, DOTCLK)

↓

V_{DDIO} / V_{CI} OFF

6-4. Enter sleep mode sequence

Back light OFF

↓

Write White Data (RGB Data: All “H” level)

↓

Wait min. 1 frame time

↓

Enter the Sleep Mode

Reg. #	Register	Data	Remark
R28h	Power control 1	0006 h	
R29h	Power control 2	8000 h	
R2Eh	Power control 3	B544h	
R2Dh	Power control 4	3F46 h	

↓

Wait min. 3 frames time

↓

Display Data Stop (VSYNC, HSYNC, DOTCLK)

6-5. Exit sleep mode sequence

Display Data Start (VSYNC, HSYNC, DOTCLK)

↓

Exit the Sleep Mode

Reg. #	Register	Data	Remark
R28h	Power control 1	0006 h	
R2Dh	Power control 4	3F44 h	
R29h	Power control 2	FFFEh	

↓

Wait min.1s

↓

Back light ON

↓

Display On

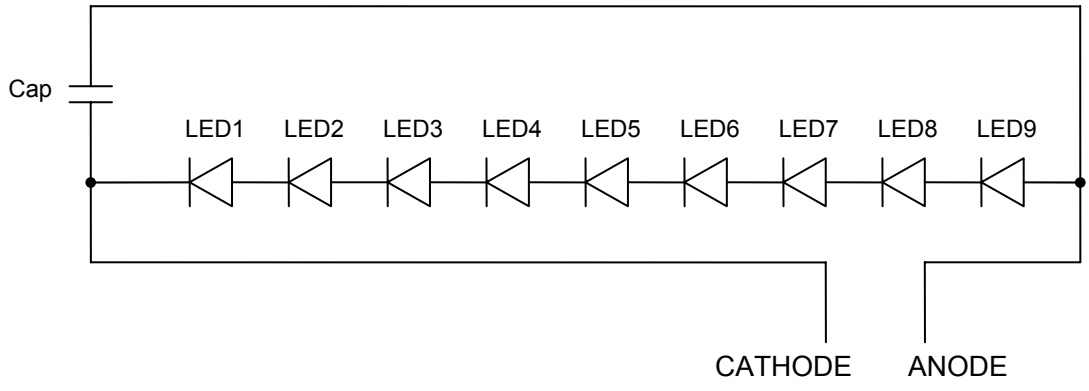
6-6. Back light driving

The back light system has 9 pieces LED

[LED type; NSSW006T (Nichia)]

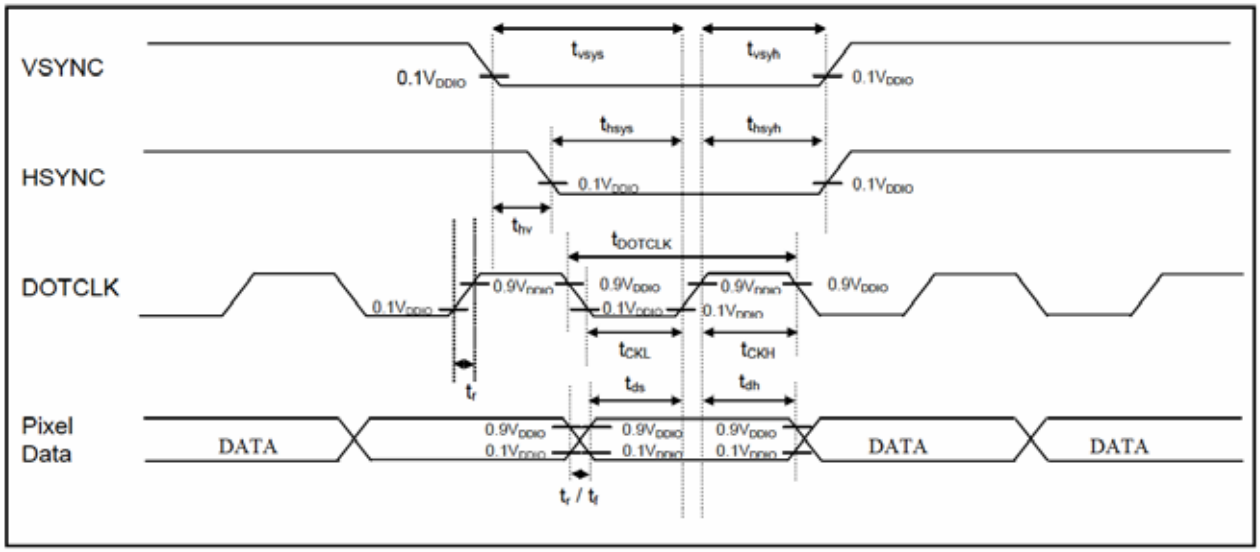
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Rated Voltage	V_{BL}	-	28.8	31.5	V	
Rated Current	I_L	-	20	-	mA	Ta=25°C
Power consumption	W_L	-	576	-	mW	

[LED-FPC circuit]



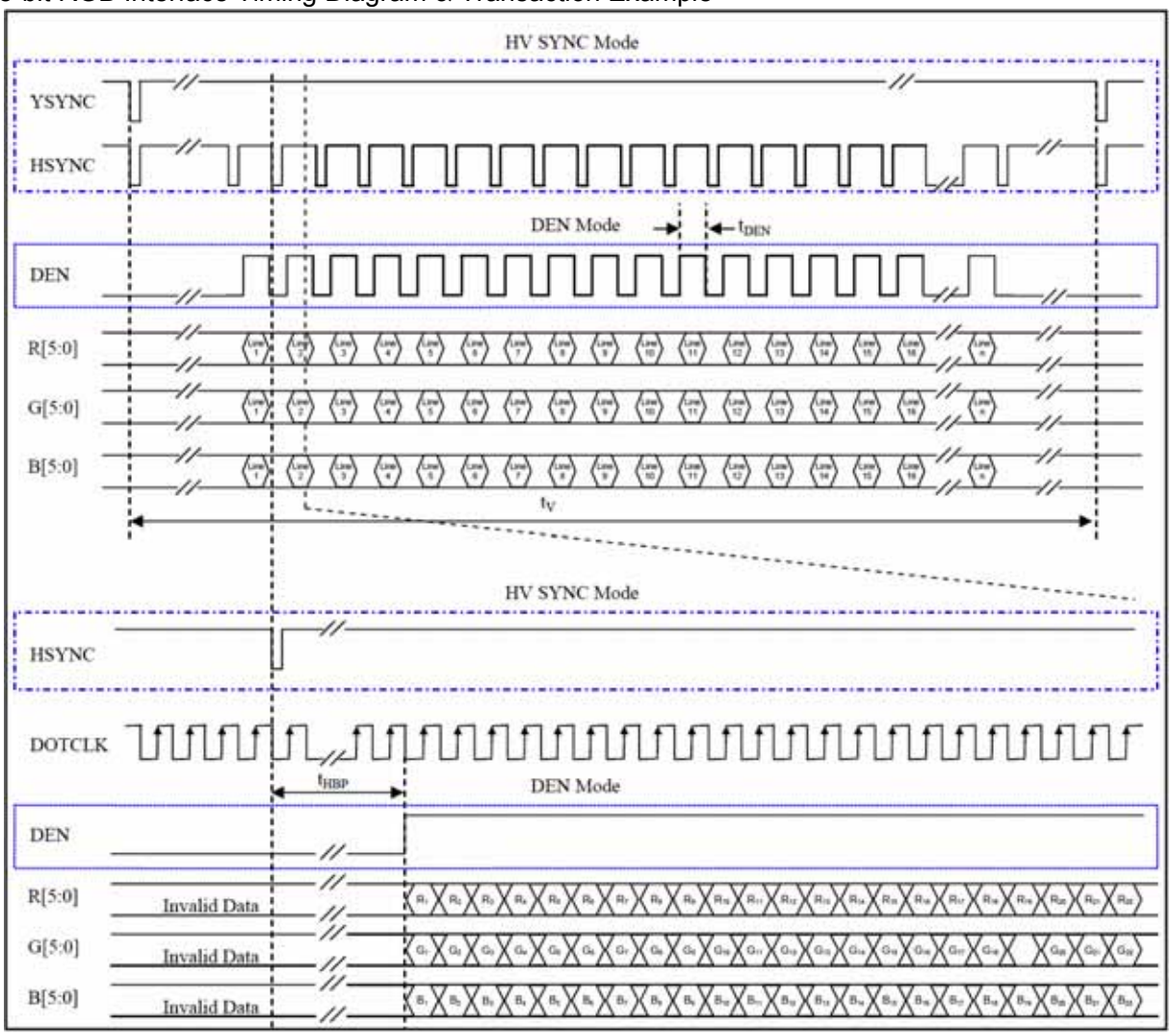
7. Timing characteristics of input signals

7-1. Pixel Clock Timing



Characteristics	Symbol	Min	Typ	Max	Units
DOTCLK Frequency	f_{DOTCLK}	-	-	8.69	MHz
DOTCLK Period	t_{DOTCLK}	115	-	-	nSec
Pixel Clock Period	t_{PIXCLK}	-	1	-	t_{DOTCLK}
Pixel Clock Frequency	f_{PIXCLK}	-	-	8.69	MHz
Vertical Sync Setup Time	t_{vsys}	5	-	-	nSec
Vertical Sync Hold Time	t_{vsyh}	5	-	-	nSec
Horizontal Sync Setup Time	t_{hsys}	5	-	-	nSec
Horizontal Sync Hold Time	t_{hsyh}	5	-	-	nSec
Phase difference of Sync Signal Falling Edge	t_{hv}	0	-	480	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	18	-	-	nSec
DOTCLK High Period	t_{CKH}	18	-	-	nSec
Data Setup Time	t_{ds}	10	-	-	nSec
Data Hold Time	t_{dh}	15	-	-	nSec
Reset Pulse Width	t_{RES}	10	-	-	uSec
Rise / Fall Time	t_r / t_f	5	-	25	nSec

7-2. 18-bit RGB Interface Timing Diagram & Transaction Example



Characteristics		Symbol	HV SYNC Mode	Units
DOTCLK Frequency		$1/t_{DOTCLK}$	8.54	MHz
Horizontal	One Line Period	t_H	512	t_{DOTCLK}
	Active Data Period	t_{data}	480	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	16	t_{DOTCLK}
	Horizontal Front Porch	t_{vsys}	16	t_{DOTCLK}
Vertical	One Field Period	t_V	278	t_H
	Active Line Period	t_{AL}	272	t_H
	Vertical Back Porch	t_{VBP}	4	t_H
	Vertical Front Porch	t_{VFP}	2	t_H

The formula of setting for control signals:

$1/t_{DOTCLK}, t_{HBP}, t_{HFP}, t_{VBP}, t_{VFP}$.

f_V=60±5Hz :Vertical Frequency(Refresh)

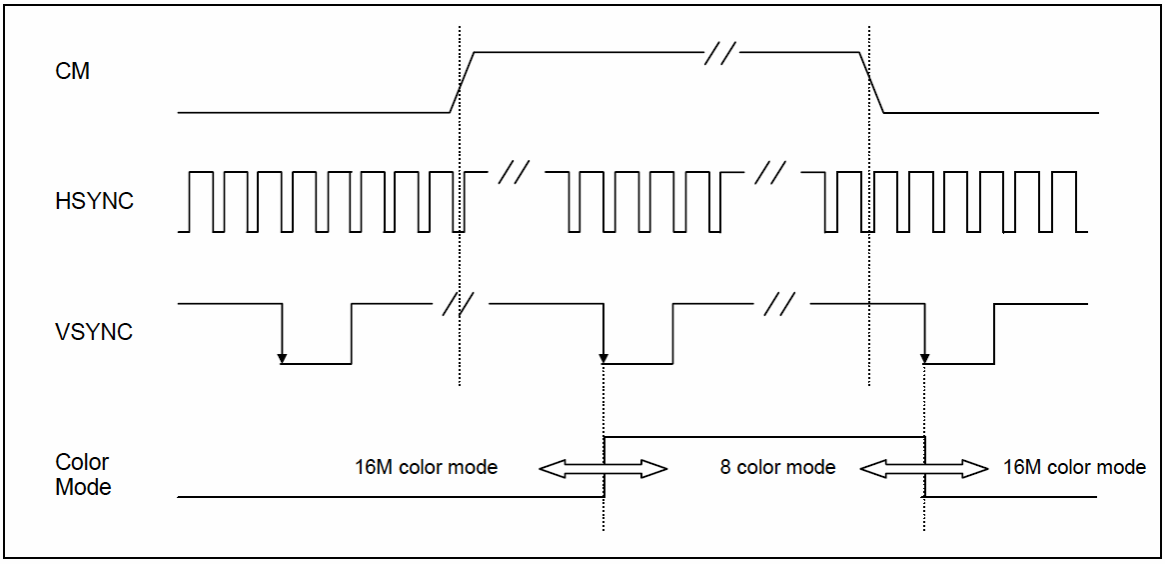
$1/t_{DOTCLK}=f_{DOTCLK}$

$f_V=f_{DOTCLK}/(t_H \times t_V)$

$t_V=(t_{VBP}+t_{AL}+t_{VFP}) \leqq 512$

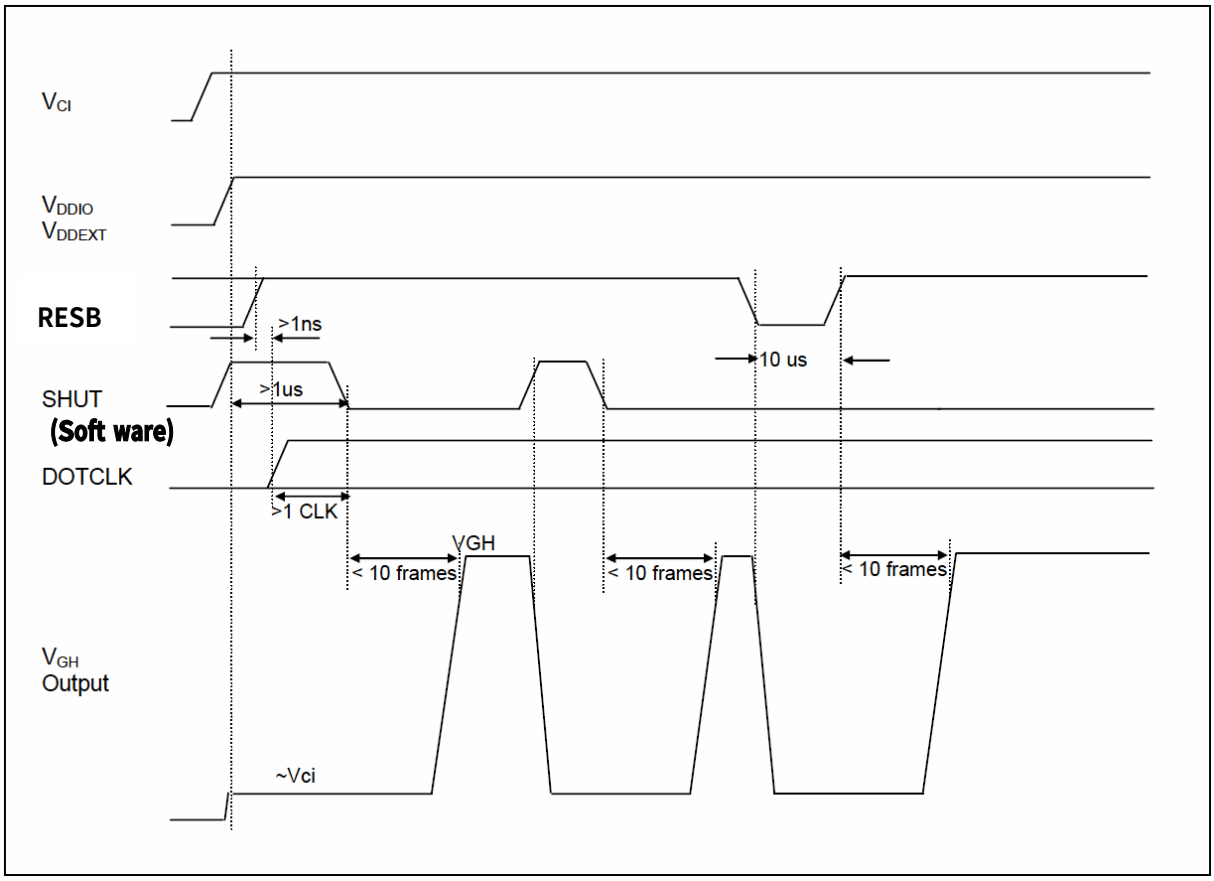
$t_H=(t_{HBP}+t_{Data}+t_{VFP}) \leqq 1024$

7-3. Color Mode Conversion Timing



Note: **The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.**

7-4. VGH Output against SHUT & RESB



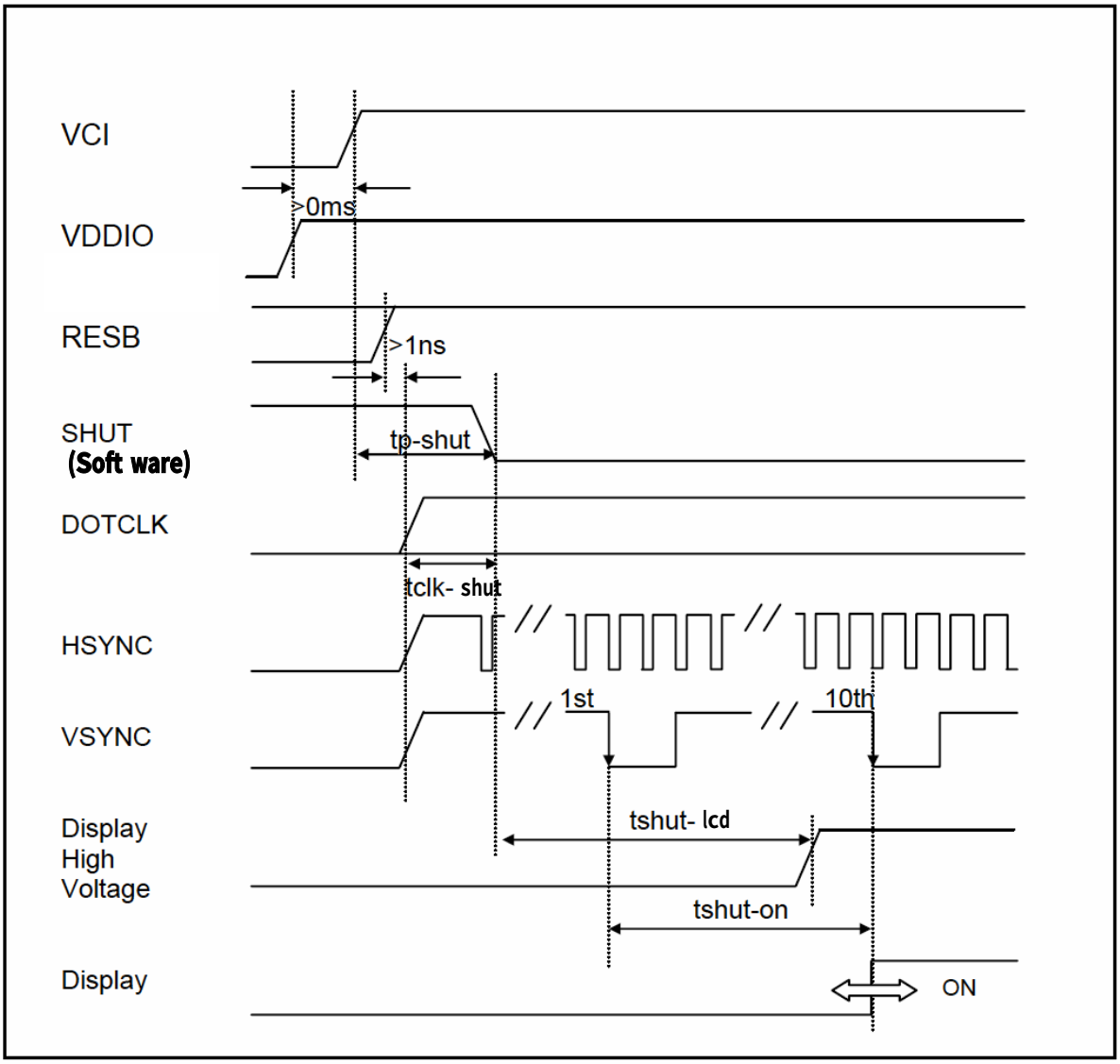
Note1: **The minimum cycle time of SHUT is 10 + 2 frames.**

Note2: **DOTCLK must be provided for boosting of V_{GH}. The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.**

Note3: **V_{GH} will be forced to V_{CI} at the low stage of RESB**

Note4: **The minimum pulse width of RESB is 10us.**

7-5. Power Up Sequence

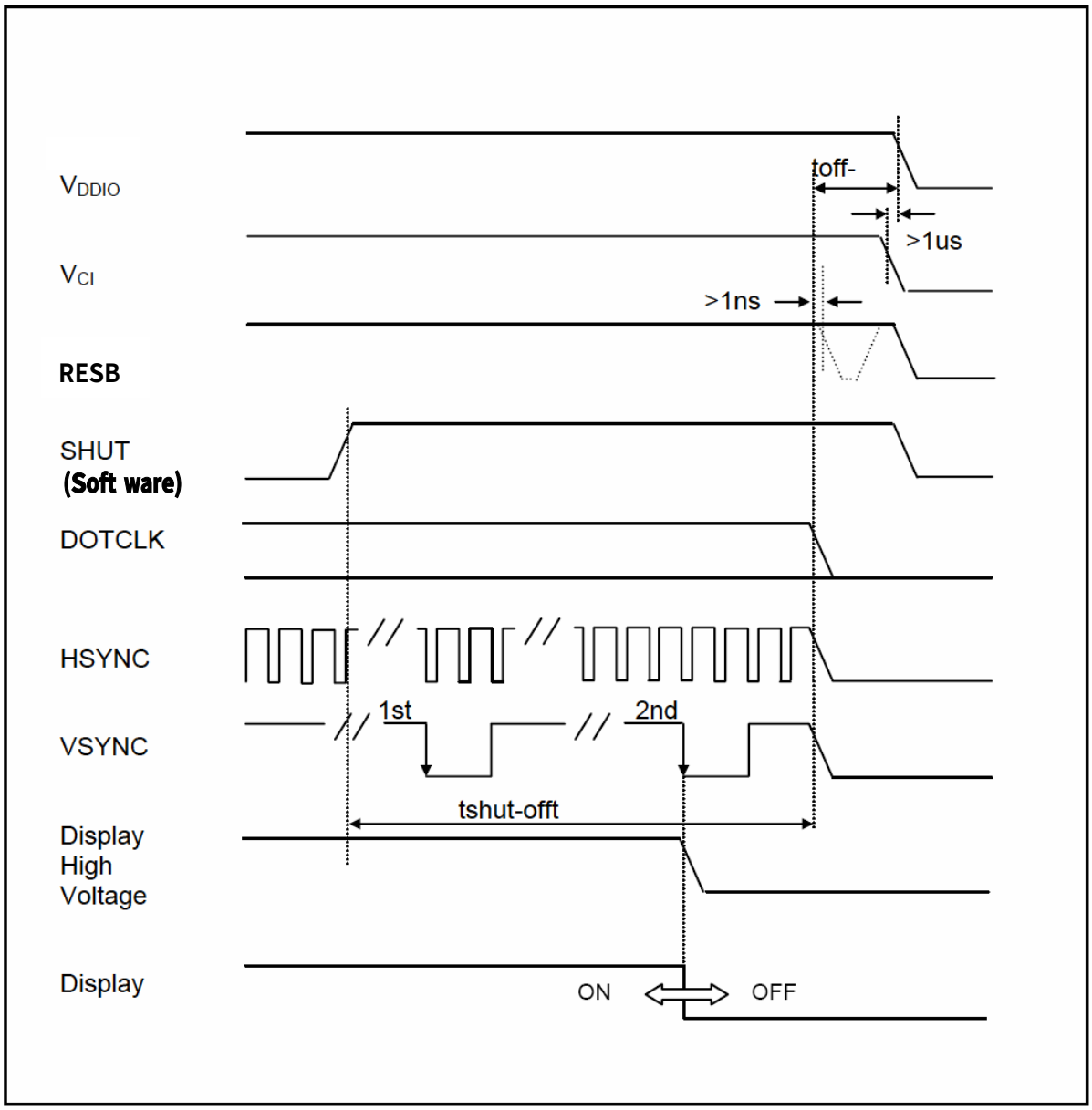


Characteristics	Symbol	MIN	TYP	MAX	Units
V_{DDIO} on to falling edge of SHUT	tp-shut	1	-	-	µsec
Start of DOTCLK to SHUT low	tclk-shut	1	-	-	DOTCLK
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	167	msec
Falling edge of SHUT to display start	tshut-on	-	-	10	frame
-- 1 line: 512 clk -- 1 frame: 278 line -- PIXCLK = 8.5MHz		-	167	-	msec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

7-6. Power Down Sequence



Characteristics	Symbol	MIN	TYP	MAX	Units
Rising edge of SHUT to display off -- 1 line: 512 clk -- 1 frame: 278 line -- PIXCLK = 8.5 MHz	tshut-off	2	-	-	frame
		33.4	-	-	msec
Input-signal-off to V_{DDIO} off	toff-vdd	1	-	-	µsec

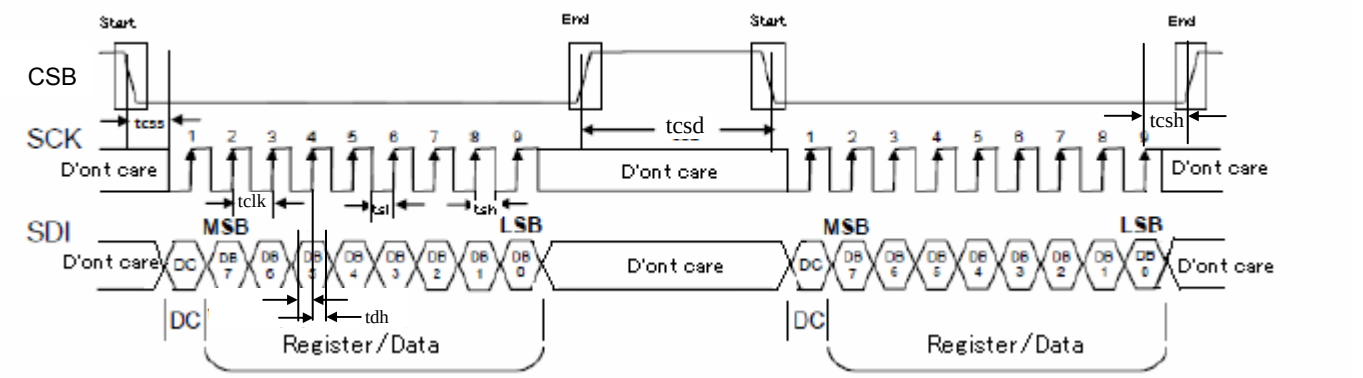
Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

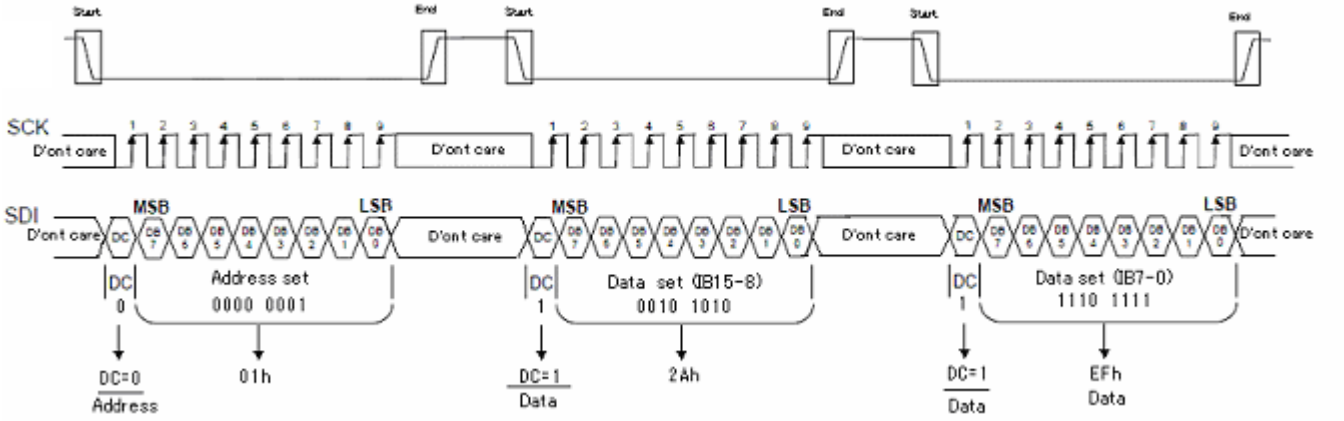
Note3: If RESB signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

7-7. SPI Interface Timing Diagram & Transaction Example

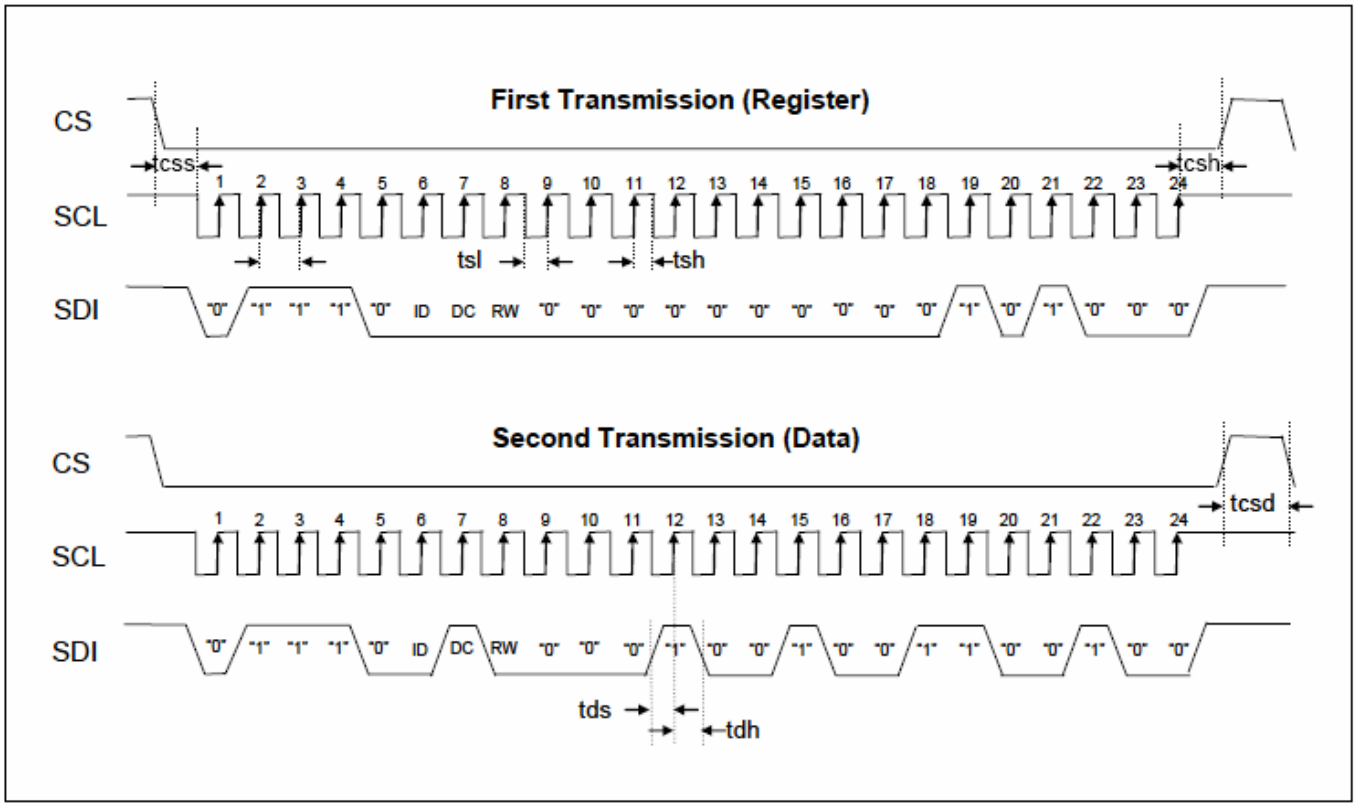
1) 3wire 9bit data



The example transmit “0x2AEFh” to register R01h.

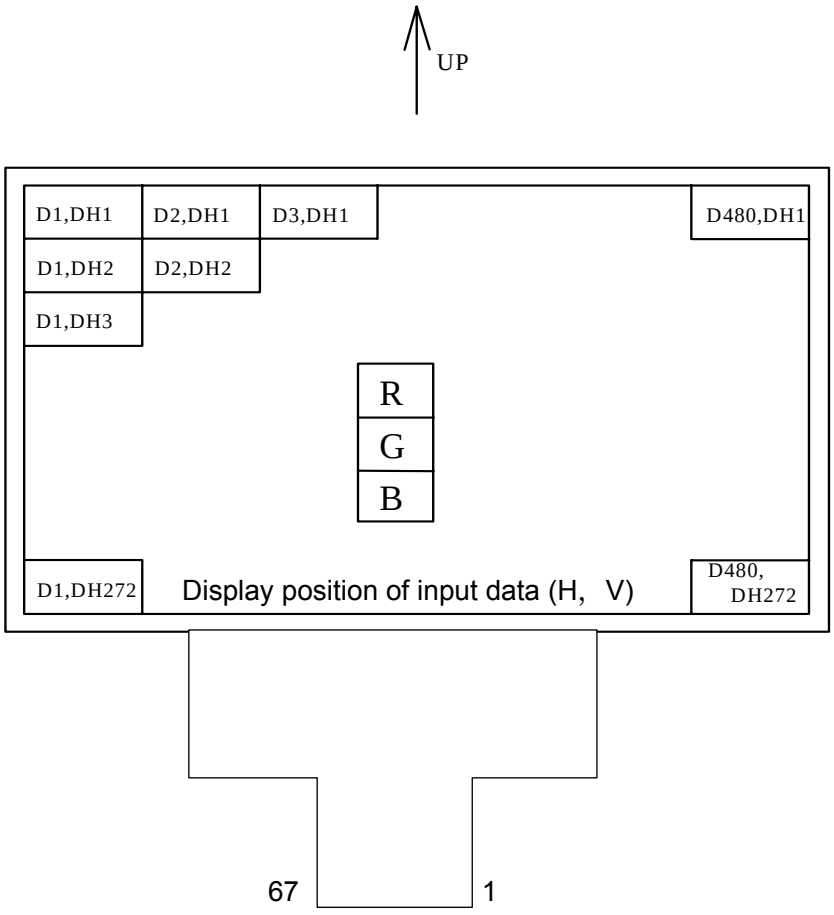


2) 3wire 24bit data



Characteristics	Symbol	MIN	TYP	MAX	Units
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	nsec
Clock Low Width	tsl	25	-	-	nsec
Clock Hifh Width	tsh	25	-	-	nsec
Chip Select Setup Time	tcss	5	-	-	nsec
Chip Select Hold Time	tcsh	10	-	-	nsec
Chip Select High Delay Time	tcsd	20	-	-	nsec
Data Setup Time	tds	5	-	-	nsec
Data Hold Time	tdh	15	-	-	nsec

7-8. Input Data Signals and Display Position on the screen



8. Input Signals, Basic Colors and Gray Scale of Each Color

	Colors & Gray Scale	Gray Scale	Date signal																	
			R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
			LSB					MSB	LSB					MSB	LSB					MSB
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	—	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	—	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	—	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	—	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓				↓						↓						↓		
	⇩	↓				↓						↓						↓		
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals.
According to the combination of 18 bit data signals, the 262k color display can be achieved on the screen.

9. Optical Characteristics

Module characteristics

Ta = 25°C, V_{DDIO} = +3.3V, V_{CI} = +3.3V

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ21	CR＞10	-	80	-	deg.	[Note1,4]
		θ22		-	80	-	deg.	
	Vertical	θ11		-	60	-	deg.	
		θ12		-	80	-	deg.	
Contrast ratio		CR	Optimum viewing angle	500	900	-	-	[Note2,4]
Response Time	Rise	τr	θ=0°	-	8	20	ms	[Note3,4]
	Decay	τd		-	21	40	ms	
Chromaticity of White		x		0.26	0.31	0.36	-	[Note4]
		y		0.29	0.34	0.39	-	
Luminance of white		X_{L1}		350	480	-	cd/m²	I_{LED}=20mA

* The optical characteristics measurements are operated under a stable luminescence (I_{LED} = 20mA) and a dark condition. (Refer to Fig.2-1,2-2)

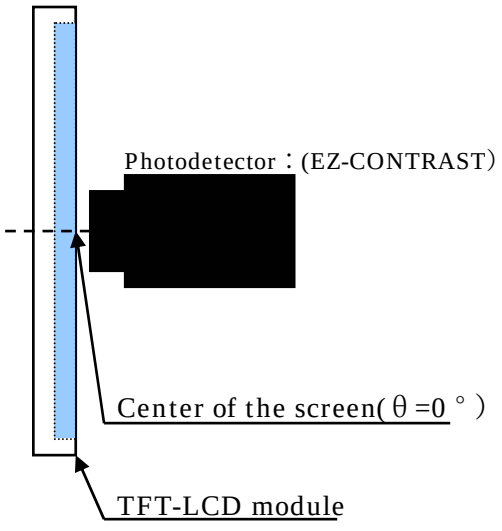


Fig.2-1 Viewing angle range/Response time measurement method

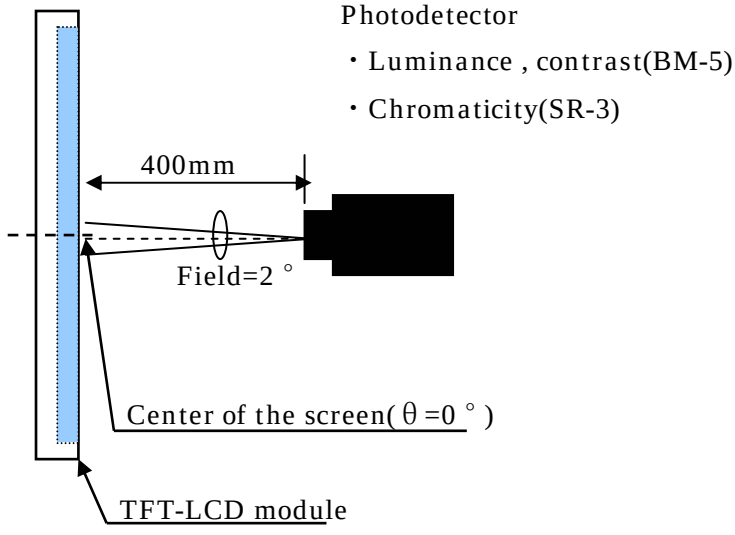
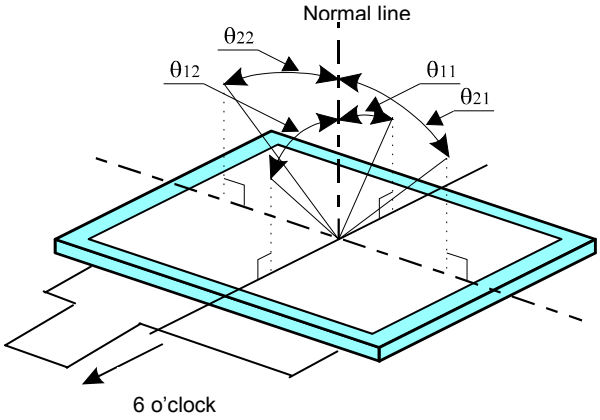


Fig2-2 Luminance/Contrast/Chromaticity measurement method

[Note1] Definitions of viewing angle range



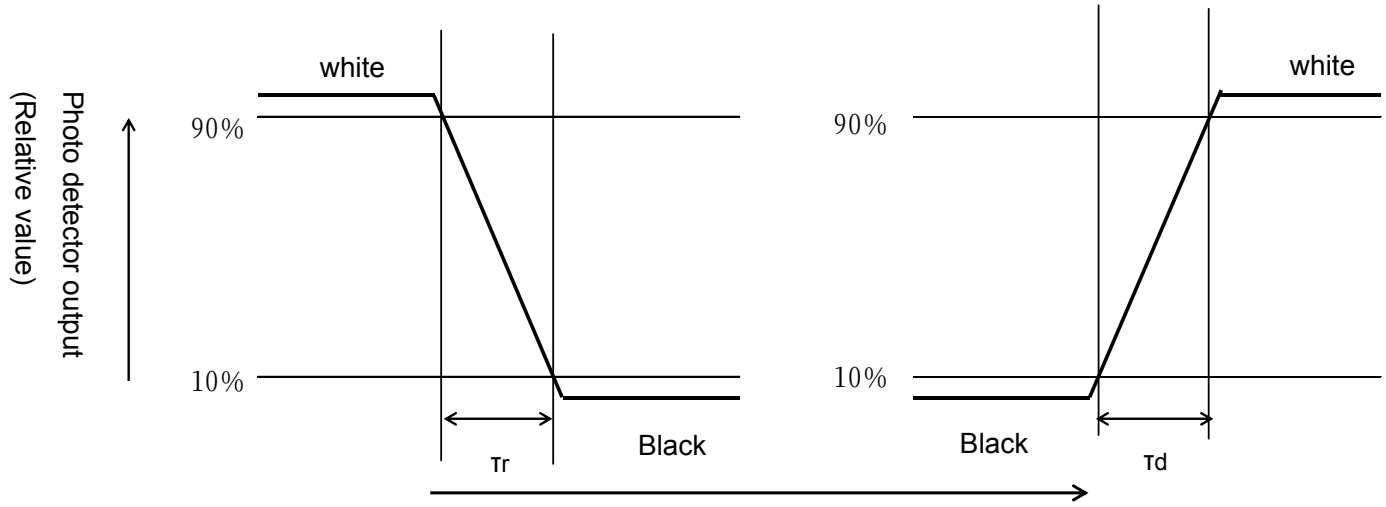
[Note2] Definition of contrast ratio

The contrast ratio is defined as the following:

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note3] Definition of response time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white"



[Note4] This shall be measured at center of the screen.

10. Handling of modules

10-1. Inserting the FPC into its connector and pulling it out.

1) Be sure to turn off the power supply and the signals when inserting or disconnecting the cable.
2) Please insert for too much stress not to join FPC in the case of insertion of FPC.

10-2. About handling of FPC

1) The bending radius of the FPC should be more than 0.6mm, and it should be bent evenly.
2) Do not dangle the LCD module by holding the FPC, or do not give any stress to it.

10-3. Mounting of the module

1) The module should be held on to the plain surface. Do not give any warping or twisting stress to the module.
2) Please consider that GND can ground a modular metal portion etc. so that static electricity is not charged to a module.

10-4. Cautions in assembly / Handling pre cautions.

As the polarizer can be easily scratched, be most careful in handling it.

1) Work environments in assembly.
   Working under the following environments is desirable:
   a) Implement more than 1MΩ conductive treatment (by placing a conductive mat or applying conductive paint) on the floor or tiles.
   b) No dusts come in to the working room. Place an adhesive, anti-dust mat at the entrance of the room.
   c) Humidity of 50 to 70% and temperature of 15 to 27°C are desirable.
   d) All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without fail.
   e) Use a blower for electrostatic removal. Set it in a direction slightly tilt downward so that each Module can be well subjected to its wind. Set the blower at an optimum distance between the blower and the module.
2) How the remove dust on the polarizer
   a) Blow out dust by the use of an N2 blower with antistatic measures taken. Use of an ionized air Gun is recommendable.
   b) When the panel surface is soiled, wipe it with soft cloth.
3) In the case of the module's metal part (shield case) is stained, wipe it with a piece of dry, soft cloth. If rather difficult, give a breath on the metal part to clean better.
4) If water dropped, etc. remains stuck on the polarizer for a long time, it is apt to get discolored or cause stains. Wipe it immediately.
5) As a glass substrate is used for the TFT-LCD panel, if it is dropped on the floor or hit by something hard, it may be broken or chipped off.
6) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

10-5. Others

1) Regarding storage of LCD modules, avoid storing them at direct sunlight-situation.
   You are requested to store under the following conditions:
   (Environmental conditions of temperature/humidity for storage)
   a) Temperature: 0 to 40°C
   b) Relative humidity : 95% or less

- As average values of environments (temperature and humidity) for storing, use the following control guidelines:
  Summer season: 20 to 35°C, 85% or less Winter season: 5 to 15°C, 85% or less
- If stored under the conditions of 40°C and 95% RH, cumulative time of storage must be less than 240 hours.

2) If stored at temperatures below the rated values, the inner liquid crystal may freeze, causing cell destruction. At temperatures exceeding the rated values for storage, the liquid crystal may become isotropic liquid, making it no longer possible to come back to its original state in some cases.
3) If the LCD is broken, do not drink liquid crystal in the mouth. If the liquid crystal adheres to a hand or foot or to clothes, immediately cleanse it with soap.
4) If a water drop or dust adheres to the polarizer, it is apt to cause deterioration. Wipe it immediately.
5) Be sure to observe other caution items for ordinary electronic parts and components.
6) If local pressure joins T/P surface for a long time, it will become the cause of generating of Newton's ring.

11. Reliability test items

No.	Test item	Conditions
1	High temperature storage test	Ta = 85°C 240h
2	Low temperature storage test	Ta = -30°C 240h
3	High temperature & high humidity operation test	Ta = 60°C ; 90%RH 240h (No condensation)
4	High temperature operation test	Ta = 70°C 240h
5	Low temperature operation test	Ta = -10°C 240h
6	Vibration test (non- operating)	Frequency range: 10 to 55Hz Stroke: 1.5mm Sweep time: 1minutes Test period: 2 hours for each direction of X,Y,Z
7	Shock test	Direction: ±X, ±Y, ±Z, Time: Third for each direction. Impact value: 980m/s², Action time 6ms
8	Thermal shock test	Ta=-10°C to 70°C /10 cycles (30 min) (30min)
9	Electro static discharge test	±200V/200pF(0Ω) to Terminals(Contact) (1 time for each terminals)

*Note Ta = Ambient temperature, Tp = Panel temperature

[Check items]

In the standard condition, there shall be no practical problems that may affect the display function.

12. Display Grade

The standard regarding the grade of color LCD displaying modules should be based on the delivery inspection standard.

13. Delivery Form

13-1. Carton storage conditions

1) Carton piling-up: Max 8 rows

2) Environments

Temperature: 0～40°C

Humidity: 65% RH or less (at 40°C)

There should be no dew condensation even at a low temperature and high humidity.

3) Packing form: As shown in Figure.

*Cartons are weak against damp, and they are apt to be smashed easily due to the compressive pressure applied when piled up. The above environmental conditions of temperature and humidity are set in consideration of reasonable pile-up for storage.

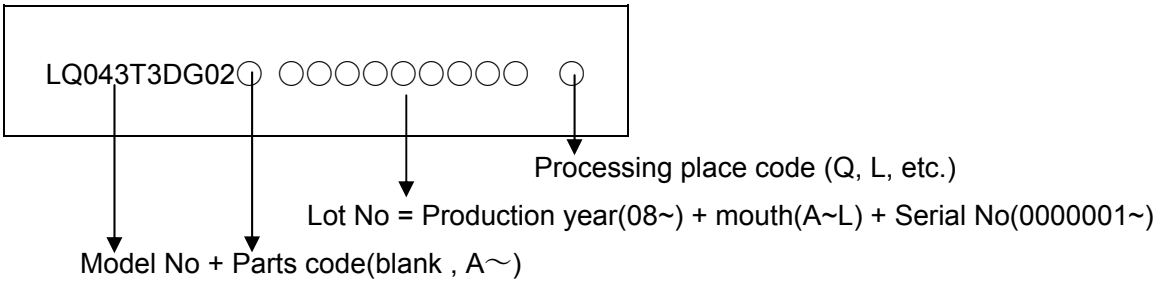
13-2. Packing composition

Name	quantity	Note
Carton size	1	575×360×225 (mm)
Tray	8	Material: Electrification prevention polypropylene
(The number of Module)	80	8 unit/tray: 80 unit/carton
Electrification prevention bag	2	Material: Electrification prevention polyethylene 680mm(length)×500mm(depth)×50μm(thin)

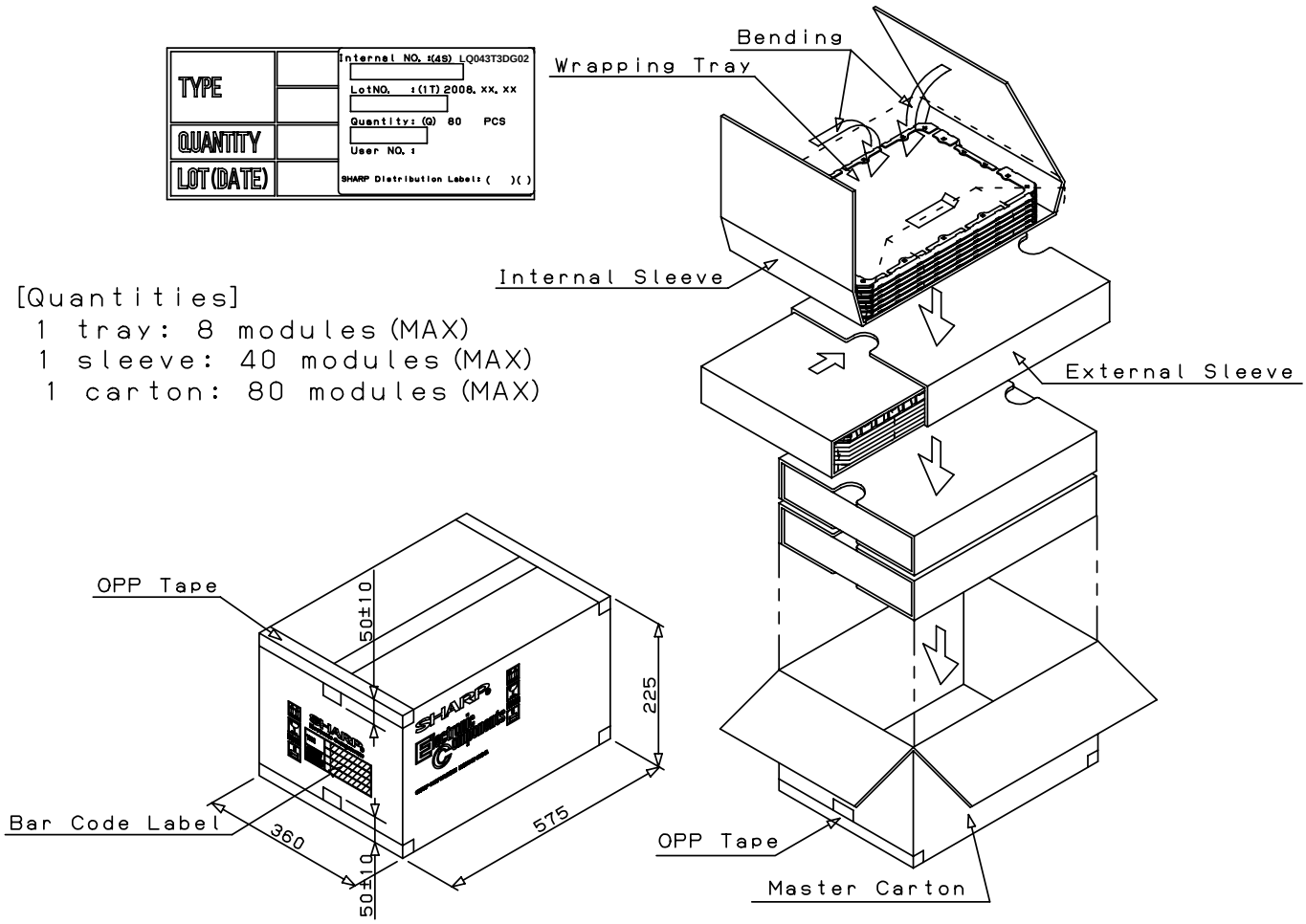
Carton weight (80 modules): Approx. 9.0 kg

14. Lot No. marking

The lot No. will be indicated on individual inkjet. The location is as shown



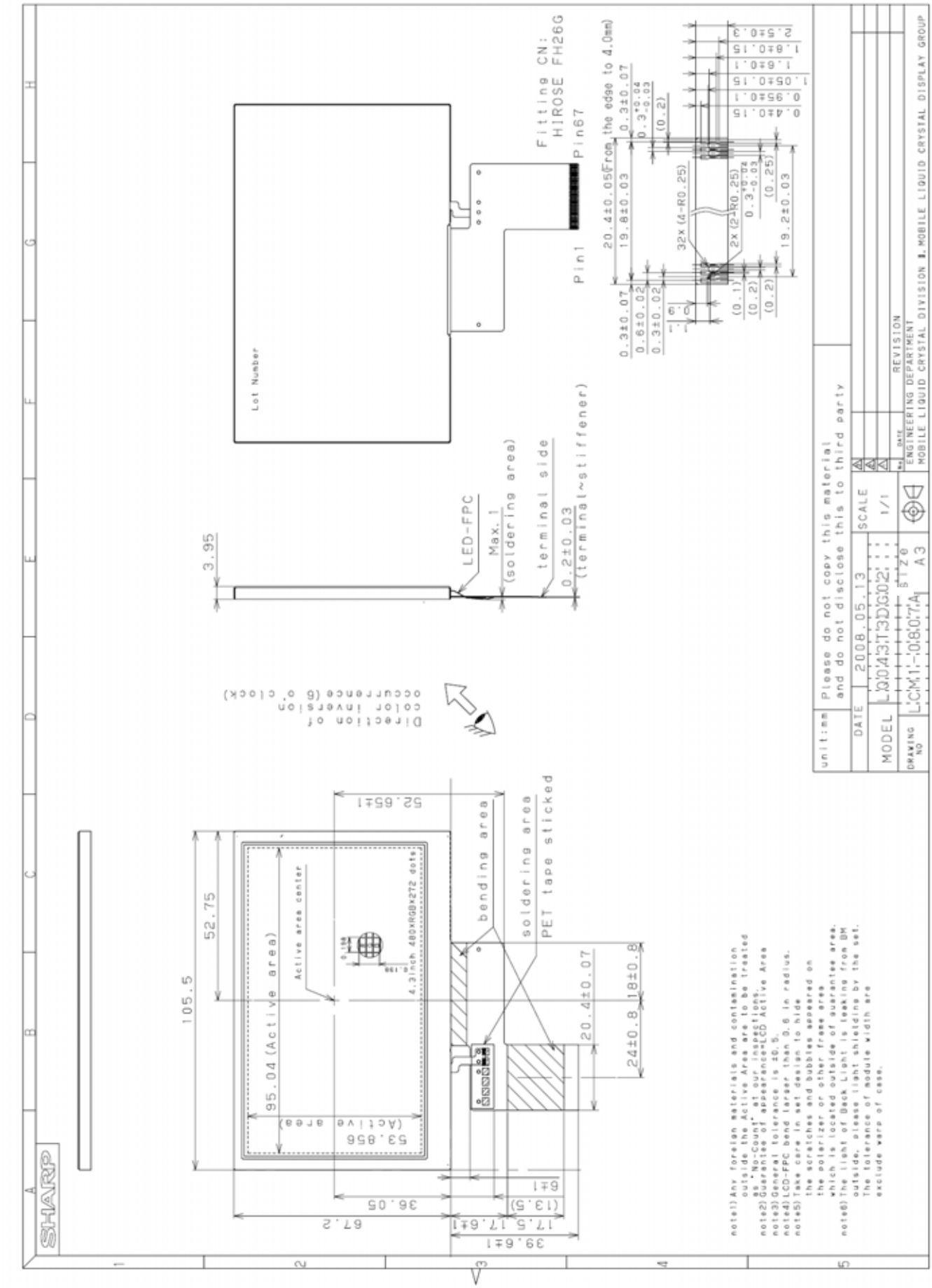
15. LCD module packing carton



16. Others

1) Disassembling the module can cause permanent damage and you should be strictly avoided.
2) Please be careful that you don't keep the screen displayed fixed pattern image for a long time, since retention may occur.
3) If you pressed down a liquid crystal display screen with your finger and so on, the alignment disorder of liquid crystal will occur. And then It will become display fault.
   Therefore, be careful not to touch the screen directly, and to consider not stressing to it.
4) If any problem arises regarding the items mentioned in this specification sheet or otherwise, it should be discussed and settled mutually in a good faith for remedy and/or improvement.

17. Outline Dimensions



Technical Document

LCD Specification

LCD Group

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