SPECIFICATION

For

APPROVAL

(¨) Preliminary Specification

( ) Final Specification

Title	20.1” UXGA TFT LCD

BUYER NAME	
MODEL NAME	

SUPPLIER	**LG.Philips LCD Co.,Ltd.**
MODEL NAME	**LM201U1**
SUFFIX	**A1**

SIGNATURE	**DATE**
/	
/	
/	

Please return 1 copy for our confirmation with your signature and comments.

APPROVED BY	**DATE**
S.H. Kang/G.Manager	
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CONTENTS

Record of Revisions

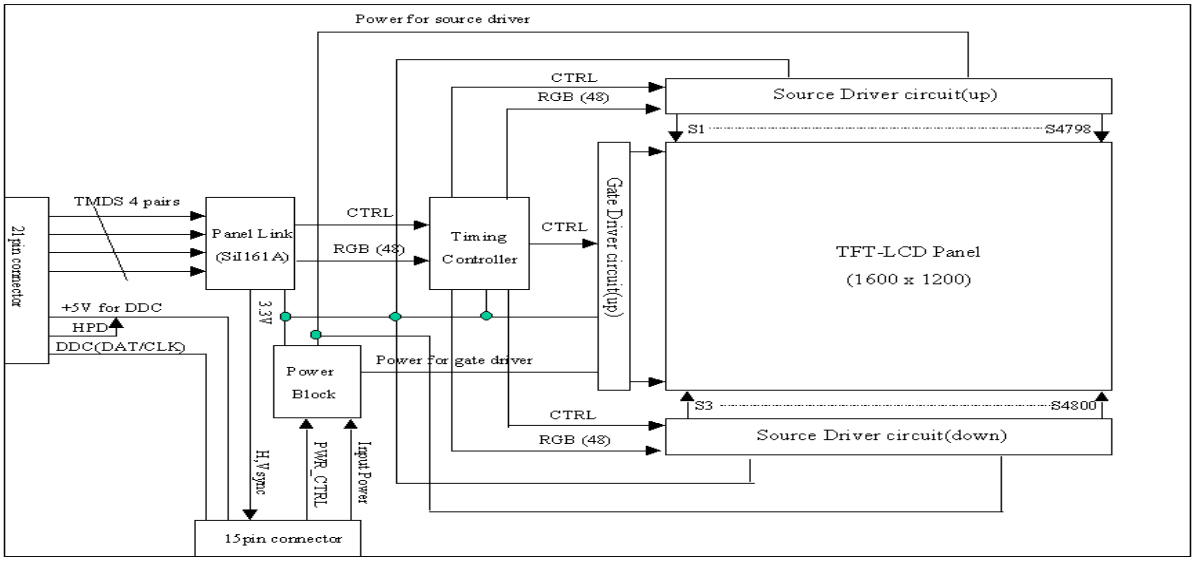
Version No.	Date	Page	Descriptions
0.0	JULY 10, 2000	-	First Draft, Preliminary

1. General Descriptions

The LM201U1 LCD is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp(CCFL) back light system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has a 20.1 inch diagonally measured active display area with UXGA resolution(1200 vertical by 1600 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16,777,216 colors.

The LM201U1 has been designed to apply the TMDS™(Transition Minimized differential Signaling) as the interface method to enables a simple and low-cost implementation in both the host and monitor.

The LM201U1 LCD is intended to support applications where high brightness, wide viewing angle, high color gamut, and high color depth are very important. In combination with the vertical arrangement of the sub-pixels, the LM201U1 characteristics provide an excellent flat panel display for office automation products such as monitors.



General Display Characteristics

Followings are general features of the model LM201U1 LCD;

Active display area	20.1 inches(56cm) diagonal
Outsize dimensions	467.80w * 361.0h * 32.0t(max)mm(Without Inverter)
Pixel pitch	0.255 mm × 0.255 mm
Pixel format	1600 horiz. By 1200 vert. pixels RGB vertical stripe arrangement
Color depth	8-bit, 16,777,216 colors
Display operating mode	transmissive mode, normally black
Surface treatments	hard coating(3H), anti-glare treatment of the front polarizer
Interface method	TMDS™ interface using SiI161 chips
Lamps	Six CCFL(Cold Cathode Fluorescent Lamp)

2. Absolute Maximum Ratings

Followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1 Absolute Maximum Ratings

Parameter	symbol	Values		Units	Notes
		Min.	Max.		
Power Input Voltage	V_{AA}	0	+21.0	V_{DC}	at 25℃
Control Logic Voltage	V_I	0	+5.5V	V_{DC}	
Operating Temperature	T_{OP}	5	+50	℃	1
Storage Temperature	T_{ST}	-20	+60	℃	1

Note: 1. The Relative Humidity must not exceed 90% non-condensing at temperatures of 40℃ or less.
At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

3. Electrical Specifications

3-1. Electrical Characteristics

The LM201U1 requires two power inputs. One input is employed to power the LCD electronics and to drive the voltages to drive the TFT array and liquid crystal. And the second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2 Electrical Characteristics:

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
MODULE:						
Power Supply Input Voltage	V_{AA}	17.1	18.0	18.9	V_{DC}	
Power Supply Input Current	I_{AA}	-	600	1000	mA	1
Control Logic Input High	V_{IH}	2.6	-	-	V_{DC}	
Control Logic Input Low	V_{IL}	-	-	0.8	V_{DC}	
Control Logic Output High	V_{OH}	2.5	-	-		
Control Logic Output Low	V_{OL}	-	-	0.5		
LAMP (each CCFL)						
Operating voltage	V_{BL}	910	770	710	V_{RMS}	2
Operating Current	I_{BL}	3.0	7.5	8.0	mA	3
Established Starting Voltage						4
at 25℃		1080	-	-	V_{RMS}	5
at 0℃		1500	-	-	V_{RMS}	
Operating Frequency		40	50	60	KHz	6
Discharge Stabilization Time	Ts	-	-	3	minutes	7
Life time	F_{BL}	30000	-	-	hours	8

Notes: 1. The input current shall be measured at V_{DD} of 18.0Vdc at 25℃, refresh rate of 60Hz, and pixel clock frequency of 162MHz under full white pattern(255gray).

2. The design of the inverter must have specifications for the lamp in LCD assembly. The performance of the lamp in LCD, for example, life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So all of the parameters of an inverter should be carefully designed as so not to produce too much leakage current from high voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter never occurs.
3. This data is for reference for inverter design.
4. The operating current shall be measured at the ground cable at ambient atmosphere of 25℃ and does not include loss of external inverter.
5. These value are measured at both end of lamp and are for reference for inverter design.
6. The output of the inverter must have symmetrical voltage waveform and symmetrical current waveform. Please do not use the inverter which has unsymmetrical waveform and spike wave. Lamp frequency may produce interference with Hsync frequency and therefore this lamp frequency shall be away as possible from the Hsync frequency and from its harmonics in order to prevent interference.
7. Ts is the time required for the brightness of the center of the lamp to be no less than 95%.
8. The life time is defined as the time at which brightness of lamp is 50% compare to that of initial value at the typical lamp current on condition of continuous operating at 25±2°C.

3-2. Interface Connections

Interface chip in host side, must be used TMDS™, part No. SiI160, designed by Silicon Image Inc., or its equivalent.

This LCD employs three kinds of interface connections. A 21 pin connector is used for TMDS signals from the host computer. This mating connector is FI-WE21P-HF-E by JAE. A 15-pin connector is used for LCD module power and LCM controls signal from external monitor control circuits. And four connectors, a three pin connector, are used for the integral backlight system.

The pin configuration for the 21 pin connector is shown in the table below.

Table 3 21Pin CONNECTOR PIN CONFIGURATION

Pin	Symbol	Description	Pin	Symbol	Description
1	TX1+	TMDS positive differential output (channel1)	11	TX2+	TMDS positive differential output (channel2)
2	TX1-	TMDS negative differential output (channel1)	12	TX2-	TMDS negative differential output (channel2)
3	SHLD1	Shield for TMDS channel 1	13	SHLD2	Shield for TMDS channel 2
4	SHLDC	Shield for TMDS clock	14	SHLD0	Shield for TMDS channel 0
5	TXC+	TMDS positive differential output (reference clock)	15	TX0+	TMDS positive differential output (channel 0)
6	TXC-	TMDS negative differential output (reference clock)	16	TX0-	TMDS negative differential output (channel 0)
7	GND	Logic Ground	17	NC	Logic Ground
8	+5V	Logic +5V Supply (See note 2)	18	HPD	Hot Plug Detection (See note 3)
9	NC	No Connection	19	DDC_DAT	DDC2B Data (See note 4)
10	NC	No Connection	20	DDC_CLK	DDC2B Clock (See note 5)
			21	NC	No connection

Notes:
1. All shield pins and GND(ground) pin should be connected together and should also be connected to the LCD's metal frame.
2. This +5V is only for external monitor control circuits and directly connected to 15 pin connector. The specifications for this source are the same as those defined in the VESA DDC Standard V3.0(+5V±5%, 50mA minimum, 1.0A maximum).
3. This pin is internally connected to pin 8 (+5V) in LCM circuits.
4, 5. These pins are only for external monitor control circuits and directly connected to 15 pin connector.
6. Refer to appendix 1 regarding TMDS signal mapping.

A 15 pin connector for external monitor control circuits, is a model 53261 manufactured by Molex. The mating connector part number is 51021 or its equivalent. The pin configuration for this connector is shown in the table below.

Table 4 15 PIN CONNECTOR PIN CONFIGURATION

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	PWR_CTRL	LCM power control input signal Low : LCM power down except Sil161 receiver High : Normal operation mode	2
3	GND	Ground	
4	V_{DD}	LCM power supply, +18V±5%	
5	V_{DD}		
6	GND	LCM power supply, +18V±5%	
7	H_{SYNC}	Ground	
8	V_{SYNC}	H_{SYNC} out from TMDS receiver	
9	GND	V_{SYNC} out from TMDS receiver	
10	NC	Ground	
11	NC	No connection (Reserved)	
12	+5V_DDC	No connection (Reserved)	3
13	SDA	+5V out for DDC	
14	SCL	DDC data line out	
15	GND	DDC clock line out Ground	

Notes: 1. All GND(ground) pins should be connected together and should also be connected to the LCD's metal frame.
2. LCM power control input signal for power saving mode. If this pin is held low state, LCM goes to power saving mode except Sil161 receiver.
3. Pin 12, 13, 14 are for DDC2B communication between host computer and external monitor control circuits. These pins are directly connected to 21 pin connector.

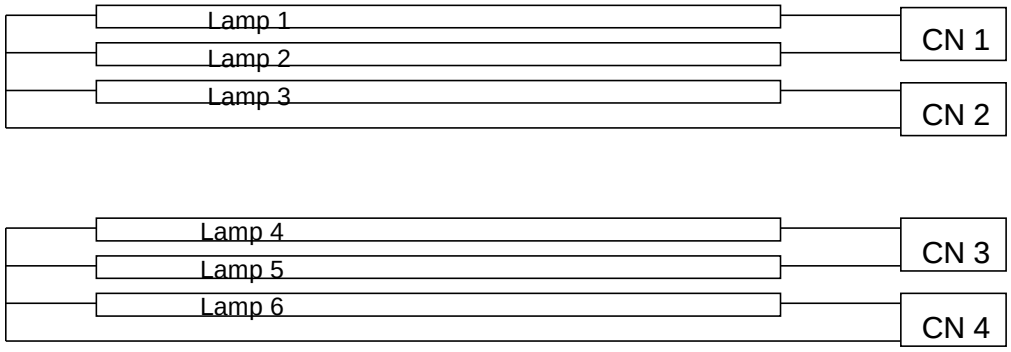
The backlight interface connector is a model BHR-03VS-1(CN1,3) and BHSR-02VS-1(CN2,4) manufactured by JST. The mating connector part number is SM02(8.0)B-BHS-1-TB and SM02B-BHSS-1-TB or equivalent. The pin configuration for the connector is shown in the table below.

Table 5 BACKLIGHT CONNECTOR PIN CONFIGURATION

No	Pin	Symbol	Description	Notes
CN 1	1	HV	High Voltage Power for lamp 1	1
	2	NC	No connection	
	3	HV	High Voltage Power for lamp 2	1
CN 2	1	HV	High Voltage Power for lamp 3	1
	2	GND	Ground for lamp 1, 2, 3	2
CN 3	1	HV	High Voltage Power for lamp 4	1
	2	NC	No connection	
	3	HV	High Voltage Power for lamp 5	1
CN 4	1	HV	High Voltage Power for lamp 6	1
	2	GND	Ground for lamp 4, 5, 6	2

Notes: 1. The input power terminal is colored pink. Ground pin color is white.
2. The backlight ground should be common with LCD metal frame.

<BACKLIGHT CONNECTOR DIAGRAM>



3-3.Signal Timing Specifications

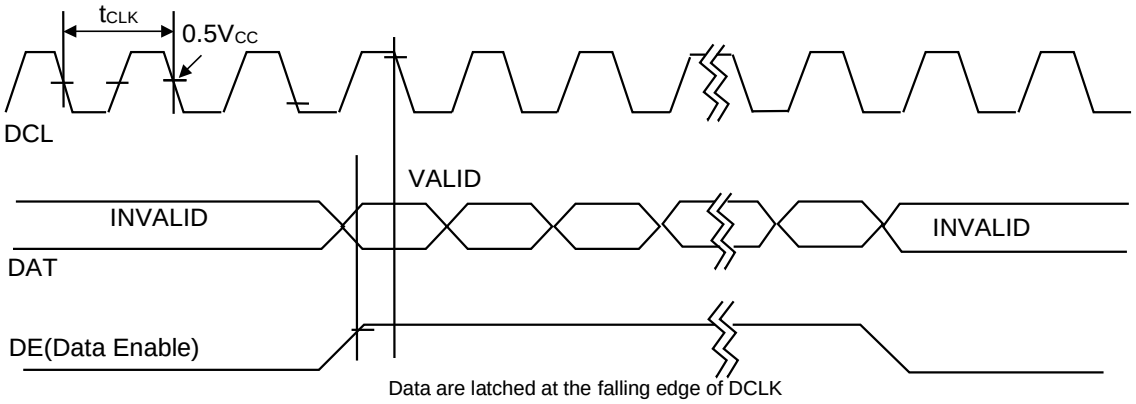
This is signal timing required at the input of the TMDS transmitter. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

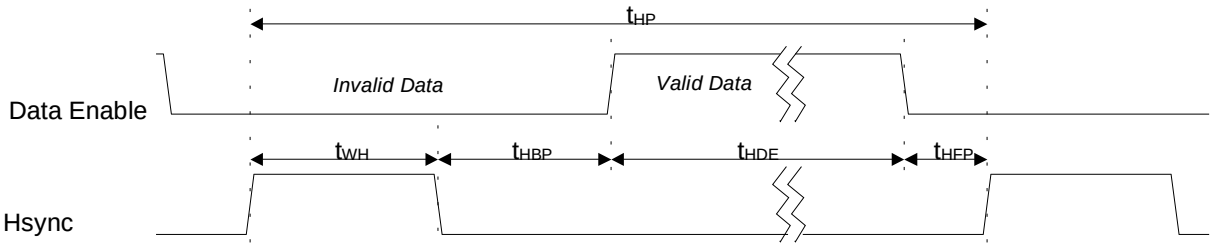
Table 6 Timing Table

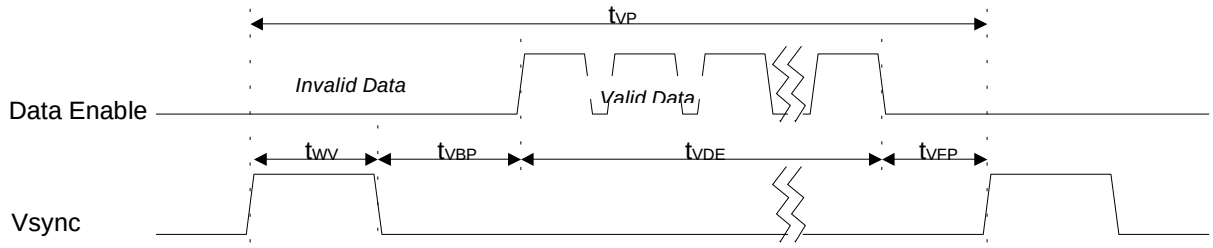
Parameter		Symbol	Value			Units	Notes
			Min.	Typ.	Max.		
Main Clock	Frequency	f_{CLK} t_{CLK}	- -	162.0 6.2	- -	MHz ns	1
Hsync	Period Pulse Width	t_{HP} t_{WH}	- tbd tbd	13.3 2160 192	- tbd -	µs clock clock	2
Vsync	Period Pulse Width	t_{VP} t_{WV}	- tbd tbd	16.7 1250 3	- tbd -	msec lines lines	3
Data Enable	Horizontal Back Porch Horizontal Active Data Horizontal Front porch	t_{HBP} t_{HDE} t_{HFP}	tbd 1600 tbd	304 1600 64	- 1600 -	clock clock clock	4
	Vertical Back Porch Vertical Active Data Vertical Front porch	t_{VBP} t_{VDE} t_{VFP}	tbd 1200 1	46 1200 1	- 1200 -	lines lines lines	

Notes: 1. Please, refer SiI160 data sheets for the detailed timing condition (required setup, hold time and etc.) between video processor and SiI160 TMDS transmitter.
2. Horizontal sync shall be active high.
3. Vertical sync shall be active high.
4. Data enable shall be active high

3-4. Signal Timimg Waveforms







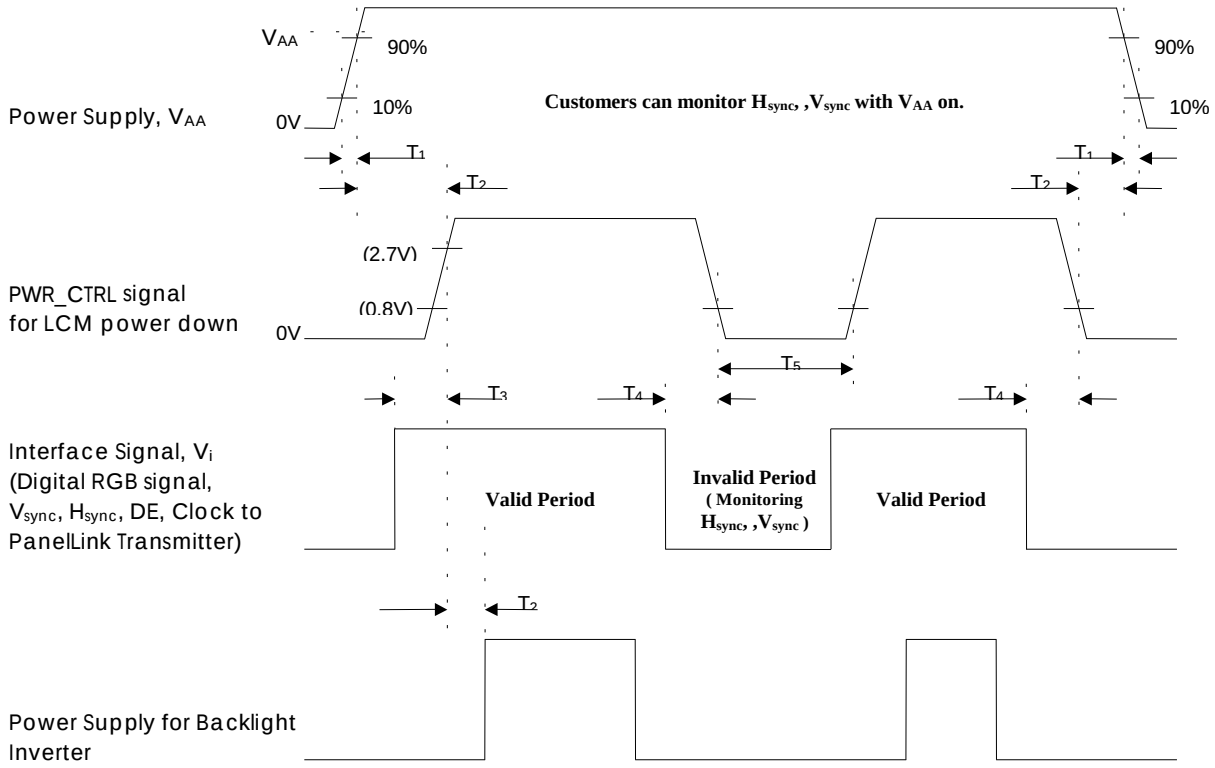
3-5. Color Input Data References

The brightness of each primary color(red, green and blue) is based on the 8-bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 7 Color Data Reference

Color		Input Color Data																							
		Red								Green								Blue							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(0) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255) Bright	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(0) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)Bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue(0) Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255) Bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3-6. Power Sequences



- **T_1** : 10 ns ~ 20 ms (Rise time, Fall time of power supplies)
- **T_2** : 100 ms (min.)
- **T_3** : 100 ms (max.)
- **T_4** : 100 ms (max.)
- **T_5** : 500 ms (min.)

Notes: 1. Please avoid floating state of interface signal at invalid period.

2. When the interface signal is invalid or no signal, be sure to pull down the power supply, **V_{AA}** to 0V or to pull down the **PWR_CTRL** signal under 0.8V. Invalid signal with V_{DD} and on state of PWR_CTRL signal for a long period of time, causes permanent damage to LCD panel.
3. BackLight inverter power must be turn on after power supply for LCD and interface signal are valid.
4. Power supply, **V_{AA}** shall be start under 0.8V.

4.Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0° and aperture 1 degree. The test equipment is PhotoResearch Prichard SpectroRadiometer Model 1980B-SC or equivalent. The input signal voltage and timing specifications are V_{DD} of 15.0Vdc, and typical values respectively. The input current of lamp is 7mA(F_{BL} = 50KHz) at the ground terminals.

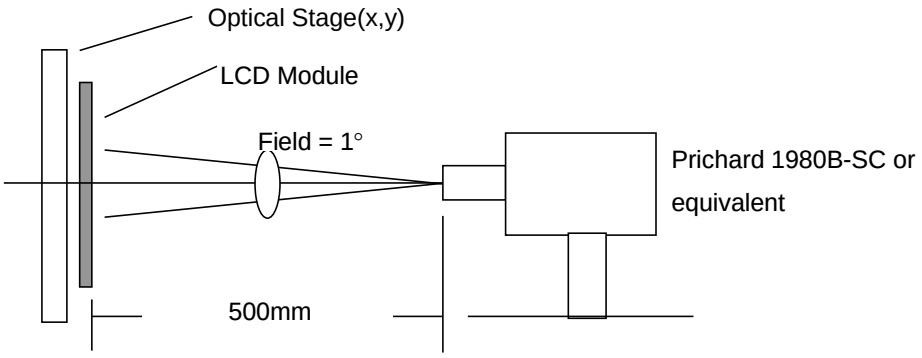
FIG. 1 presents additional information concerning the measurement equipment and method

Table 8 Optical Characteristics

(Ta:25℃, V_{DD}:18V, fv:60Hz, f_{DLK}:162MHz, I_{BL}:8mA, After 30minutes aging)

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
Contrast Ratio	CR	250	350	-		1
Luminance, white	SB_{WH}	200	250	-	cd/m^2	2
Luminance Variation	SB_V	-	-	1.30		3
Response Time	Tr	-	30	50	msec	4
Rise Time	Tr_R	-	15	25		
Decay Time	Tr_D	-	15	25		
CIE Color Coordinates						
Red	x_R	0.610	0.640	0.670		
	y_R	0.310	0.340	0.370		
Green	x_G	0.270	0.300	0.330		
	y_G	0.570	0.600	0.630		
Blue	x_B	0.120	0.150	0.180		
	y_B	0.070	0.100	0.130		
White	x_W	0.283	0.313	0.343		
	y_W	0.299	0.329	0.359		
Viewing Angle by CR ≥ 10					degree, °	5
x axis, right (Φ =0º)	θ	80	-	-		
x axis, left(Φ =180º)	θ	80	-	-		
y axis, up(Φ =90º)	θ	80	-	-		
y axis, down (Φ =270º)	θ	80	-	-		
Half Luminance Angle					degree, °	6
x axis, right (Φ =0º)	θ	45	50	-		
x axis, left(Φ =180º)	θ	45	50	-		
y axis, up(Φ =90º)	θ	35	40	-		
y axis, down (Φ =270º)	θ	35	40	-		
Cross talk		-	-	4	%	7
Flicker		-	-	-30	dB	8
Relative luminance		-	-	-		9

FIG. 1 Optical Characteristic Measurement Equipment and Method



Notes 1. Contrast Ratio (CR) is defined mathematically as:

$$\frac{\text{(Surface Luminance with all white pixels)}}{\text{(Surface Luminance with all black pixels)}}$$

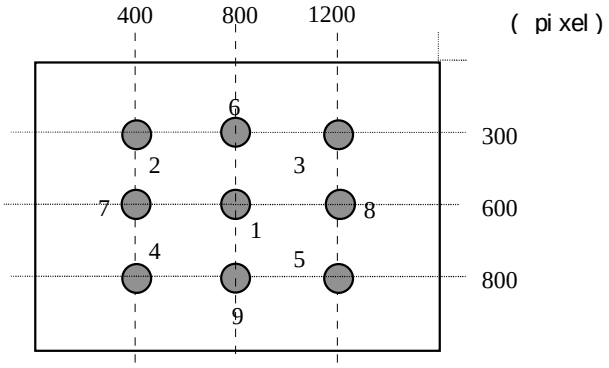
Contrast ratio shall be measured at the center of the display (Location 1).

2. Luminance is measured at the center point (location 1)

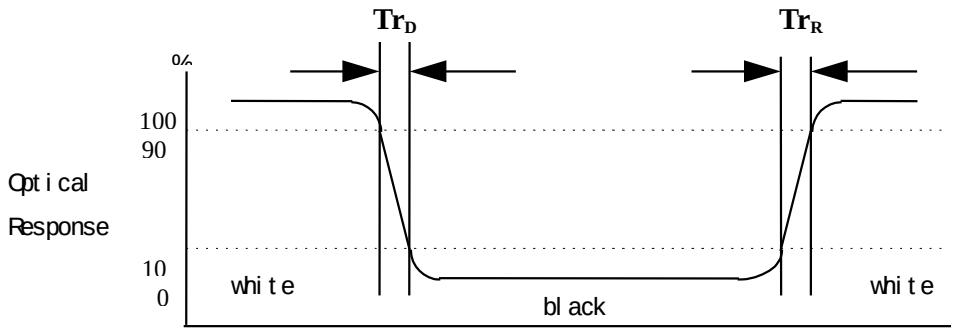
3. The variation in surface luminance, SB_V is defined as :

$$\frac{\text{Maximum } (B_1, B_2, \ldots B_9)}{\text{Minimum } (B_1, B_2, \ldots B_9)}$$

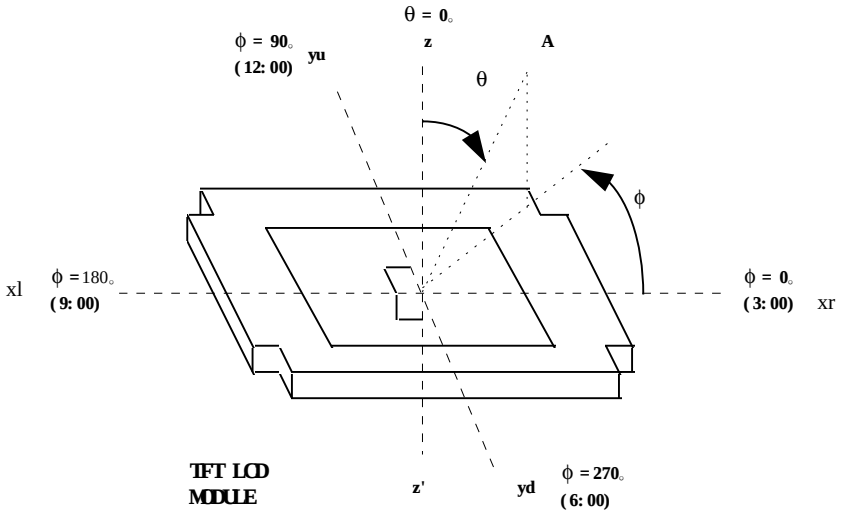
Where B1 to B9 are the luminance with all pixels displaying white at 9 locations.



4. The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.



5. Viewing angle is the angle at which the contrast ratio is greater than 10.



6. Half Luminance Angles

Half Luminance angles are defined as the up, down, left, and right angular boundaries at which the luminance value is 50% of the luminance value measured on-axis.

Measurements shall be done at the center of the display area (Location 1) with an all white image.

7. Cross talk shall be measured at center location.

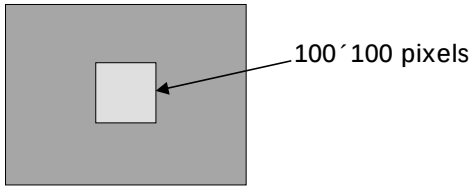
$$\text{Crosstalk Ratio} = \frac{\text{Luminance at pattern A - Luminance at pattern B}}{\text{Luminance at pattern A}}$$

Pattern A

(Mid-gray : Gs(S)=127)

Pattern B

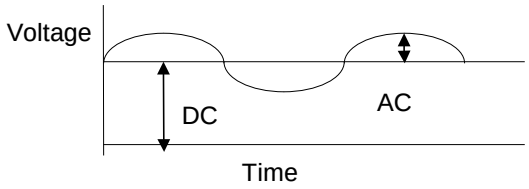
(Background:Gs(S)=0, Rectangular:Gs(S)=127)



8. Flicker shall be measured at the center location.

Test pattern : Pixel pattern
Background RGB gray (0, 0, 0)
Foreground RGB gray (127,127,127)

$$\text{Test equation : } 20 \log \frac{\text{AC(at 30Hz)}}{\text{DC level}}$$



9. Relative Luminance

(tbd)

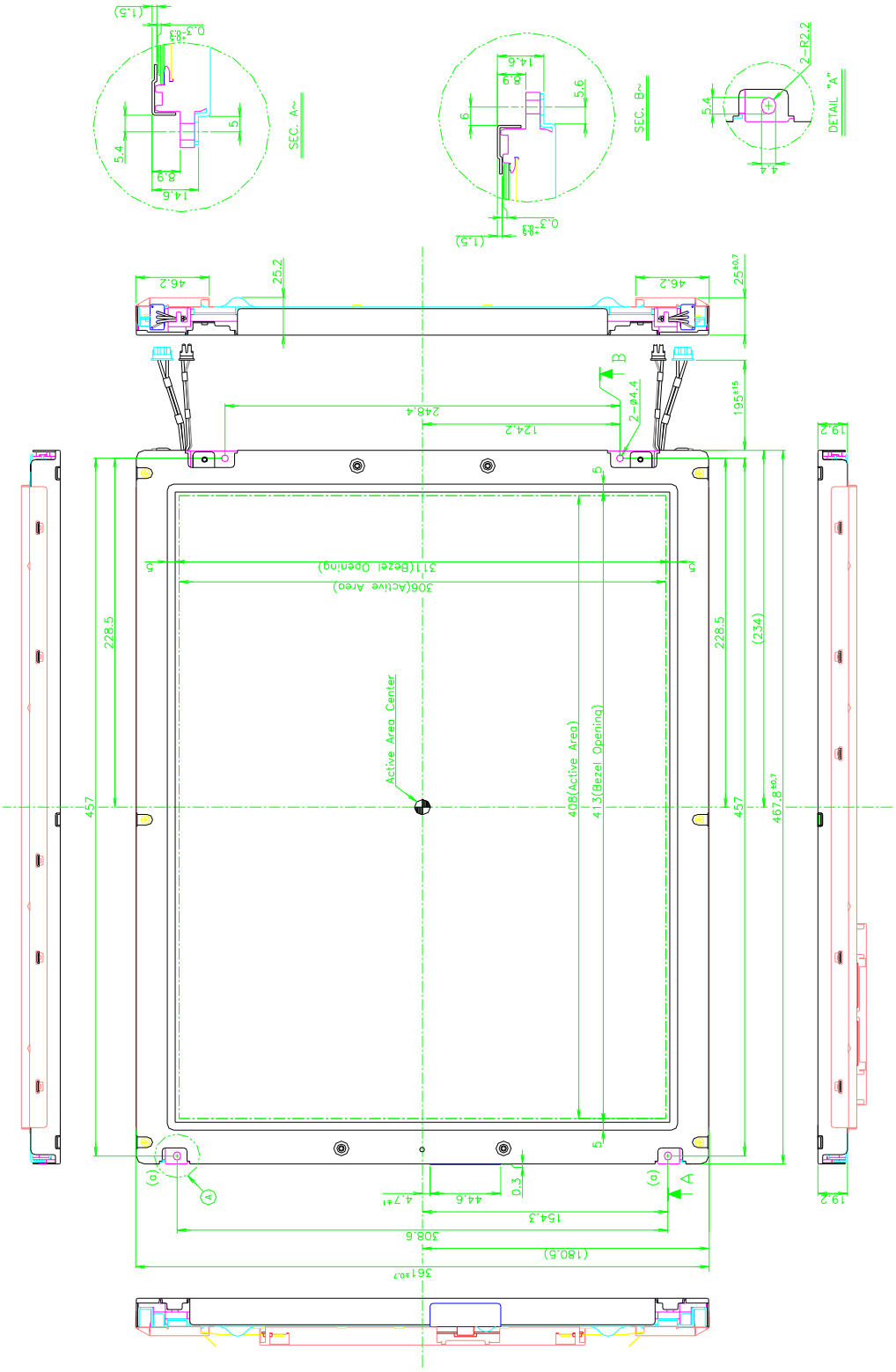
5.Mechanical Characteristics

The chart below provides general mechanical characteristics for the model LM201U1 LCD. Please refer to appendix 2 regarding the detailed mechanical drawing of the LCD module.

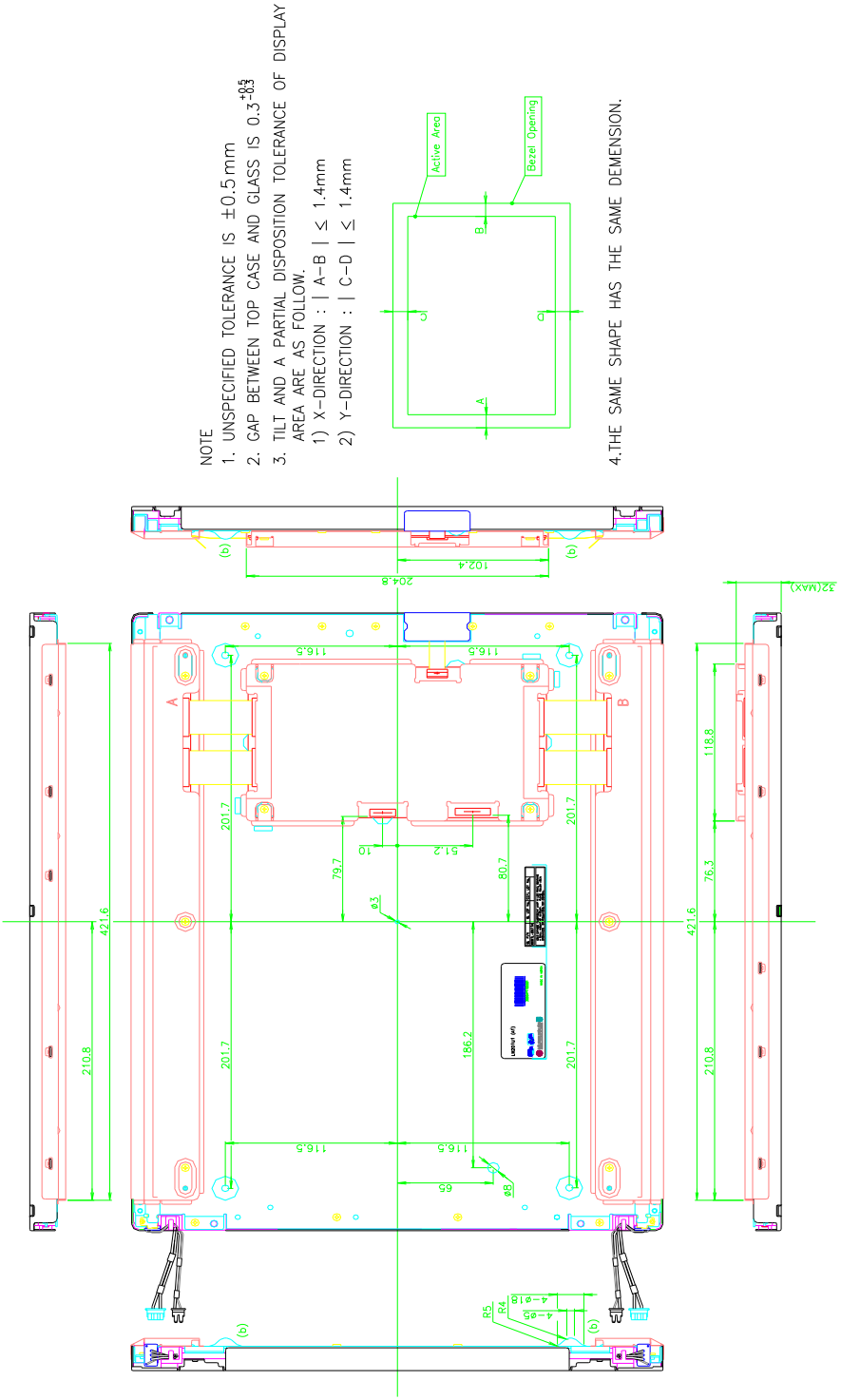
Table 9 Mechanical Specifications

Parameter	Value	Symbol	Notes
Outside dimension Width Height Thickness	 467.8 (typ) 361.0 (typ) 32.0 (max)	mm	Appendix 2.
Bezel area Width Height	 tbd tbd	mm	
Active area Width Height	 408.0 306.0	mm	
Weight	4100(typ) 4300(max)	gram	
Front surface of LCD	Hard coating 3H. Anti-glare treatment of the front polarizer	-	

5-1. Front View



5-2. Rear View


NOTE
1. UNSPECIFIED TOLERANCE IS ±0.5mm
2. GAP BETWEEN TOP CASE AND GLASS IS 0.3 +0.5 -0.3
3. TILT AND A PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA ARE AS FOLLOW.
1) X-DIRECTION : | A-B | ≤ 1.4mm
2) Y-DIRECTION : | C-D | ≤ 1.4mm
4.THE SAME SHAPE HAS THE SAME DEMENSION.
Active Area
Bezel Opening
204.8
102.4
32(MAX)
421.6
210.8
201.7
118.8
76.3
79.7
80.7
186.2
116.5
65
ø3
ø8
R5
R4
4-ø10
4-ø5

6. Reliability

No	Test ITEM	Conditions
1	High temperature operating test	50℃, 240 hour
2	High temperature storage test	60℃, 240 hour
3	Low temperature operating test	5℃, 240 hours
4	Thermal Shock Test (non-operating)	-20℃/30minutes, 60℃/30minutes, 50cycle
5	Altitude (non-operating)	Storage : 40,000ft
6	Vibration test (non-operating)	Waveform : Random Vibration level : 1.0 G RMS Bandwidth : 5 ~500Hz Duration : X, Y, Z, 10 min one time each direction
7	Shock test (non-operating)	Shock level : 100G Waveform: half sine wave, 2ms Direction : ±X, ±Y, ±Z one time each direction

<Result Evaluation Criteria>

There should be no changes, which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 1950 Third Edition, Underwriters Laboratories, Inc. Jan. 28, 1995.
Standard for Safety of Information Technology Equipment Including Electrical Business Equipment.

b) CAN/CSA C22.2 No. 950-95 Third Edition, Canadian Standards Association, Jan. 28, 1995.
Standard for Safety of Information Technology Equipment Including Electrical Business Equipment.

c) EN 60950 : 1992 + A1 : 1993 + A2 : 1993 + A3 : 1995 + A4 : 1997 + A11 : 1997
IEC 950 : 1991 + A1 : 1992 + A2 : 1993 + A3 : 1995 + A4 : 1996
European Committee for Electrotechnical Standardization (CENELEC)
EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9kHz to 40GHz.” American National Standards Institute(ANSI),1992.

b) C.I.S.P.R “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment.” International Special Committee on Radio Interference

c) EN 55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment.” European Committee for Electrotechnical Standardization (CENELEC),1988

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A, B ,C : SIZE
D : YEAR
E : MONTH
F,G : PANEL CODE
H : ASSEMBLY CODE
I,J,K,L,M : SERIAL NO.

Note : 1. YEAR

YEAR	97	98	99	2000	2001	2002	2003	2004	2005	2006	2007
Mark	7	8	9	0	1	2	3	4	5	6	7

2. MONTH

MONTH	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct.	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. Is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without notice.

8-2. Packing Form

a) Package quantity in one box : tbd pcs

b) Box Size : tbd mm ×tbd mm ×tbd mm

packing assembly drawing. (tbd)

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9.1 Mounting Precautions

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied To the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach a transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polalizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And Please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaked with petrolium benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluen and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9.2 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V = ± 200mV (Over and under shoot voltage).
(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) A module has high frequency circuit. If you need to shield the electromagnetic noise, please do in yours. When a Back-light unit is operating, it sounds. If you need to shield the noise, please do in yours.

9.3 Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc . And don't touch interface pin directly.

9.4 Precautions for strong light exposure

Strong light exposure causes degradation of polarizer and color filter.

9.5 Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9.6 Handling Precautions for protection film

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion- blown equipment or in such a condition, etc..

(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.

(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.

(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX 1 : Required Signal Assignment for SiI160 TMDS Receiver

Signal Name of SiI160	Pin Number of SiI160	Required Signals	
		1 pixel / clock	2 pixel / clock
DIE7 ~ DIE0	9, 10, 11, 12, 13, 14, 15, 16	Blue[7:0]	Even Blue[7:0]
DIE15 ~ DIE8	99, 100, 1, 2, 3, 4, 5, 6	Green[7:0]	Even Green[7:0]
DIE23 ~ DIE16	90, 91, 92, 93, 94, 95, 96, 97	Red[7:0]	Even Red[7:0]
DIO7 ~ DIO0	68, 69, 70, 71, 72, 73, 74, 75	N/A	Odd Blue[7:0]
DIO15 ~ DIO8	58, 59, 60, 61, 62, 63, 64, 65	N/A	Odd Green[7:0]
DIO23 ~ DIO16	48, 49, 50, 51, 52, 53, 54, 55	N/A	Odd Red[7:0]
H_{sync}	76	Horizontal Sync	Horizontal Sync
V_{sync}	77	Vertical Sync	Vertical Sync
DE	78	Data Enable	Data Enable
IDCK	80	Input Clock(162MHz)	Input Clock(81MHz)
PIXS	25	Low level	High level

Notes : 1. Input data shall be followed by $D_0(R_0G_0B_0)$, $D_1(R_1G_1B_1)$, $D_2(R_2G_2B_2)$, $D_3(R_3G_3B_3)$, $D_4(R_4G_4B_4)$.
2. Refer to SiI160 Data Sheet or application notes for detail descriptions.