SPECIFICATION
FOR
APPROVAL

(V) **Preliminary Specification**
( ) **Final Specification**

Title	10.4” VGA TFT LCD

BUYER	
MODEL	

SUPPLIER	LG.Philips LCD Co., Ltd.
*MODEL	LB104V03
Suffix	A1

*When you obtain standard approval,
please use the above model name without suffix

SIGNATURE	DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

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RECORD OF REVISIONS

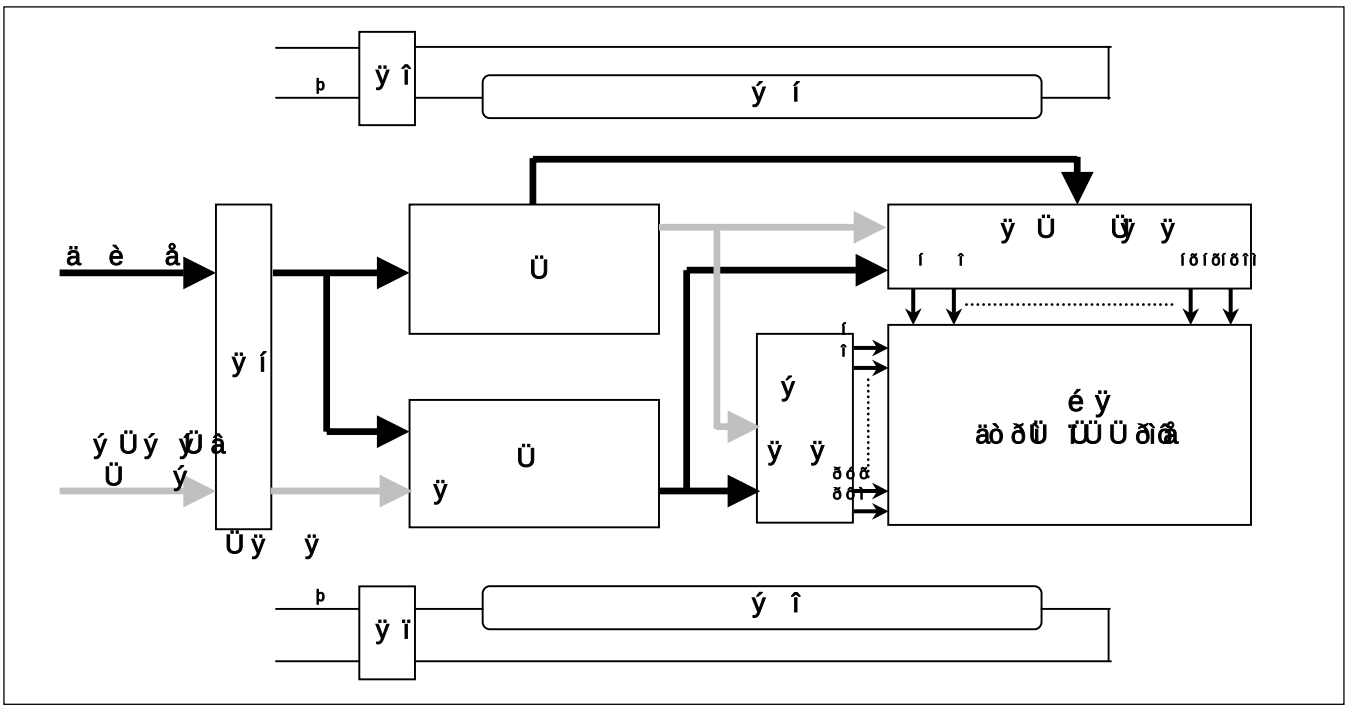
Revision No	Revision Date	Page	Description	Note
0.0	Mar. 14. 2003	-	First Draft (Preliminary)	

1. General Description

The LB104V03-A1 is a Color Active Matrix Liquid Crystal Display with an integral Cold Cathode Fluorescent Lamp (CCFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 10.4 inches diagonally measured active display area with VGA resolution(480 vertical by 640 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors.

The LB104V03-A1 has been designed to apply the interface method that enables low power, high speed, low EMI.

The LB104V03-A1 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LB104V03-A1 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	10.4 inches(26.42cm) diagonal
Outline Dimension	236(H) Ý 180(V) Ý 10(D) mm
Pixel Pitch	0.33 mm Ý 0.33 mm
Pixel Format	640 horiz. By 480 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	400 cd/m^2(Typ.) Lamp Ass'y replaceable
Power Consumption	TBD Watt(Typ.)
Weight	500 g (Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Hard coating(3H) Anti-glare treatment of the front polarizer

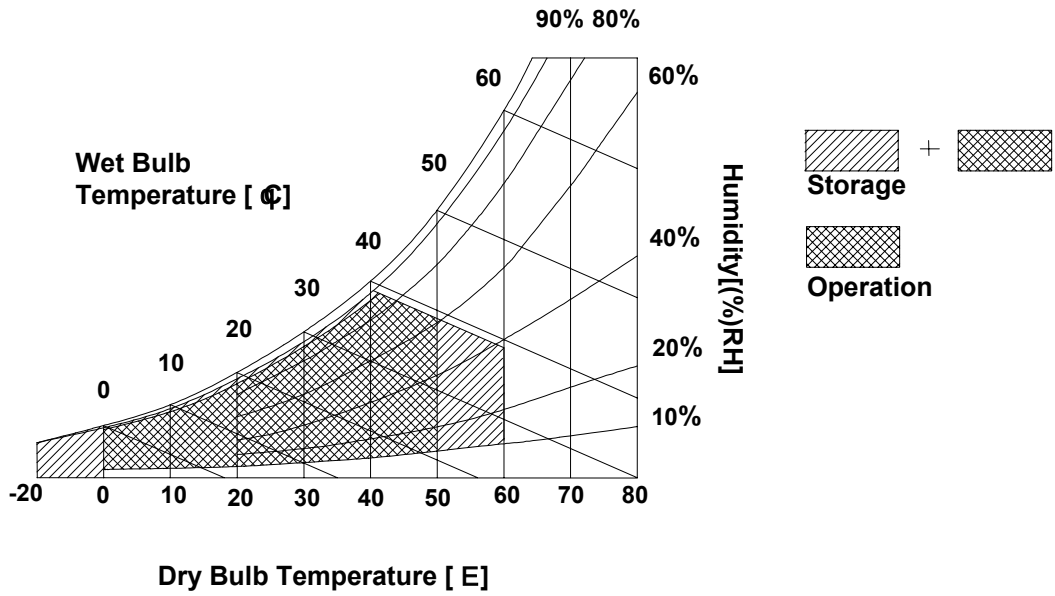
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 r 5 ¢
Operating Temperature	TOP	0	50	¢	1
Storage Temperature	TST	-20	60	¢	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ¢ Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

The LB104V03-A1 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the CCFL, is typically generated by an inverter. The inverter is an external unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
MODULE :						
Power Supply Input Voltage	VCC	3.0	3.3	3.6	Vdc	
Power Supply Input Current	I_{CC}	-	TBD	TBD	mA	1
Power Consumption	Pc	-	TBD	TBD	Watt	1
LAMP :						
Operating Voltage	V_{BL}		485	625	V_{RMS}	2
Operating Current	I_{BL}	2.0	6.0	7.0	mA_{RMS}	3
Established Starting Voltage	Vs					4
at 25 ℃		-	-	750	V_{RMS}	
at 0 ℃		-	-	940	V_{RMS}	
Operating Frequency	f_{BL}	40	55	80	kHz	5
Discharge Stabilization Time	Ts	-	-	3	Min	6
Power Consumption	P_{BL}	-	5.8	6.4	Watt	7
Life Time		40,000	-	-	Hrs	8

Note)

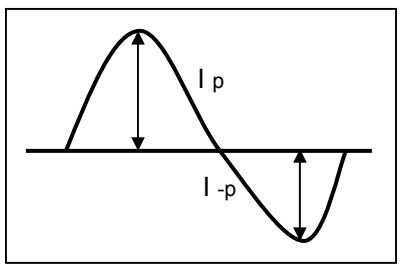
The design of the inverter must have specifications for the lamp in LCD Assembly. The performance of the Lamp in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter(no lighting, flicker, etc) never occurs. When you confirm it, the LCD Assembly should be operated in the same condition as installed in your instrument.

1. VCC=3.3V, 25 ℃, f_V (frame frequency) = 60Hz condition, whereas Mosaic pattern(Typ).,full black pattern(Max) is displayed.
2. The variance of the voltage is r 10%.
3. The typical operating current is for the typical surface luminance (L_{WH}) in optical characteristics.
4. The voltage above VS should be applied to the lamps for more than 1 second for start-up. Otherwise, the lamps may not be turned on. The used lamp current is the lamp typical current.

5. The output of the inverter must have symmetrical(negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave.
   Lamp frequency may produce interference with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.
6. Let's define the brightness of the lamp after being lighted for 5 minutes as 100%.
   T_S is the time required for the brightness of the center of the lamp to be not less than 95%.
7. The lamp power consumption shown above does not include loss of external inverter.
   The used lamp current is the lamp typical current. (2 Lamp)
8. The life time is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25 ± 2℃.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following. It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.
b. The distortion rate of the waveform should be within ± 10%.
* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

* Distortion rate

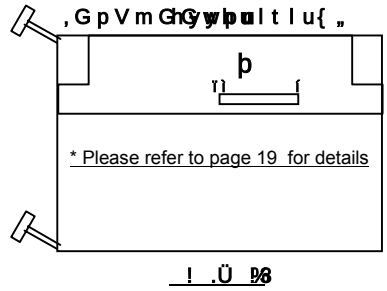
I_p (or I_{-p}) / I_{rms}

Do not attach a conducting tape to lamp connecting wire.
If the lamp wire attach to a conducting tape, TFT-LCD Module has a low luminance and the inverter has abnormal action. Because leakage current is occurred between lamp wire and conducting tape.

3-2. Interface Connections

This LCD employs Three interface connections, a 41 pin connector is used for the module electronics interface and the other connectors are used for the integral backlight system.
The electronics interface connector is a model KN10G-30S-1H manufactured by Hirose or equivalent.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	GND	Ground	
2	VCC	Power (3.3V)	
3	VCC	Power (3.3V)	
4	GND	Ground	
5	DCLK	Data Clock	
6	DTMG	Data Enable	
7	VSYNC	Vertical sync	
8	HSYNC	Horizontal sync	
9	GND	Ground	
10	R0	Red Data	Red data least significant bit (LSB)
11	R1	Red Data	
12	R2	Red Data	
13	R3	Red Data	
14	R4	Red Data	
15	R5	Red Data	Red data most significant bit (MSB)
16	GND	Ground	
17	G0	Green Data	Green data least significant bit (LSB)
18	G1	Green Data	
19	G2	Green Data	
20	G3	Green Data	
21	G4	Green Data	
22	G5	Green Data	Green data most significant bit (MSB)
23	GND	Ground	
24	B0	Blue Data	Blue data least significant bit (LSB)
25	B1	Blue Data	
26	B2	Blue Data	
27	B3	Blue Data	
28	B4	Blue Data	
29	B5	Blue Data	Blue data most significant bit (MSB)
30	GND	Ground	

The backlight interface connector is a model BHSR-02VS-1, manufactured by JST. The mating connector part number is SM02B-BHSS-1 or equivalent.

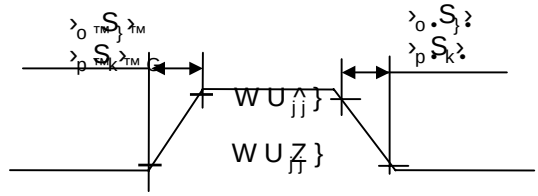
Pin	Symbol	Description	Notes
1	HV	High Voltage (Pink color)	-
2	LV	Low Voltage (white color)	-

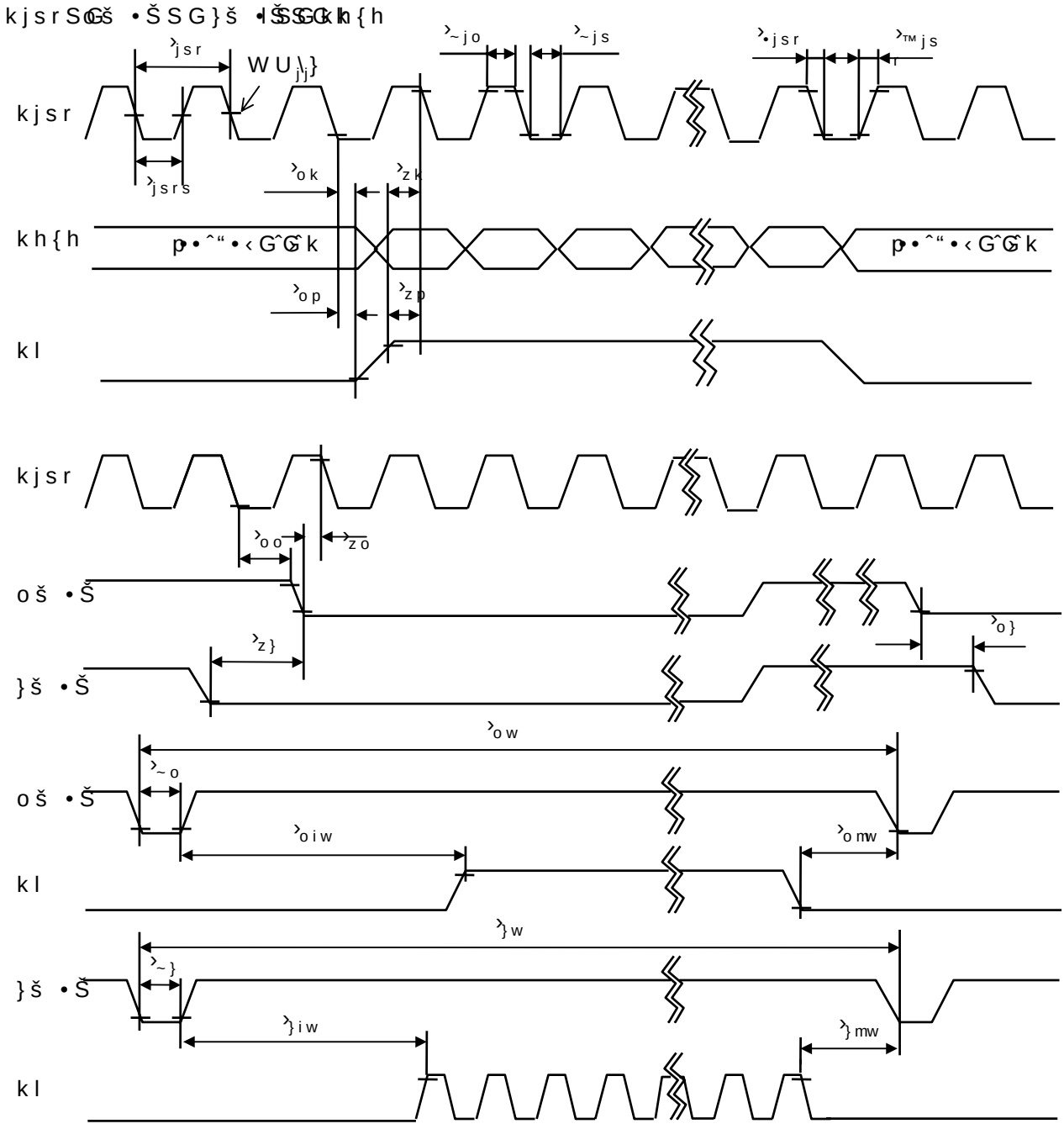
3-3. Signal Timing Specifications

Table 5. TIMING TABLE

ITEM		Symbol	MIN.	TYP.	MAX.	UNIT	NOTE
DCLK	Frequency	f_{CLK}	21	25.1	28	MHz	
	Width_Low	t_{WCL}	8	-	-	ns	
	Width_High	t_{WCH}	5	-	-		
	Rise Time	t_{rCLK}	-	-	25		
	Fall Time	t_{fCLK}	-	-	25		
Hsync	Setup Time	t_{SH}	3	-	-	ns	For Dclk
	Hold Time	t_{HH}	8	-	-		
	Period	t_{HP}	770	800	900	t_{CLK}	
	Width_Active	t_{WH}	12	-	120		
	Rise/Fall Time	t_{Hr}, t_{Hf}	-	-	30	ns	
Vsync	Setup Time	t_{SV}	0	-	-	ns	For Hsync
	Hold Time	t_{HV}	2	-	-		
	Period	t_{VP}	515	525	560	t_{Hp}	
	Width_Active	t_{WV}	2	-	24		
	Rise/Fall Time	t_{Vr}, t_{Vf}	-	-	50	ns	
DE	Setup Time	t_{SI}	6	-	-	ns	For Dclk
	Hold Time	t_{HI}	1	-	-		
	Rise/Fall Time	t_{Ir}, t_{If}	-	-	30	ns	
	Horizontal Back Porch	t_{HBP}	12	-	-	t_{CLK}	
	Horizontal Front Porch	t_{HFP}	12	-	-		
	Vertical Back Porch	t_{VBP}	5	-	-	t_{Hp}	
	Vertical Front Porch	t_{VFP}	1	-	-		
DATA	Setup Time	t_{SD}	6	-	-	ns	For Dclk
	Hold Time	t_{HD}	3	-	-		
	Rise/Fall Time	t_{Dr}, t_{Df}	-	-	25	ns	

3-4. Signal Timing Waveforms





3-5. Color Input Data Reference

The brightness of each primary color (r