Engineering Specification

Type 18.1 SXGA Color TFT/LCD Module
Model Name:ITSX98

Document Control Number : OEM I-98-02

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Product Development
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
May 23,2001	OEM98-01	All	First Edition for customer. Based on Internal Spec. as of May 11,2001.
October 19,2001	OEM I-98-02		Updated by establishment of the New Company as "International Display Technology". Based on Internal Spec. EC H30912 as of October 19,2001.
		5,8,18	To update White Luminance.
		5	To update Weight, Optical Rise Time + Fall Time and Power Consumption.
		7	To update value of Shock Test Criteria.
		8	To update Vewing Angle and Response Time.
		19	To update the Lamp Current versus Luminance Curve.
		21	To add Note for Timing Characteristics.
		24,25	To update Power Consumption.
		27,28	To update Reference Drawings.

1.0 Handling Precautions

- Damage to the panel or the panel electronics may result from any deviation from the recommended power on/off sequencing. The panel should not be hot plugged. Refer to the Power On/Off Sequence section in this Specification.
- Handle the panel with care. The LCD panel and CCFL (Cold Cathode Fluorescent Lamp)s are made of glass and may crack or break if dropped or subjected to excessive force.
- The CCFLs contain a small amount of Mercury so should not be disposed of to landfill. Dispose of as required by local ordinances or regulations.
- The LCD module contains small amounts of material having no flammability grade. The exemption conditions of the flammability requirements (4.7.3.4, IEC60950 3rd.Ed. or UL60950 3rd.Ed.) should be applied.
- The panel may be damaged by the application of twisting or bending forces to the module assembly.Care should be taken in the design of the monitor housing and the assembly procedure to prevent stress damage to the panel especially the lamp cable and the lamp connector..
- Use standard earthing/grounding procedures to prevent damage to the CMOS LSI while handling the module.
- Use earthing/grounding procedures, an ionic shower, or similar to prevent static damage while removing the protective front sheet.
- The front polarizer can be easily damaged. Take care not to scratch the front surface with any hard or abrasive material. Dust, finger marks, grease etc. can be removed with a soft damp cloth (a small amount of mild detergent can be used on the damp cloth). Do not apply water or datergent directly to the front surface as this may cause staining or damage the electronic components.
- Never use any solvent on the front polarizer or module as this may cause permanent damage.
- Do not open or modify the module assembly.
- Continuous operation of the panel with the same screen content may result in some image sticking. Over 10 hours operation with the same content is not recommended.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

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2.0 General Description

This specification applies to the Type 18.1 Color TFT/LCD Module 'ITSX98'.

This module is designed for a LCD monitor style display unit and excluding inverter.

The screen format and electrical interface are intended to support the VESA SXGA (1280(H) x 1024(V)at 60Hz) screen.

Support color is native 16M colors(RGB 8-bit data driver).

All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.

2.1 Characteristics

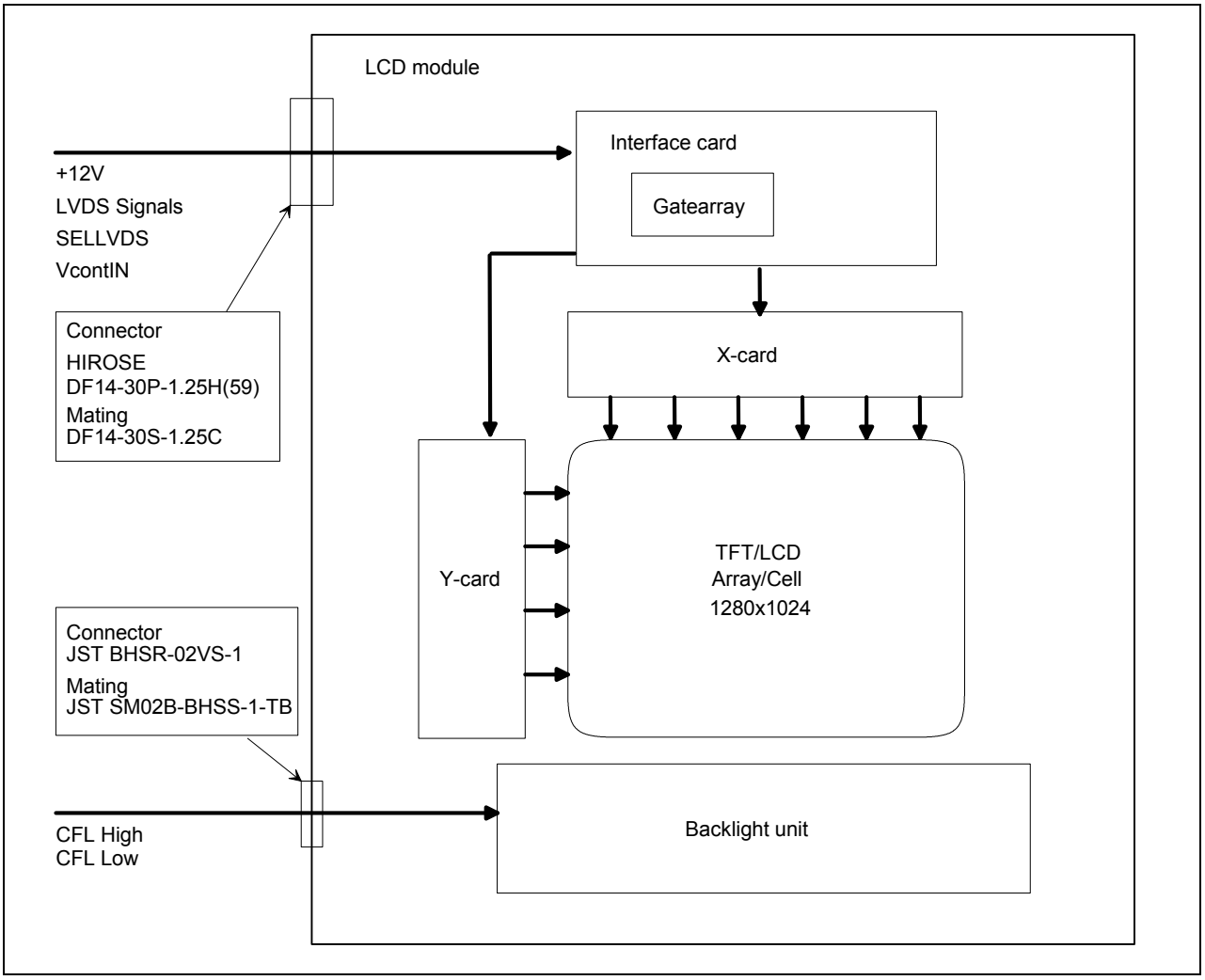
The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	460
Pixels H x V	1280(x3) x 1024
Active Area [mm]	359.0(H) x 287.2(V)
Pixel Pitch [mm]	0.2805(per one triad) x 0.2805
Pixel Arrangement	R,G,B Vertical Stripe
Weight [gram]	2,850 typ.
Physical Size [mm]	389.0(W) typ. x 317.2(H) typ. x 27.0(D) max.
Display Mode	Normally Black
Support Color	16M (RGB 8-bit data)
White Luminance [cd/m^2]	270 typ.
Contrast Ratio	400 : 1 typ.
Optical Rise Time/Fall Time [msec]	Rise Time + Fall Time : 40 typ. (total) **Note**
Input Voltage [V]	+12 +/- 5%
Power Consumption [W]	28.5 typ., 31.3 max. (Without inverter power loss)
Electrical Interface	LVDS Dual (Even/Odd R/G/B Data(8bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60

Note : Luminance : Rise / Fall Time:Respective 10% -> 90%, 90%->10%

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 18.1 Color TFT/LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows ;

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+13.2	V	
Select LVDS data order	SELLVDS	-0.3	+3.3	V	
CFL Current	ICFL	0.0	+9.0	mArms	
CFL Ignition Inverter Voltage	Vi_invCFL	0.0	1,700	Vrms	
CFL Peak Inrush Current	ICFLp	0.0	20	mArms	
Contrast control	VcontlN	-0.3	+3.3	V	
Operating Temperature	TOP	0	+50	deg.C	Note 1
Operating Humidity	HOP	8	80	%RH	Note 1
Storage Temperature	TST	-20	+60	deg.C	Note 1
Storage Humidity	HST	5	95	%RH	Note 1
Vibration			1.5 10-200	G Hz	Note 2
Shock			50 11	G ms	Note 2 Half sine wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.

Note 2 : Vibration Specification

- Sign Vibration:10-200-10Hz, 1.5G, 0.29 Oct/min, 30 min, X, Y, A Axis, Each One Time.

Shock Specification

- Half sine wave:50G 11msec. -X+/-, -Y+/-, -Z+/- (Total 6 directions), Each two times Shock.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≧15 (Left)	85 85	- -
	Vertical (Upper) K≧15 (Lower)	85 85	- -
	Horizontal (Right) K≧10 (Left)	- -	85 Min. 85 Min.
	Vertical (Upper) K≧10 (Lower)	- -	85 Min. 85 Min.
Contrast ratio		400	-
Response Time (ms)	Rising(10%->90%) + Falling(90%->10%)	40	-
Color Chromaticity (CIE)	Red x	0.640	+-0.030
	Red y	0.330	+-0.030
	Green x	0.290	+-0.030
	Green y	0.600	+-0.030
	Blue x	0.150	+-0.030
	Blue y	0.060	+-0.030
	White x	0.313	+-0.030
	White y	0.329	+-0.030
Maximum White Luminance (cd/m^2)	CFL 6.0 mA **Note**	270	-

Note:Measure center of the screen.

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Signal Connector
Manufacturer	HIROSE
Type / Part Number	DF14-30P-1.25H(59)
Mating Type / Part Number	DF14-30S-1.25C
Contact / Part Number	DF14-2628SCFA

Connector Name / Designation	For Backlight Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Interface Signal Connector

Pin #	Signal Name	Pin #	Signal Name
30	Vin(+12V)	29	Vin(+12V)
28	Vin(+12V)	27	VinRTN(GND)
26	VinRTN(GND)	25	VinRTN(GND)
24	SELLVDS	23	VcontIN
22	DGND	21	RxOIN3+
20	RxOIN3-	19	RxOCLKIN+
18	RxOCLKIN-	17	RxOIN2+
16	RxOIN2-	15	RxOIN1+
14	RxOIN1-	13	RxOIN0+
12	RxOIN0-	11	RxEIN3+
10	RxEIN3-	9	RxECLKIN+
8	RxECLKIN-	7	RxEIN2+
6	RxEIN2-	5	RxEIN1+
4	RxEIN1-	3	RxEIN0+
2	RxEIN0-	1	LVDSGND

Lamp Connector Pin Assignment

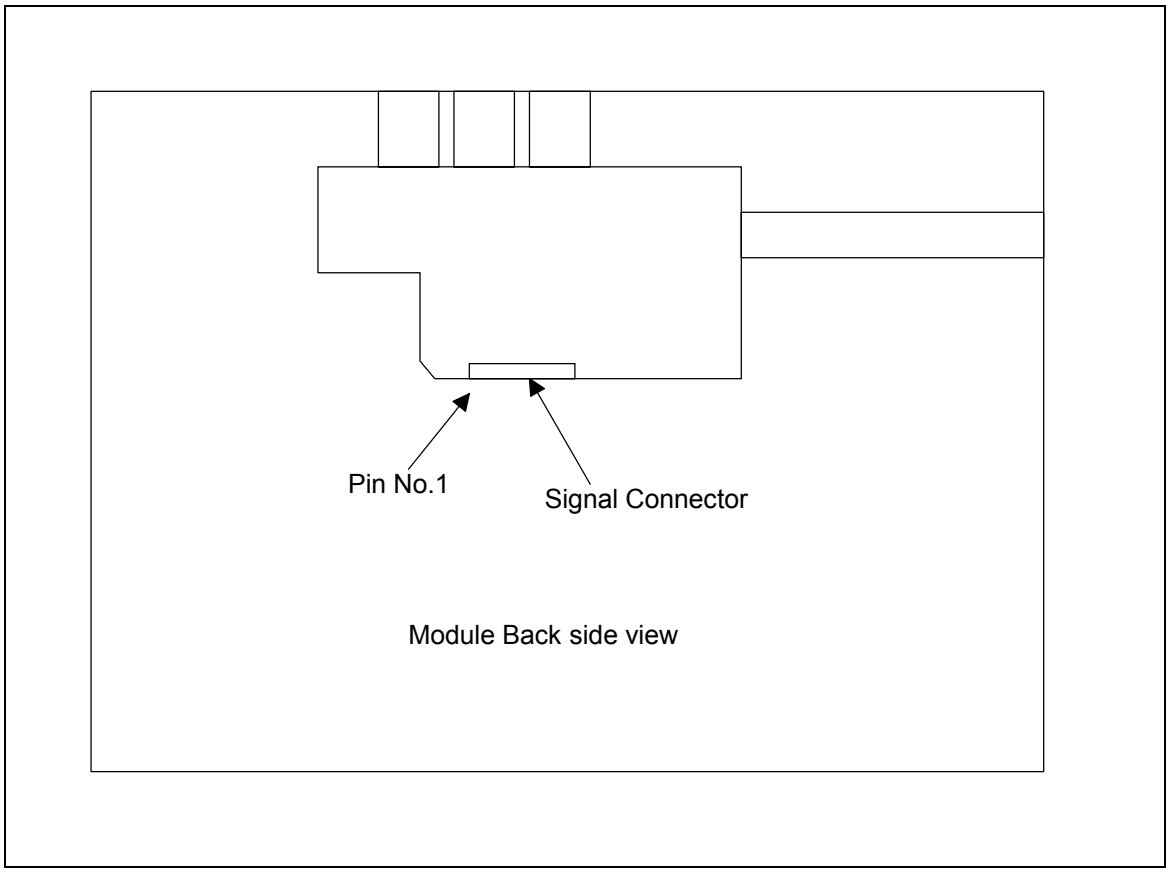
Pin #	Signal Name	Pin #	Signal Name
1	CFL-High	2	CFL-Low

5.3 Interface Signal Description

The module uses a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible.
The first LVDS port (RxExxx) transmits even pixels while the second LVDS port (RxOxxx) transmits odd pixels.

Pin numberings have been changed from previous models of ITSX94, ITSX94N, ITSX94N1, and ITSX96R, due to signal connector type change. Physical order of singals are not changed.
Please refer to the chart below for pin #1.

LCD Drive Connector No.1 Pin location

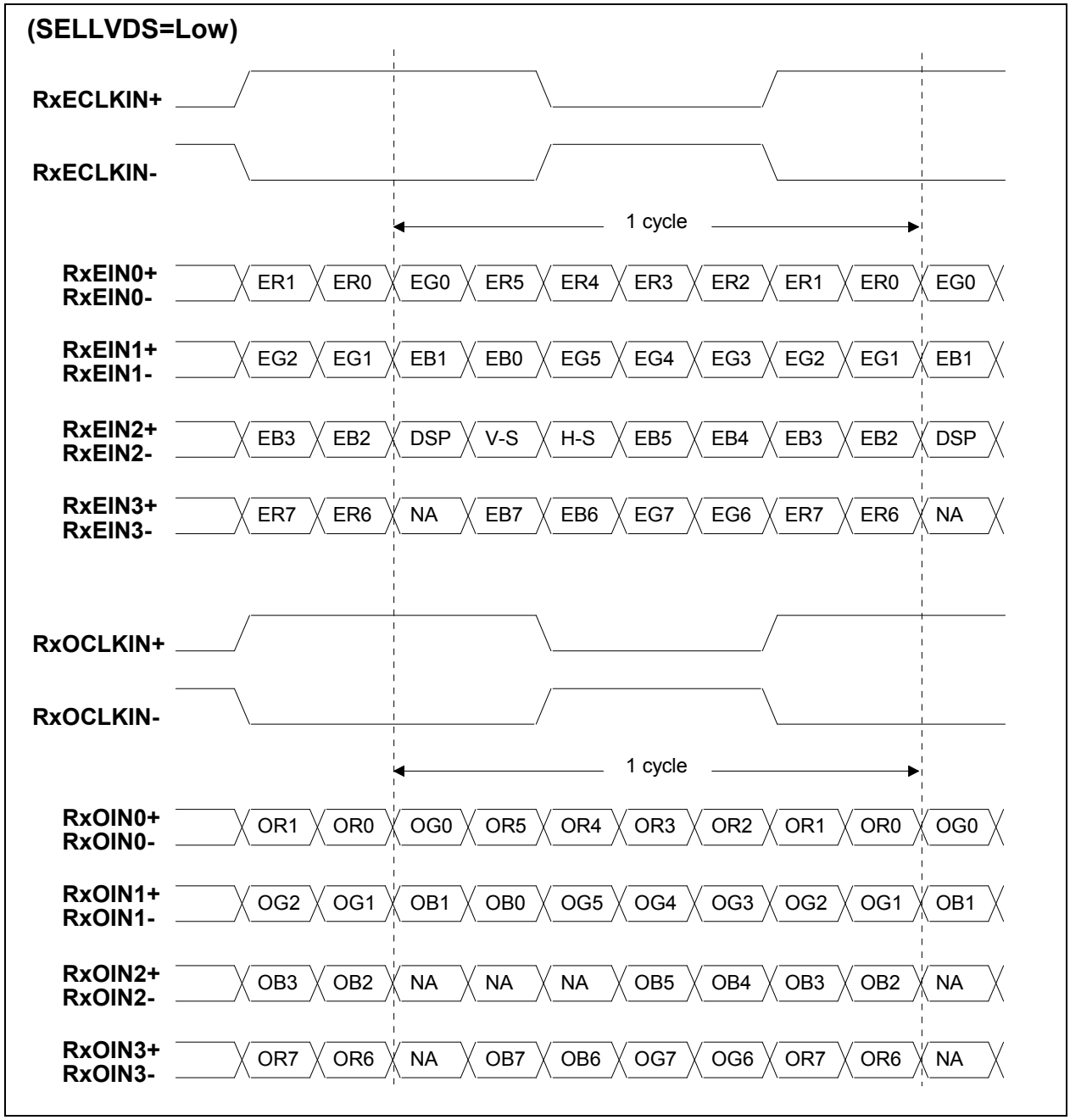


LCD Drive Connector Signal Description

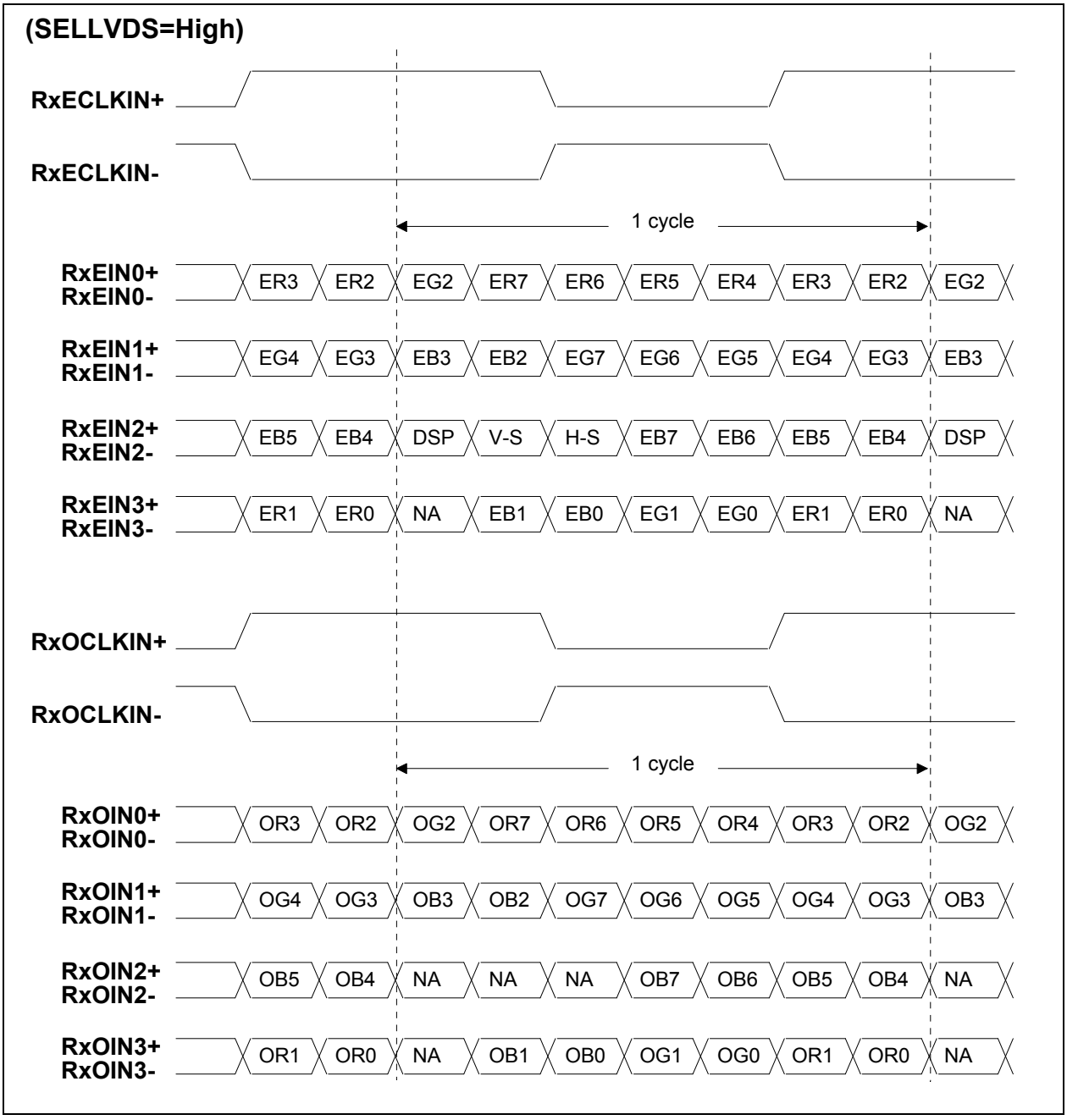
PIN #	SIGNAL NAME	Description
30	Vin	+12.0V Power Supply
29	Vin	+12.0V Power Supply
28	Vin	+12.0V Power Supply
27	VinRTN	Ground for Vin line
26	VinRTN	Ground for Vin line
25	VinRTN	Ground for Vin line
24	SELLVDS	Select LVDS data order. See the following figure.
23	(RESERVED)	This pin should be left open.
22	DGND	Signal Ground
21	RxOIN3+	Positive LVDS differential data input (Odd data)
20	RxOIN3-	Negative LVDS differential data input (Odd data)
19	RxOCLKIN+	Positive LVDS differential clock input (Odd Clock)
18	RxOCLKIN-	Negative LVDS differential clock input (Odd Clock)
17	RxOIN2+	Positive LVDS differential data input (Odd data)
16	RxOIN2-	Negative LVDS differential data input (Odd data)
15	RxOIN1+	Positive LVDS differential data input (Odd data)
14	RxOIN1-	Negative LVDS differential data input (Odd data)
13	RxOIN0+	Positive LVDS differential data input (Odd data)
12	RxOIN0-	Negative LVDS differential data input (Odd data)
11	RxEIN3+	Positive LVDS differential data input (Even data)
10	RxEIN3-	Negative LVDS differential data input (Even data)
9	RxECLKIN+	Positive LVDS differential clock input (Even Clock)
8	RxECLKIN-	Negative LVDS differential clock input (Even Clock)
7	RxEIN2+	Positive LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG)
6	RxEIN2-	Negative LVDS differential data input (Even data,H-Sync,V-Sync,DSPTMG)
5	RxEIN1+	Positive LVDS differential data input (Even data)
4	RxEIN1-	Negative LVDS differential data input (Even data)
3	RxEIN0+	Positive LVDS differential data input (Even data)
2	RxEIN0-	Negative LVDS differential data input (Even data)
1	DGND	Signal Ground

Note: Input signals of odd and even clock shall be the same timing.

The interface card has a 100ohm resistor between positive and negative lines of each LVDS signal input on the internal circuit.



Note:R/G/B data 7:MSB, R/G/B data 0:LSB



Note:R/G/B data 7:MSB, R/G/B data 0:LSB

The following is LVDS Signal description.

LVDS DATA NAME	Description	
DSP	**Display Timing**	When the signal is high, the pixel data shall be valid to be displayed.
V-S	**Vertical Sync**	Both Positive and negative polarity are acceptable.
H-S	**Horizontal Sync**	Both Positive and negative polarity are acceptable.

TI LVDS X'mitter (SN75LVDS83) Signal name	ITSX98 LVDS Signal (SELLVDS=Low)	ITSX98 LVDS Signal (SELLVDS=High)
D0	Red0	Red2
D1	Red1	Red3
D2	Red2	Red4
D3	Red3	Red5
D4	Red4	Red6
D5	Red7	Red1
D6	Red5	Red7
D7	Green0	Green2
D8	Green1	Green3
D9	Green2	Green4
D10	Green6	Green0
D11	Green7	Green1
D12	Green3	Green5
D13	Green4	Green6
D14	Green5	Green7
D15	Blue0	Blue2
D16	Blue6	Blue0
D17	Blue7	Blue1
D18	Blue1	Blue3
D19	Blue2	Blue4
D20	Blue3	Blue5
D21	Blue4	Blue6
D22	Blue5	Blue7
D23	NA	NA
D24	H Sync	H Sync
D25	V Sync	V Sync
D26	Disp Timing	Disp Timing
D27	Red6	Red0

Note:
SELLVDS: Pin#7 of Signal connector
Red0: LSB, Red7: MSB

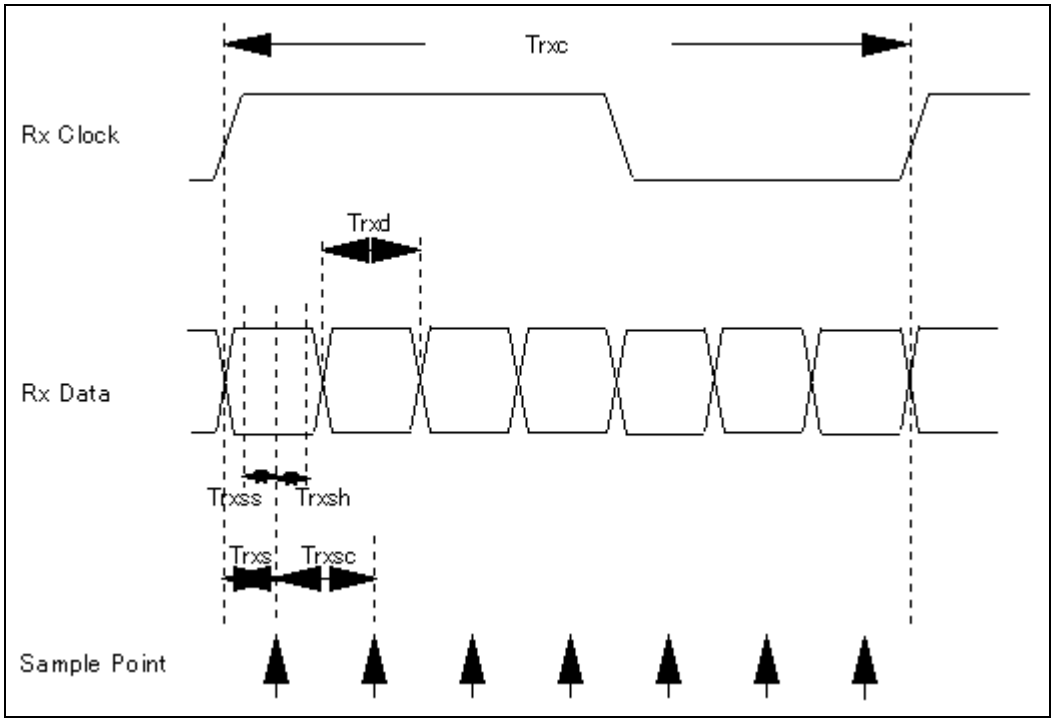
5.4 Interface Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when Vin is off.
It is recommended to refer the specifications of SN75LVDS82DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	unit
Vth	Differential Input High Voltage (Vcm=+1.2V)		100	mV
Vtl	Differential Input High Voltage (Vcm=+1.2V)	-100		mV

LVDS Timing



LVDS Macro AC characteristics.

Parameter	Symbol	Min	Typ	Max	Unit
LVDS Clock Cycle	Trxc	17.6	18.5	20	[ns]
LVDS Data Cycle	Trxd		Trxc/7		[ns]
Sample Data Setup Time (Trxc=Typ.)	Trxss	600			[ps]
Sample Data Hold Time (Trxc=Typ.)	Trxsh	600			[ps]
Data Sample Time	Trxs		Trxc/14		[ns]
Data Sample Cycle	Trxsc		Trxc/7		[ns]

Name	Description	Min	Typ	Max	Unit	Note
SELLVDS	High voltage	2	3	3.3	V	
	Low voltage	-0.1	0	0.7	V	
	Current	-1	-	1	mA	

5.5 Lamp Connector Signal Description

PIN #	SIGNAL NAME	Description
1	CFL-High	High voltage input for backlight CFL
2	CFL-Low	Low voltage input for backlight CFL

5.6 Lamp Connector Input Signal Electrical Characteristics

CFL Characteristics

CFL characteristics are as follows. Each parameter value is described for one CFL.

Symbol	Parameter	MIN	MAX	Units	Condition	Remark
ICFL	CFL Current	3	9	mArms	Ta=25C	Note 1
fCFL	CFL Frequency	30	80	KHz	Ta=25C	Note 2
ViCFL	CFL Ignition Voltage		1,500	Vrms	Ta=0C	
TdlyCFL	CFL Ignition Delay Time		1	second	Ta=25C	

Note 1: If the CFL current exceeds MIN/MAX values, then "CFL life", "ON/OFF cycle", and "Safety" will not be guaranteed.
Note 2: CFL frequency should be carefully determined to avoid interference between inverter and TFT LCD.

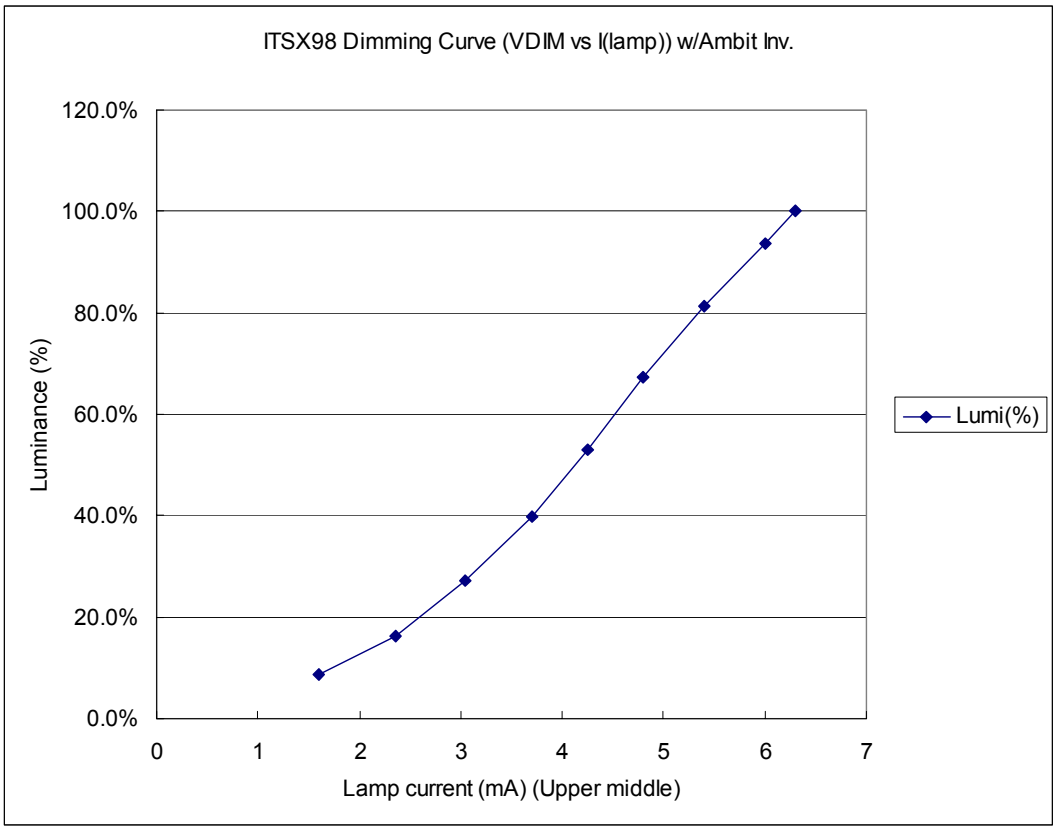
Inverter Design Point

Following is a guideline for the inverter. Each parameter value except White Luminance is described for one CFL.

Symbol	Parameter	MIN	Design Point	MAX	Units	Condition	Remark
(L63)	White Luminance	-	270	-	cd/m^2	Ta=25C	Note 1
ICFL	CFL Current	4	6.0	9	mA	Ta=25C	Note 2
VCFL	CFL Voltage (reference)		667		V	Ta=25C	Note 2
PCFL	CFL Power Consumption		4.0(x6)		W	Ta=25C	Note 3
fCFL	CFL Frequency	30	65	80	KHz	Ta=25C	Note 4
Vi_invCFL	CFL Ignition Voltage for Inverter	1,500		1,700	Vrms	Ta=0C	
Tdly_invCFL	CFL Ignition Delay Time for Inverter	1			second	Ta=25C	Note 5
ICFLp	CFL Peak Inrush Current			20	mA	Ta=25C	Note 6

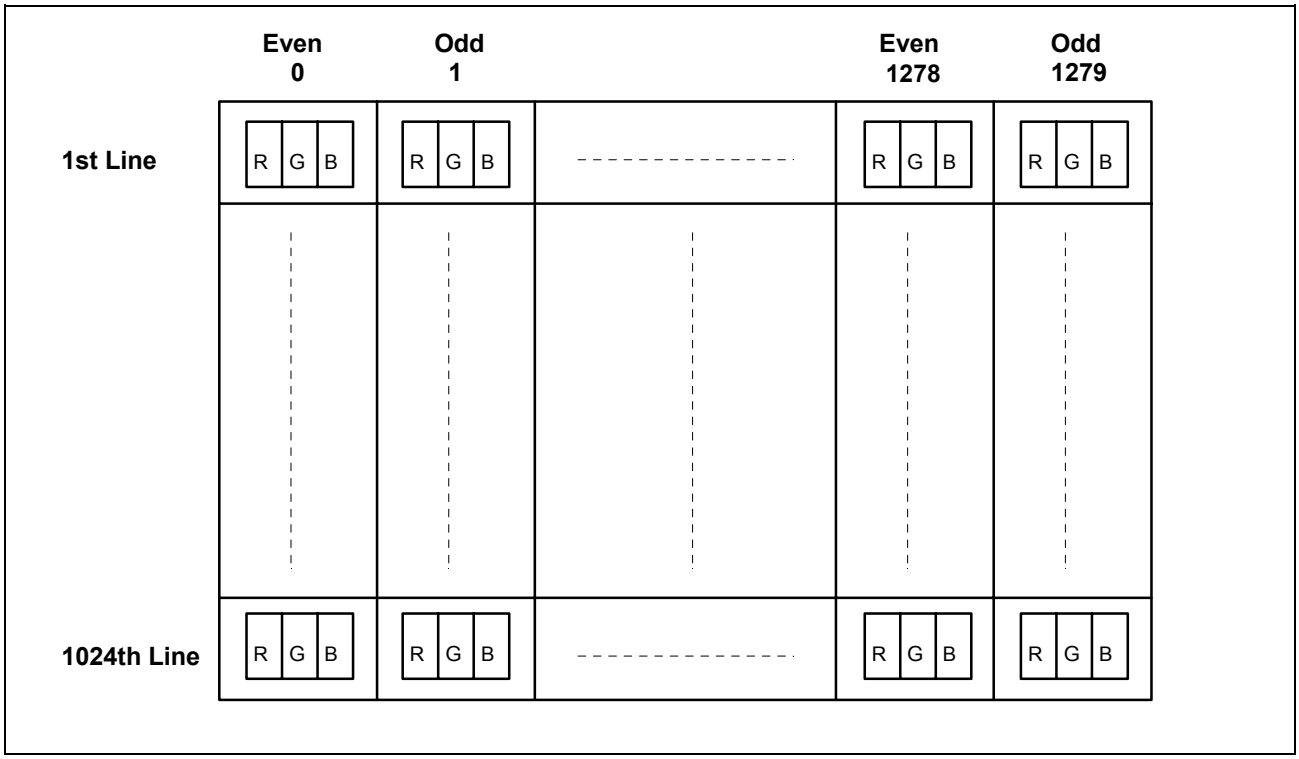
Note 1: Design Point; At white luminance 270 cd/m^2, PCFL=4.0x6 W is required.
Note 2: If the CFL current exceeds MIN/MAX values, then "CFL life", "ON/OFF cycle" and "Safety" will not be guaranteed.
Note 3: Caluculated value for reference (ICFL x VCFL = PCFL).
Note 4: CFL frequency should be carefully determined to avoid interference between inverter and TFT LCD.
Note 5: Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1.0 second unit discharge at least.
Note 6: (Duration = 50 msec)

The following chart is the Lamp current versus Luminance curve for your reference.



6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Odd and even pair of RGB data are sampled at a time.



7.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG(Texas Instruments) or equivalent.

7.1 Timing Characteristics

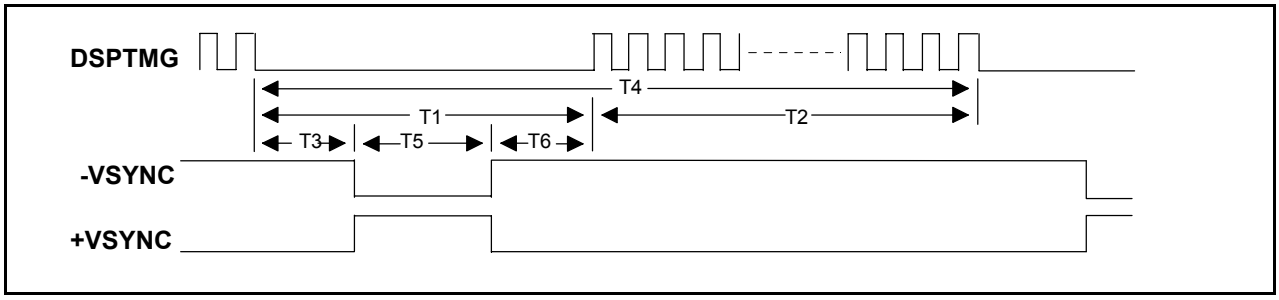
Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freq.	Fdck	50	54	56.8	MHz
DTCLK	Cycle	Tck	17.6	18.5	20	ns
+V-Sync	Frame Rate	1/Tv	56.25	60.02	61	Hz
+V-Sync	Cycle	Tv	16.39	16.66	17.78	ms
+V-Sync	Cycle	Tv	1035	1066	2047	lines
+V-Sync	active level	Tva	3	3		lines
+V-Sync	V-back porch	Tvb	7	38	63	lines
+V-Sync	V-front porch	Tvf	1	1		lines
+DSPTMG	V-Line	m	-	1024	-	lines
+H-Sync	Scan Rate	1/Th	-	63.98	-	KHz
+H-Sync	Cycle	Th	844	844	1023	Tck
+H-Sync	active level	Tha(*1)	4	56		Tck
+H-Sync	Back porch	Thb(*1)	4	124		Tck
+H-Sync	Front porch	Thf	4	24		Tck
+DSPTMG	Display Pixels	n	-	640	-	Tck

Note1 : Typical value is refer to VESA STANDARD.
(*1): Tha+Thb should be less than 1024 Tck.

Note2 : When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module Protection Mode.

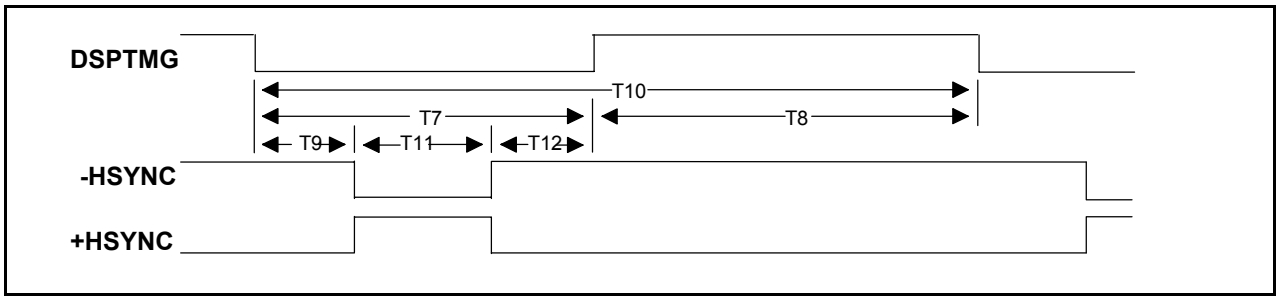
7.2 Timing Definition

Vertical Timing

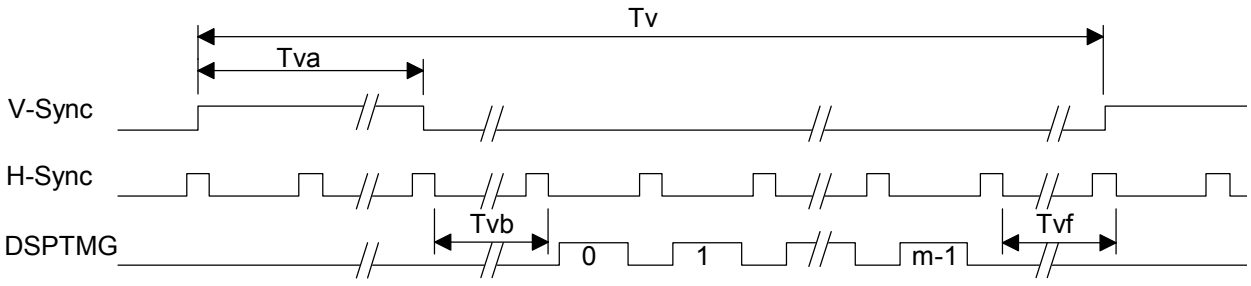


Support mode	T1 Vertical Blanking	T2 Active Field	T3 VSYNC Front Porch	T4 Frame Time	T5 VSYNC Width	T6 VSYNC Back Porch
1280 x 1024 at 60Hz (VESA STANDARD) (H line rate : 15.6 us)	0.656 ms (42 lines)	16.005 ms (1024 lines)	0.016 ms (1 line)	16.661 ms (1066 lines)	0.047 ms (3 lines)	0.594 ms (38 lines)

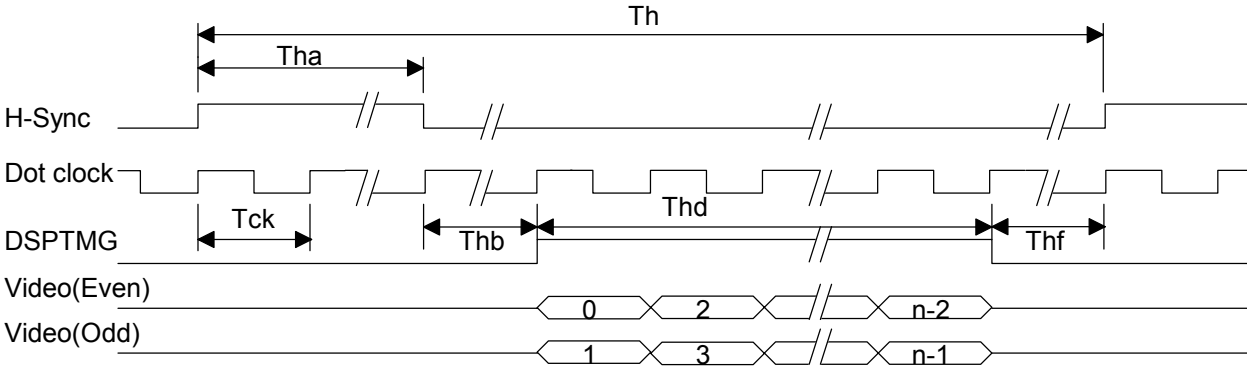
Horizontal Timing



Support mode	T7 Horizontal Blanking	T8 Active Field	T9 HSYNC Front Porch	T10 H line Time	T11 HSYNC Width	T12 HSYNC Back Porch
1280 x 1024 (VESA STANDARD) (Dotclock : 108.000 MHz)	3.778 us (408 dots)	11.852 us (1280 dots)	0.444 us (48 dots)	15.630 us (1688 dots)	1.037 us (112 dots)	2.296 us (248 dots)



Vsync, Hsync and Display Timing



Video signal, Hsync and Dot clock

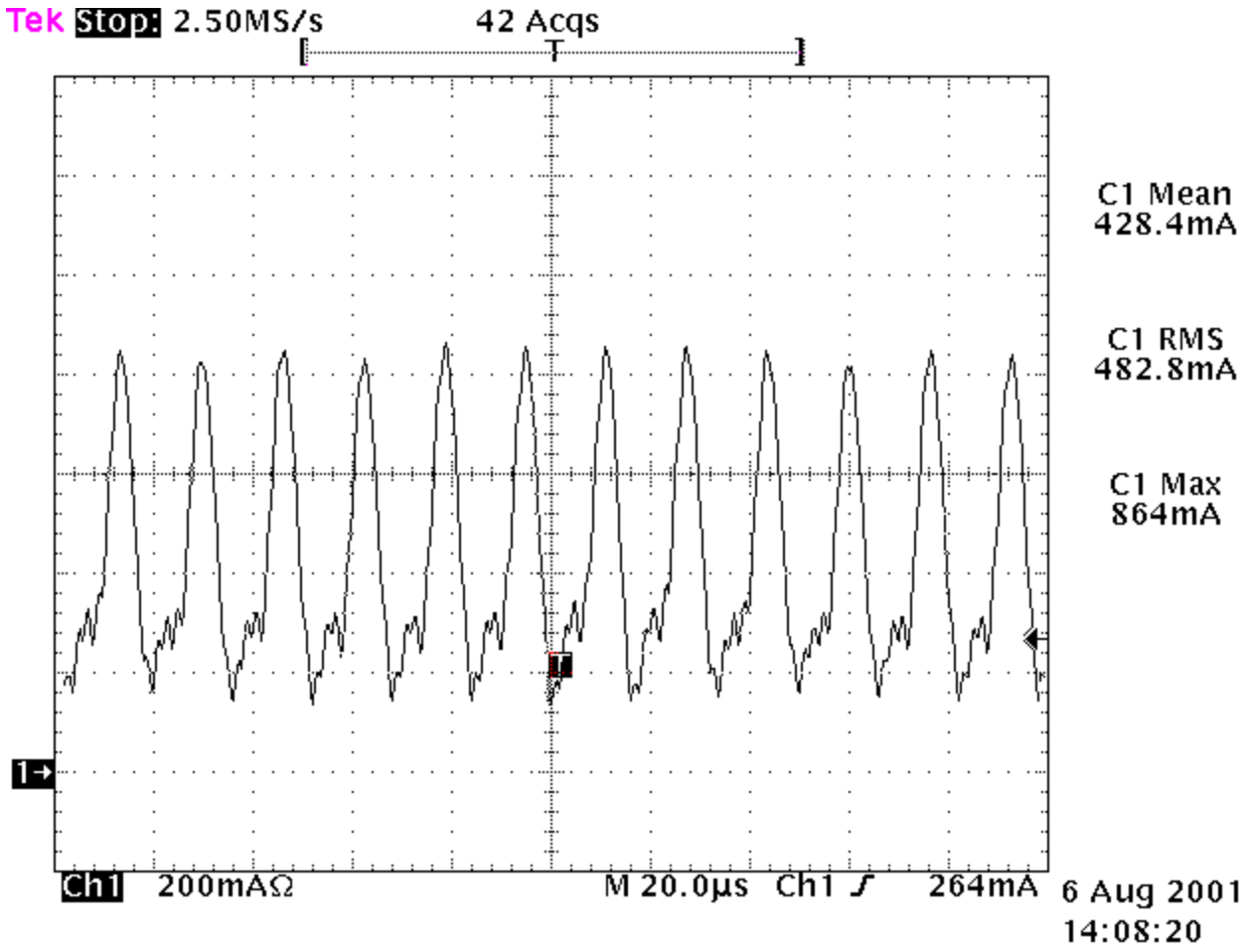
8.0 Power Consumption

Input power specifications are as follows;

SYMB	PARAMETER	Min	Typ	Max	UNITS	CONDITION
Vin	Logic/LCD Drive Voltage	11.4	12	12.6	V	
Iin	Vin Current			550	mA	Vin=11.4V (All White Pattern) (This value indicates long term average.)
Pin(1)	Vin Power		4.5		W	Typical Load Condition (Vertical Gray Bar, 256 Scale)
Pin(2)			5.2	6.3	W	Maximum Load Condition (All White)
	Logic/LCD DC current Waveform	Refer to the Typical Logic/LCD Current Waveform shown in the following Figure. Waveform may vary in paticular application. Actual current waveform on user application must be evaluated and make sure the ripple current and/or peak current should be allowable to user power supply.				Maximum Load Condition (All White)
Vin rp	Allowable Logic/LCD Drive Ripple Voltage			500	mVp-p	
VBL	Backlight power voltage	11.4	12	12.6	V	

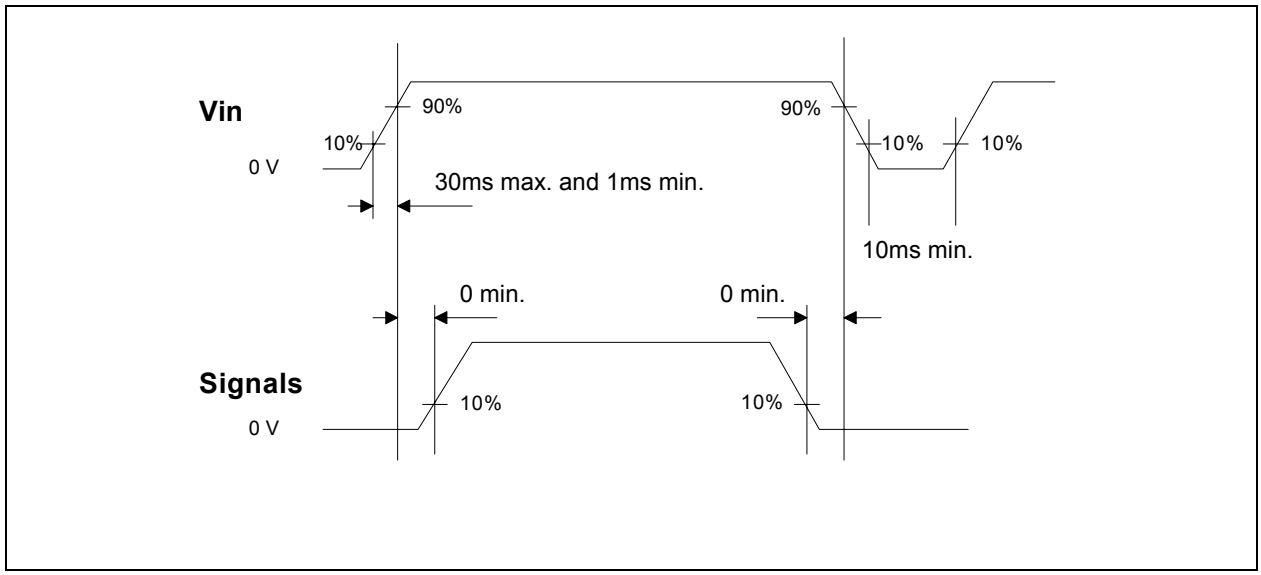
(Note) A used DC power supply for this LCD module should be have a over current protection function to safety.

Figure. Typical Logic/LCD Current Waveform
Condition : Maximum Load Condition(All White)
Voltage : 12.0V measured at Interface Connector J1
Interface Cable : AWG28, 30 Conductors, L=500mm from Voltage Source to EUT

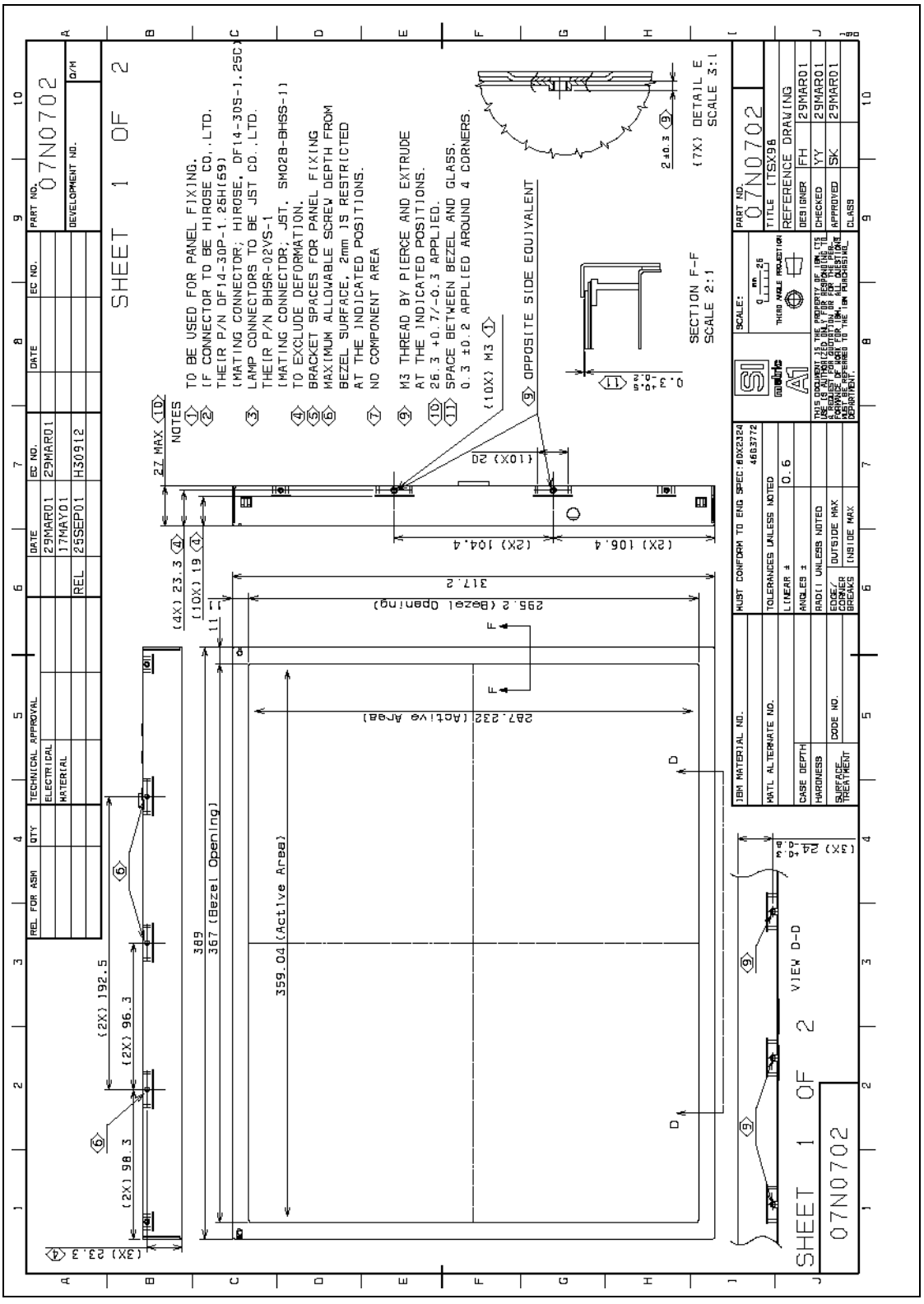


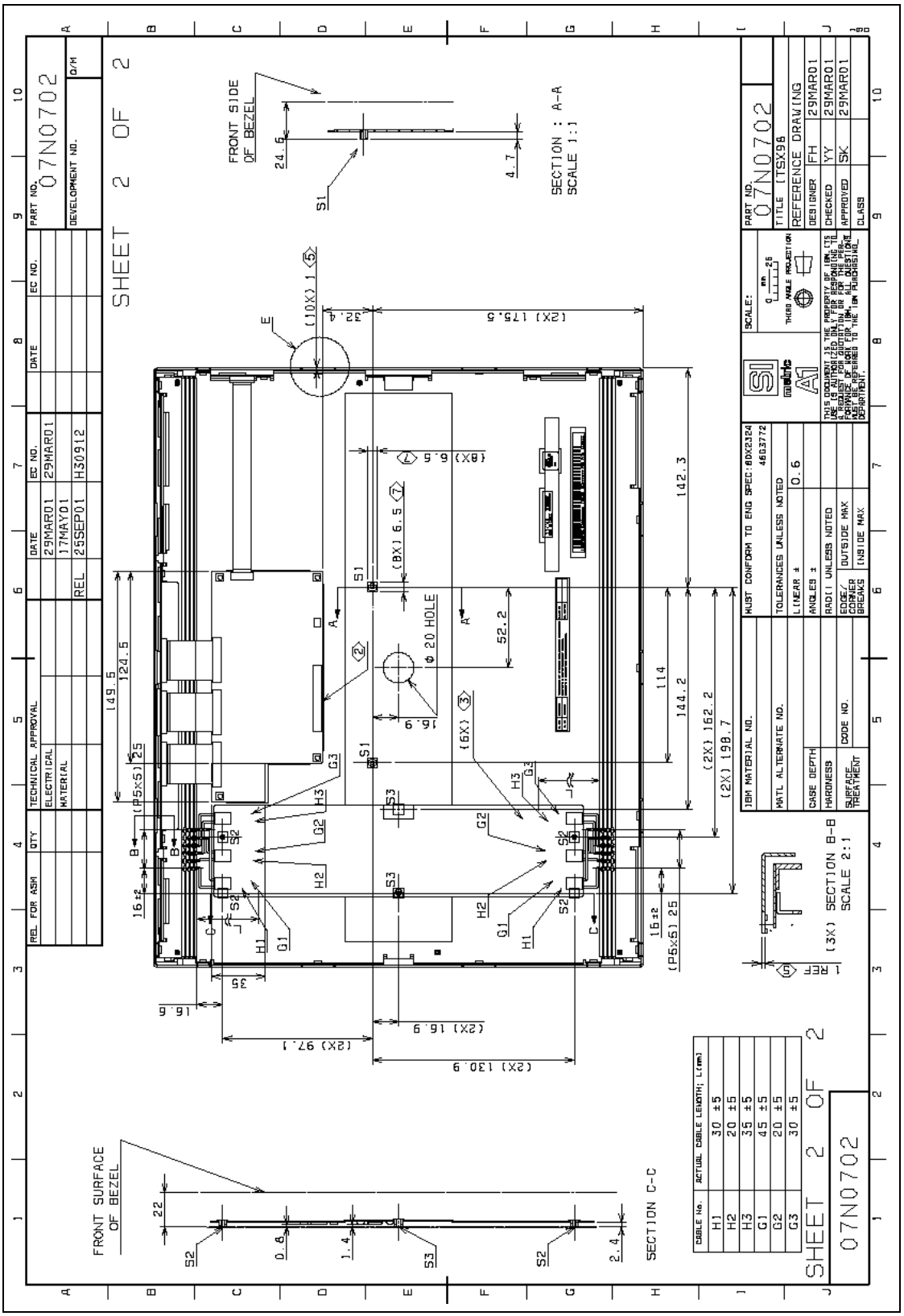
9.0 Power ON/OFF Sequence

Vin and VBL power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin is off.
It is recommended that the Lamp on signal should be supplied after other signals are stable in order to avoid visible screen noise when power-on.



10.0 Mechanical Characteristics





11.0 National Test Lab Requirement

The display module will satisfy all requirements for compliance to

UL60950 3rd. Ed.	U.S.A. Information Technology Equipment

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