Engineering Specification

Type 14.1 XGA Color TFT/LCD Module
Model Name:IAXG15H

Document Control Number : OEM I-915H-02

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

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ii Record of Revision

Date	Document Revision	Page	Summary
December 4,2001	OEM I-915H-01	All	First Edition for customer. Based on Internal Spec. EC H300970 as of November 7,2001. To adopt a "Burst Mode Inverter".
April 10,2002	OEM I-915H-02	 6 8 9 17 20 21 25 27,28	Based on Internal Spec. EC H300972 as of April 8,2002. To update the following items. • White Luminance • Backlight Power Consumption • Weight • Physical Size To update the value of Shock. To update Optical Rise Time + Fall Time. To add Cycle Modulation Rate. To update Inverter Signal Electrical Characteristics. To update the SMData versus the Luminance. To update Power Consumption. To update Reference Drawings.

1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle with care when mount in the system cover. Mechanical damage for lamp cable/lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end product.
- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the Type 14.1 Color TFT/LCD Module 'IAXG15H'.

This module is designed for a display unit of notebook style personal computer.

The screen format and electrical interface are intended to support the XGA (1024(H) x768(V))screen.

Support color is native 262k colors (RGB 6-bit data driver).

All input signals are LVDS interface compatible. This module contains an inverter card for backlight.

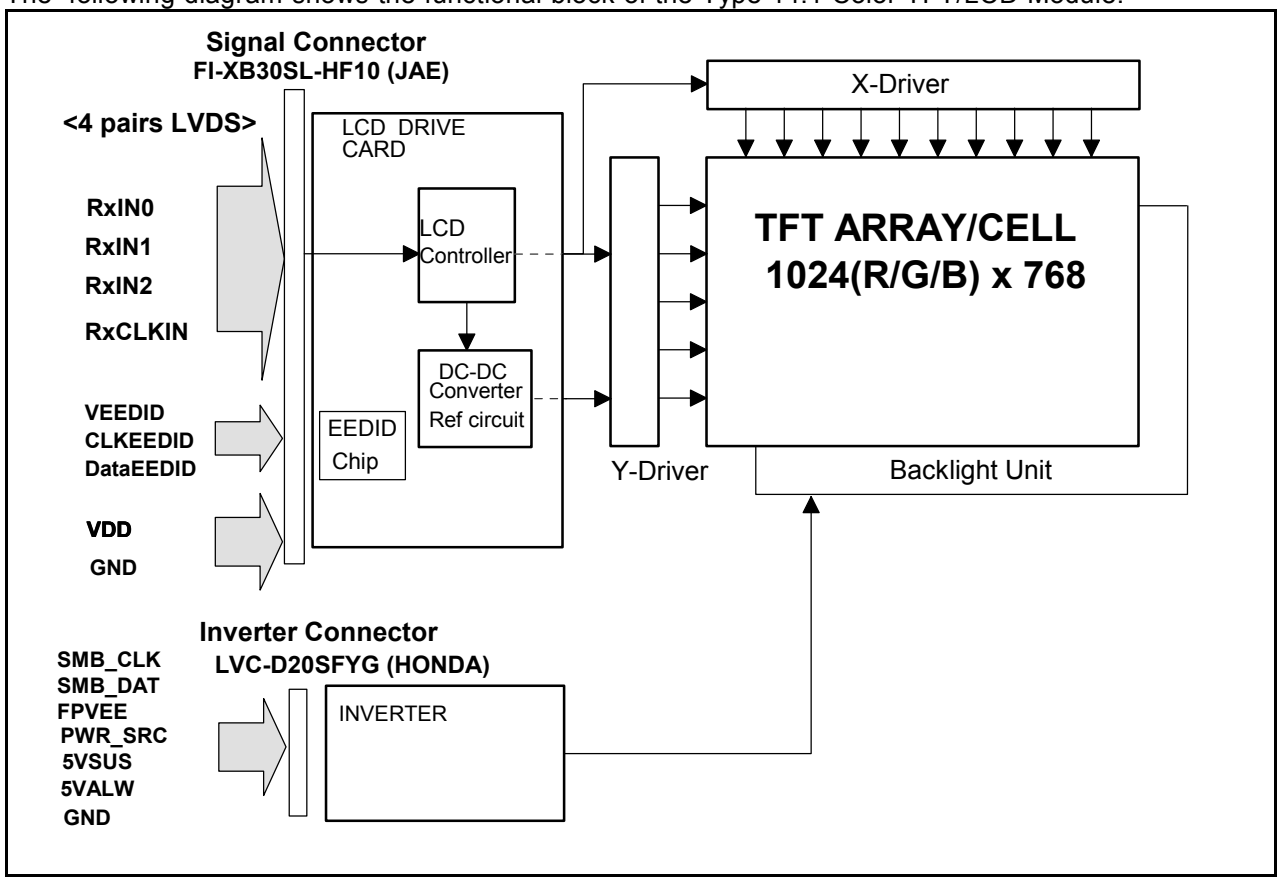
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	357
Active Area [mm]	285.7(H) x 214.3(V)
Pixels H x V	1024(x3) x 768
Pixel Pitch [mm]	0.279(per one triad) x 0.279
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
White Luminance [cd/m^2] SMData=FFH: @14.4V SMData=00H: @14.4V	 8.5 Typ.(center) 170 Typ., 150 Min.(5 Points average)
Contrast Ratio	250 : 1 Typ.
Optical Rise Time + Fall Time [msec]	50Max.
Nominal Input Voltage [Volt] VDD 5VSUS,5VALW line PWR_SRC line	 +3.3 Typ. +5.0 Typ. +14.4 Typ.
Logic Power Consumption [watt] (VDD Line)	1.2 Typ. (All Black Pattern)
Backlight Power Consumption [watt] PWR_SRC line SMData=00H (at:PWR_SRC=14.4V)	4.8 Typ.
Weight [grams]	440 Max. (with Inverter)
Physical Size [mm]	299.0(W)x 239.4(H) x 5.5(D) Typ.(with Inverter space) 299.0(W)x 226.5(H) x 5.2(D) Typ.(without Inverter space)
Electrical Interface (Logic)	4 pairs LVDS(R/G/B Data (6-bit), 3 sync signals, Clock), EEDID(clock, data)
Electrical Interface (Inverter)	SMB_CLK,SMB_DAT,FPVEE
Support Color	Native 262K colors (RGB 6-bit data driver)
Temperature Range (degree C) Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the Type 14.1 Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+4.0	V	
	5VSUS, 5VALW	-0.3	+5.5	V	
	PWR_SRC	-0.3	+25	V	
Input Voltage of Signal	Vin	-0.3	+VDD+0.3	V	
	FPVEE	-0.3	5.5	V	
	SMB_CLK SMB_DAT	-1.0	7.0	V	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Humidity	HOP	8	95	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	
Shock			50 18 220 2	G ms G ms	Rectangle Wave Half Sine Wave

Note 1 : Maximum Wet-Bulb should be 39 degree C and No condensation.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≧10 (Left)	40 40	- -
	Vertical (Upper) K≧10 (Lower)	15 30	- -
Contrast ratio		250	-
Response Time (ms)	Rising + Falling	-	50 Max.
Color Chromaticity (CIE)	Red x	0.577	-
	Red y	0.338	-
	Green x	0.310	-
	Green y	0.554	-
	Blue x	0.158	-
	Blue y	0.124	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2) SMData=00H		170 5 Points Average	150 Min.

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Type / Part Number	FI-X30M, FI-X30C2L

Connector Name / Designation	For Inverter Connector
Manufacturer	HONDA
Type / Part Number	LVC-D20SFYG
Mating Type / Part Number	LVC-C20LPMSG

5.2 Interface Signal Connector

Pin #	Signal Name
1	FG (GND)
2	GND
3	VDD
4	VDD
5	V_{EEDID} **(Note 2,3)**
6	Reserved **(Note 1)**
7	CLK_{EEDID} **(Note 2,4)**
8	$Data_{EEDID}$ **(Note 2,4)**
9	RxIN0- **(Note 5)**
10	RxIN0+ **(Note 5)**
11	GND
12	RxIN1- **(Note 5)**
13	RxIN1+ **(Note 5)**
14	GND
15	RxIN2- **(Note 5)**
16	RxIN2+ **(Note 5)**

Pin #	Signal Name
17	GND
18	RxCLKIN- **(Note 5)**
19	RxCLKIN+ **(Note 5)**
20	GND
21	Reserved **(Note 1)**
22	Reserved **(Note 1)**
23	Reserved **(Note 1)**
24	Reserved **(Note 1)**
25	Reserved **(Note 1)**
26	Reserved **(Note 1)**
27	Reserved **(Note 1)**
28	Reserved **(Note 1)**
29	Reserved **(Note 1)**
30	Reserved **(Note 1)**
31	Reserved **(Note 1)**
32	FG (GND)

Note :

1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3". This module is equipped with a I^2C compatible EEPROM FM24C03U (Fairchild Semiconductor International), whose device address is fixed zero.
3. V_{EEDID} power source shall be the limited current circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC™) Proposed Standard", VESA)
4. Both CLK_{EEDID} line and $DATA_{EEDID}$ line are pulled up with 10k ohm resistor to V_{EEDID} power source line at LCD panel, respectively.
5. Voltage levels of all input signals are LVDS compatible. Refer to "Signal Electrical Characteristics for LVDS", for voltage levels of all input signals.

5.3 Interface Signal Description

Signal Name	Description
RxIN0+, RxIN0-	LVDS differential data input (Red0-Red5, Green0)
RxIN1+, RxIN1-	LVDS differential data input (Green1-Green5,Blue0-Blue1)
RxIN2+, RxIN2-	LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG)
RxCLKIN+, RxCLKIN-	LVDS differential clock input
VEEDID	EEDID 3.3V Power Supply
CLKEEDID	EEDID Clock
DataEEDID	EEDID Data
VDD	+3.3V Power Supply
GND	Ground

Note:

- The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
- Input signals shall be low or Hi-Z state when VDD is off.

SIGNAL NAME	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	Data Clock	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals.
DSPTMG	Display Timing	This signal is strobed at te falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .
V_{EEDID}	V_{EEDID}	EEDID 3.3V Power Supply
CLK_{EEDID}	CLK_{EEDID}	EEDID Clock
$Data_{EEDID}$	$Data_{EEDID}$	EEDID Data

Note : Output signals from any system except EEDID signals shall be low or Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

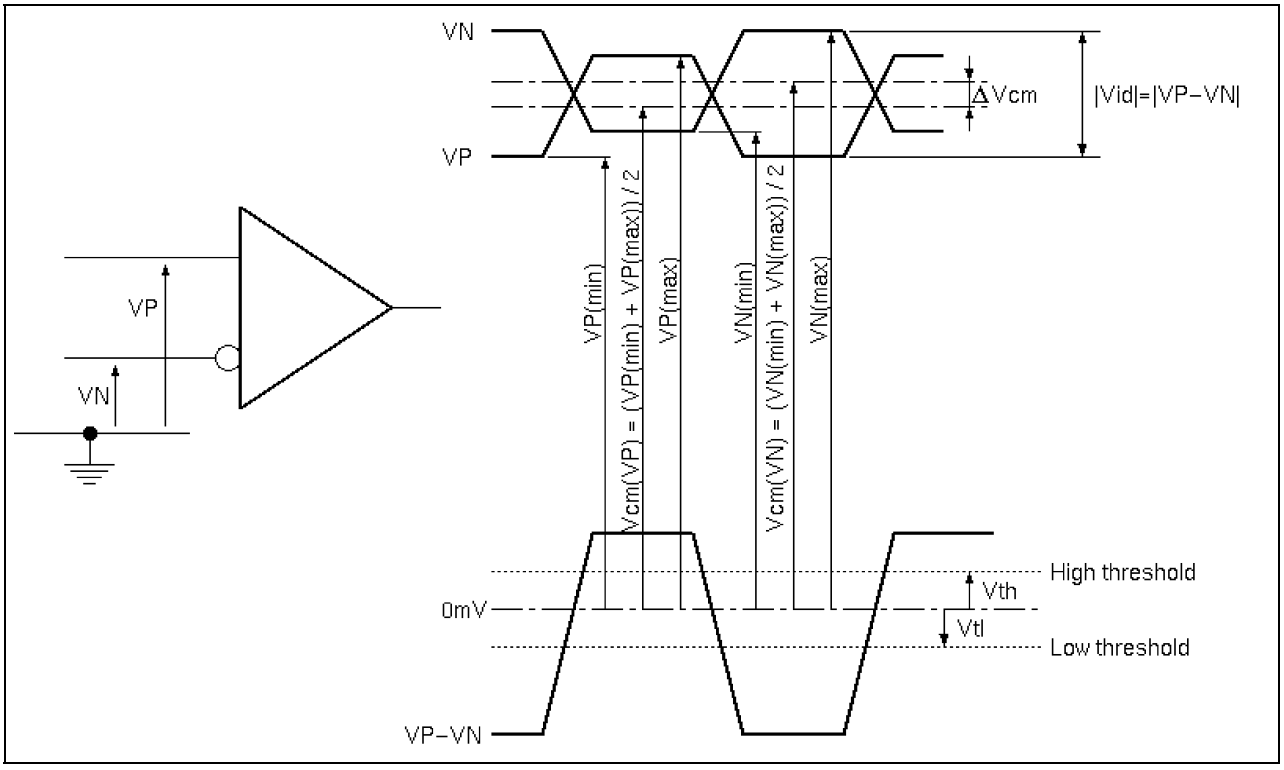
Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	1.0	1.2	1.4	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	△Vcm	-50		+50	mV	Vth - Vtl = 200mV

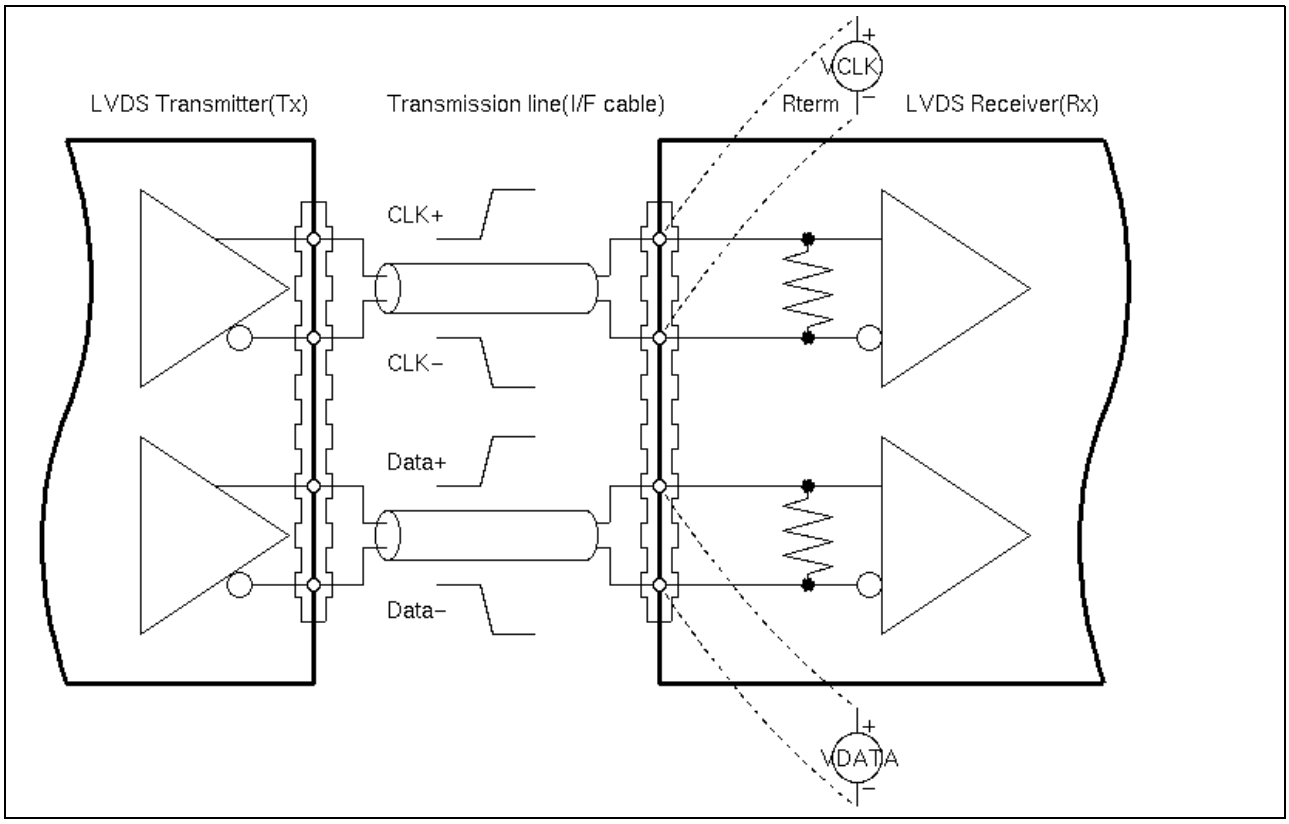
Note:

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Voltage Definitions



Measurement System



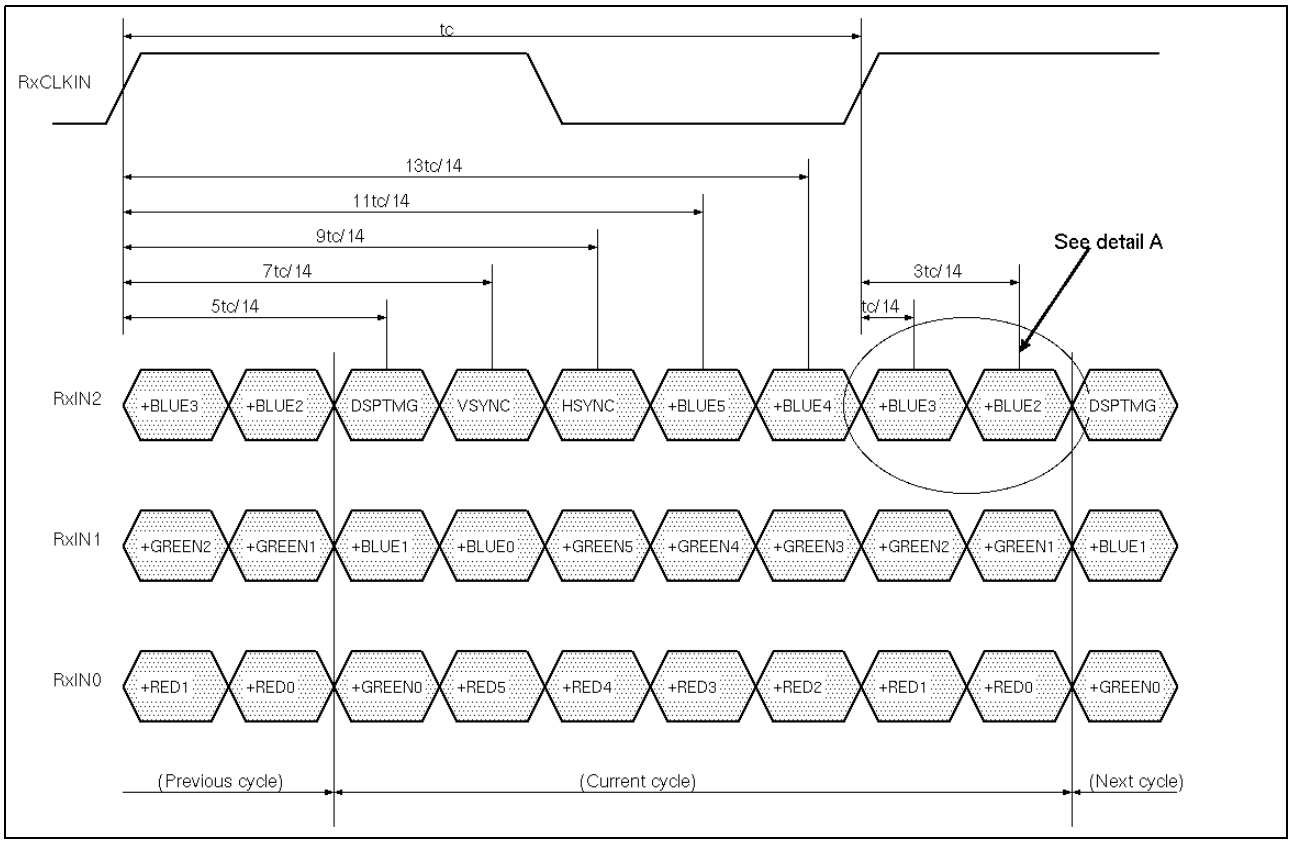
Timming Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	50	65	67	MHz	
Cycle Time	tc	14.93	15.38	20.00	ns	
Data Setup Time(Note 1)	Tsu	600			ps	fc = 65MHz, tCCJ < 50ps, Vth-Vtl = 200mV, Vcm = 1.2V, △Vcm = 0
Data Hold Time(Note 2)	Thd	600			ps	
Cycle-to-cycle jitter(Note 3)	tCCJ	-150		+150	ps	fc = 65MHz, Tsu=Thd=900ps
Cycle Modulation Rate(Note 4)	tCJavg			20	ps/clk	fc = 65MHz, Tsu=Thd=900ps

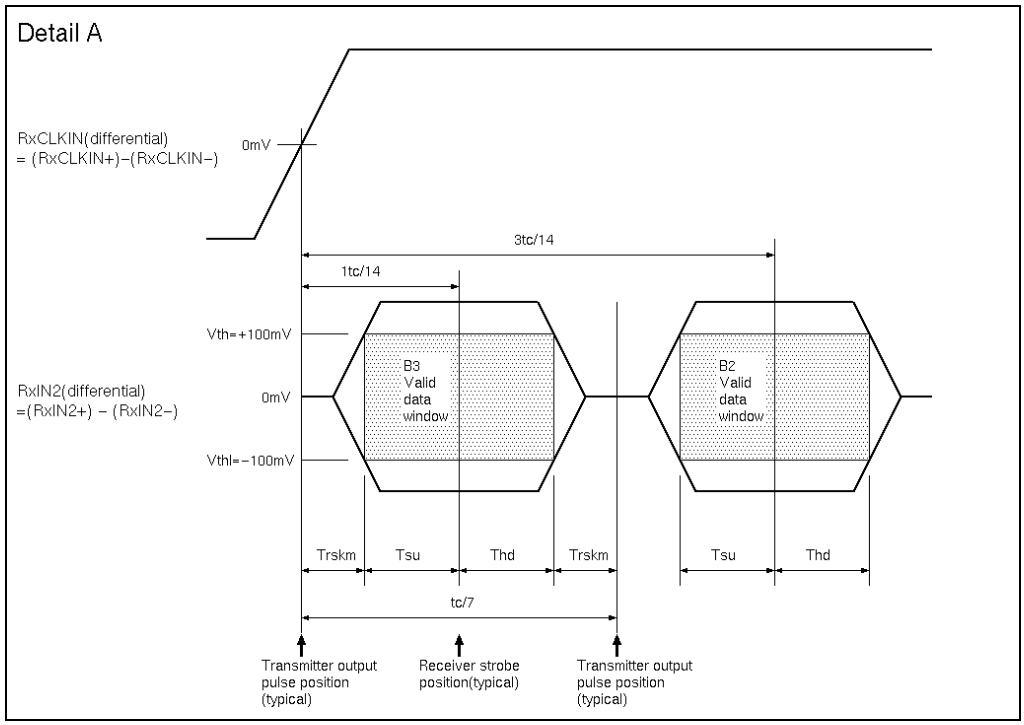
Note :

1. All values are at VDD=3.3V, Ta=25 degree C.
2. See figure "Timing Definition" and "Timing Definition(detail A)" for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. Figure "Cycle Modulation Rate" illustrates a case against this requirement.
   This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Timing Definition

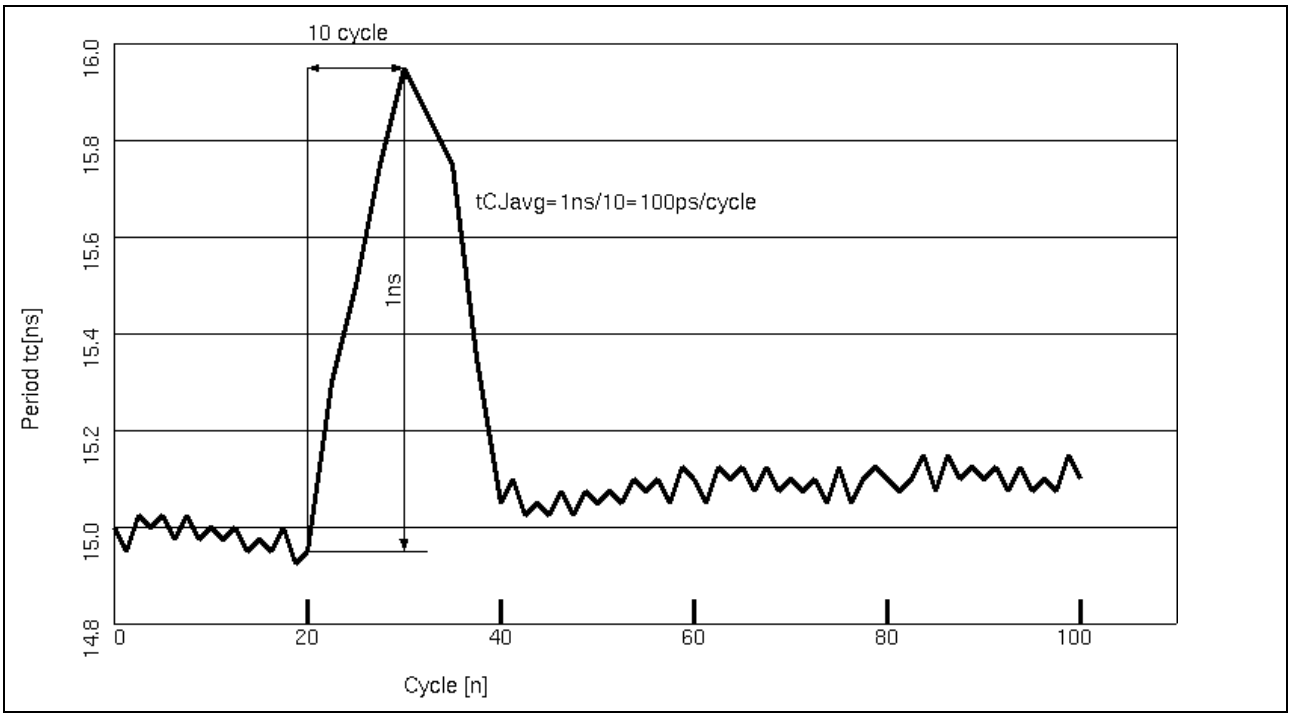


Timing Definition (detail A)



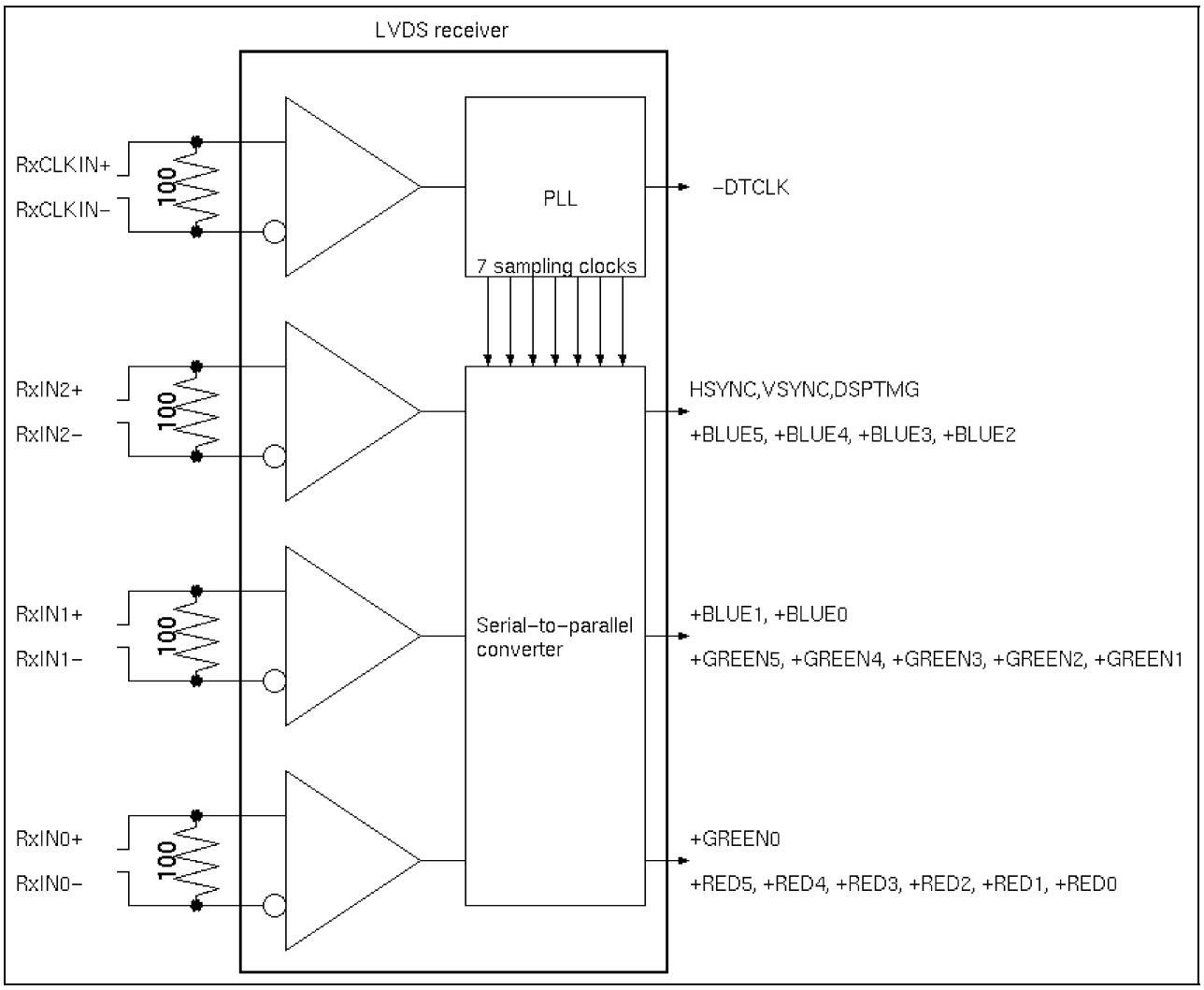
Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

Cycle Modulation Rate



5.4.2 LVDS Receiver Internal Circuit

The following figure shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

- Following the suggestions below will help to achieve optimal results.
- Use controlled impedance media for LADS signals. They should have a matched differential impedance of 100 ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TEL signals from LADS signals.
- For cables, twisted pair, twin, or flex circuit with close coupled differential traces are recommended.

5.5 Inverter Signal connector

Pin#	Signal Name
1	PWR_SRC
2	PWR_SRC
3	PWR_SRC
4	NC (No Connection)
5	GND
6	5VSUS
7	5VALW
8	GND
9	SMB-DAT
10	SMB-CLK

Pin#	Signal Name
11	GND
12	FPVEE
13	GND
14	NC (No Connection)
15	NC (No Connection)
16	NC (No Connection)
17	NC (No Connection)
18	NC (No Connection)
19	NC (No Connection)
20	NC (No Connection)

5.6 Inverter Signal Description

SIGNAL NAME	Description	Note
5VSUS	Power source for the control circuit on the inverter.	4.85 to 5.2V
5VALW	Power source for storing the brightness value and for the interfacing with SMB-CLK & SMB-DAT	
FPVEE	Control signal input into the inverter to turn the backlight ON/OFF	3.3V : ON 0V : OFF
PWR_SRC	Power rail to drive the backlight inverter	9.0V to 21.0V
SMB-CLK SMB-DAT	SMBus interface for sending brightness information to the inverter	0V,5V
GND	Ground	

Note : Output signals from any system shall be low or hi-fi state when VDD is off.

5.7 Inverter Signal Electrical Characteristics

Electrical Specifications

Item	Symbol	Min.	Typ.	Max.	UNITS	CONDITION
Input Voltage	PWR_SRC	9.0	14.4	21	[V]	(Ta=25degree C)
	5VSUS, 5VALW	4.85	5.0	5.2	[V]	
Input Power	P(PWR_SRC) PWR_SRC=14.4[V]		4.8	5.5	[W]	SMData=00H
			0.7	1.0	[W]	SMData=0FFH
	P(5VSUS)		15	25	[mW]	
	P(5VALW)		5	25	[mW]	
ON/OFF	FPVEE	2.0			[V]	ON
	FPVEE			0.8	[V]	OFF
Lamp Frequency	F	52	59	66	[KHz]	
Burst Frequency	F_B	130	150	170	[Hz]	

Dimming

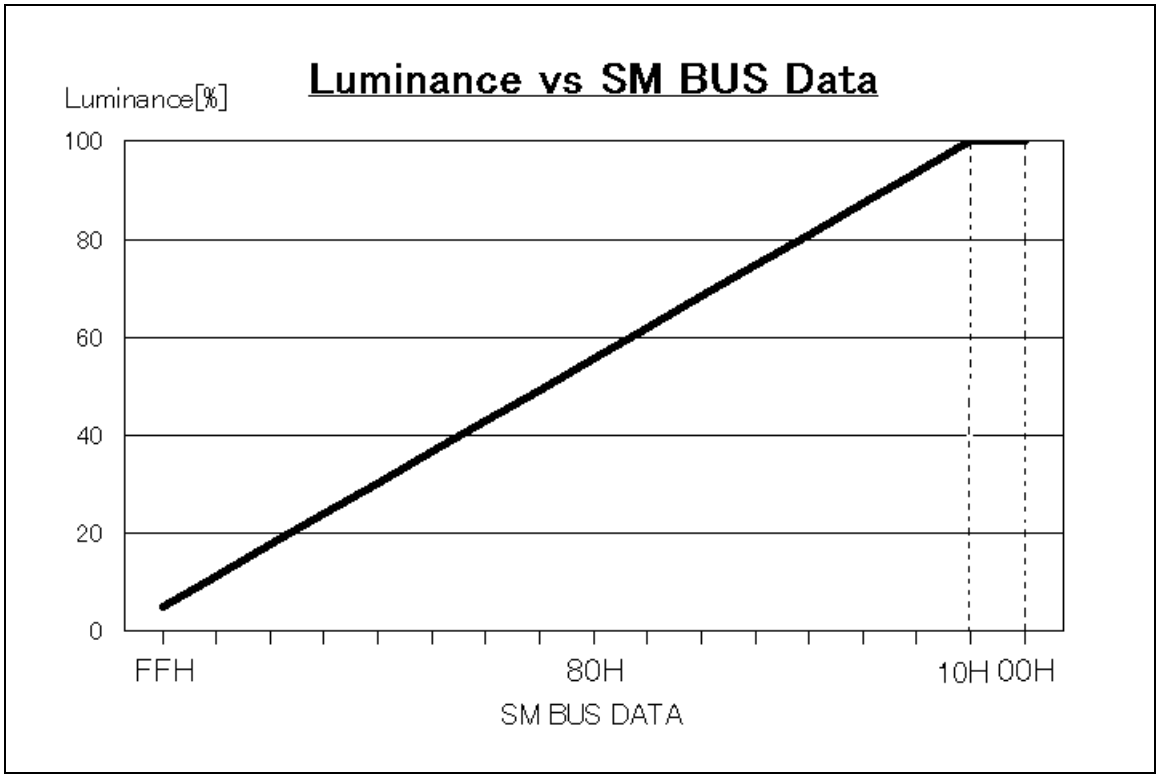
SMData	Brightness [%]			Brightness (5pts) [cd/m^2]	Lamp Current (Return side)[mA]
	Min.	Typ.	Max.		
00H	-	100	-	170 **(*1)**	6.5 **(*1)**
0FFH	2	5	9	8.5 **(*1)**	1.7 **(*1)**

***1** : Reference Only

SMBUS Data

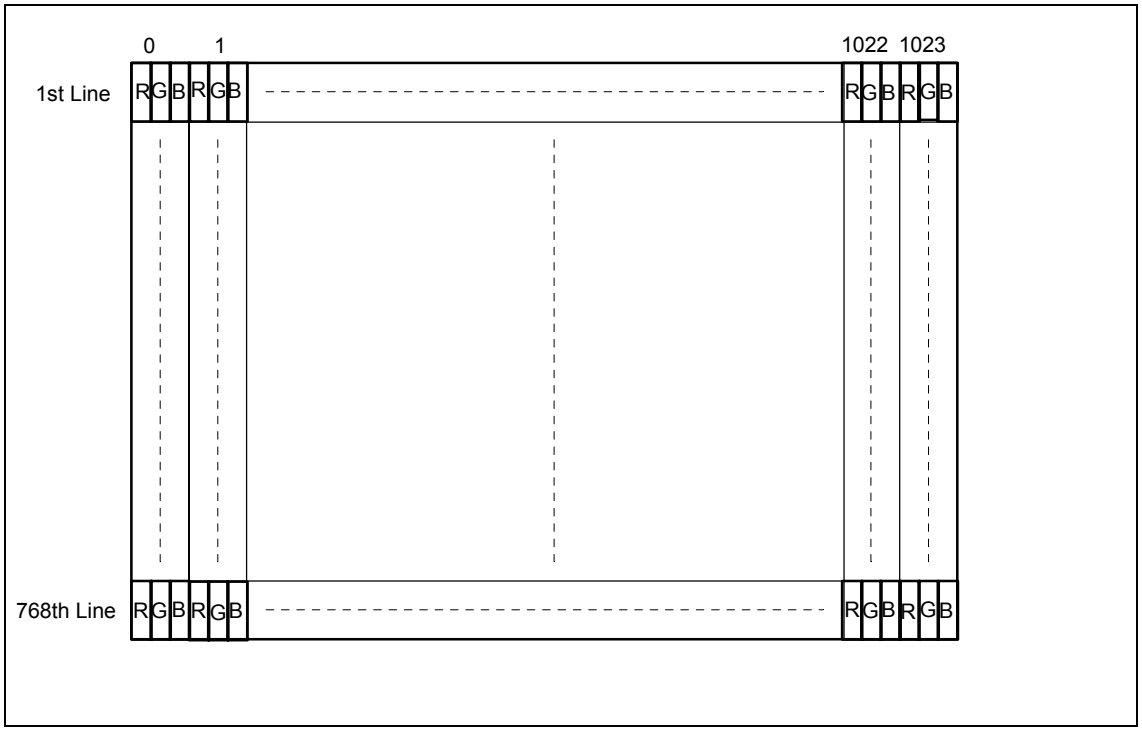
SMBUS	Device Identifier	Device Address
	0101	100

The following chart is the SMData versus the Luminance for your reference.



6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.



7.0 Interface Timings

Basically, interface timings should match the VESA 1024x768 / 60 Hz (VG901101) manufacturing guide line timing. These timings described here are not actual input timings of LCD module but output timings of SN75LVDS86DGG(Texas Instruments) or equivalent.

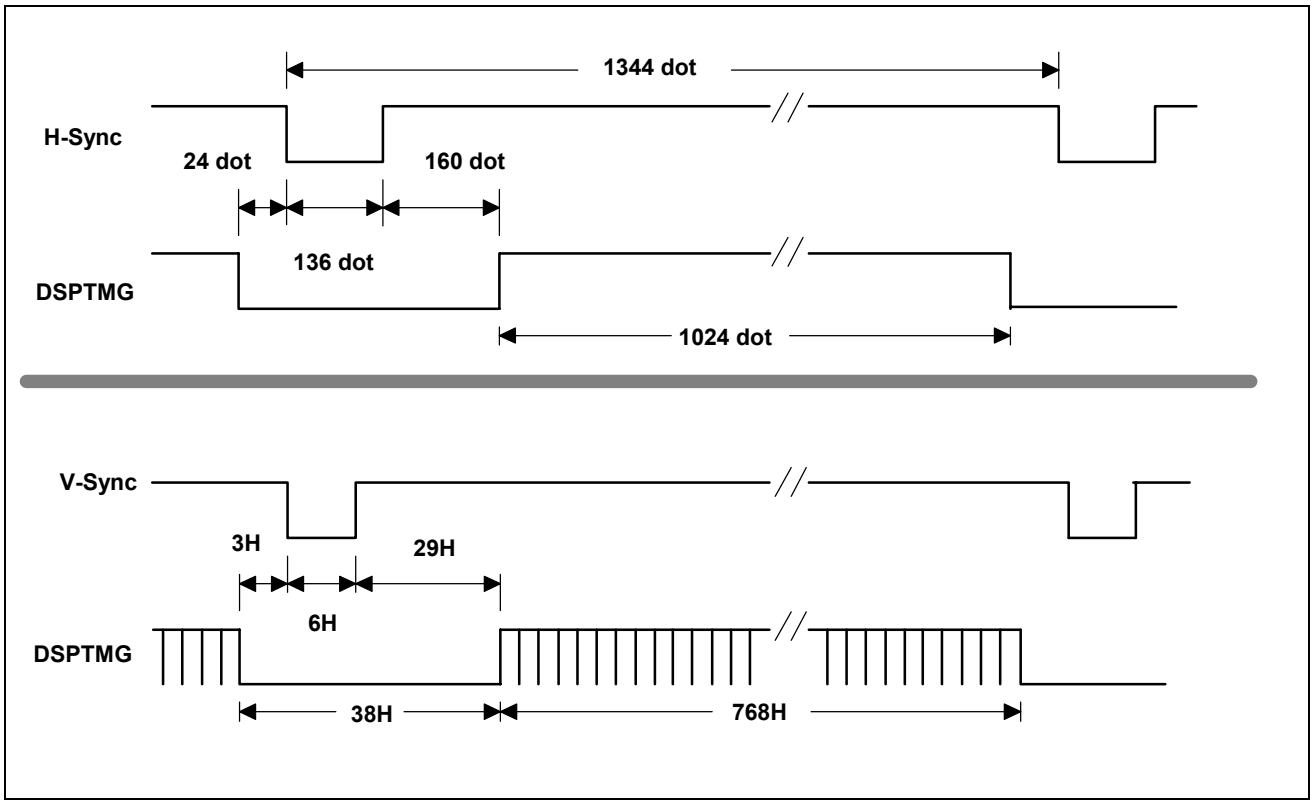
7.1 Timing Characteristics

Symbol		MIN	TYP	MAX	Unit	Note
fdck	DTCLK Frequency		65.00		MHz	
tck	DTCLK cycle time		15.38		nsec	
tx	X total time	1206	1344	2047	tck	
tacx	X active time	1024	1024	1024	tck	
Hsync	H frequency		48.363		KHz	
Hsw	H-Sync width	8	136		tck	2
Hbp	H back porch	8	160		tck	2
Hfp	H front porch	0	24		tck	
ty	Y total time	777	806	1023	tx	
tacy	Y active time	768	768	768	tx	
Vsync	Frame rate	(55)	60	61	Hz	
Vw	V-sync Width	1	6		tx	
Vfp	V-sync front porch	1	3		tx	
Vbp	V-sync back porch	7	29	63	tx	3

Note1 : tbkx = Hfp + Hsw + Hbp
Note2 : Hsw + Hbp should be less than 515 [tck].
Note3 : Vbp should be static.

When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module Protection Mode.

7.2 Timing Definition



8.0 Power Consumption

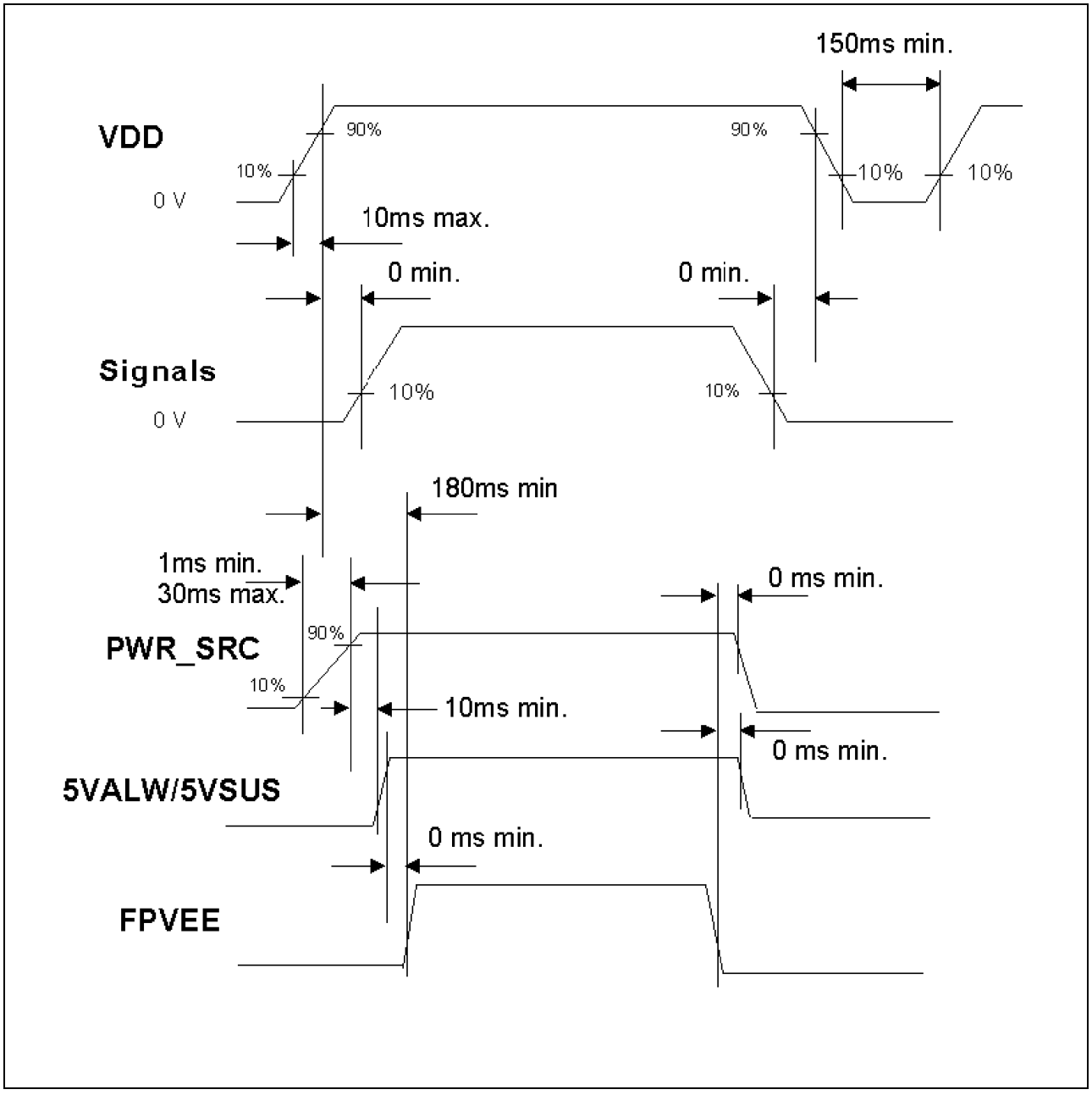
Input power specifications are as follows;

Power Requirements

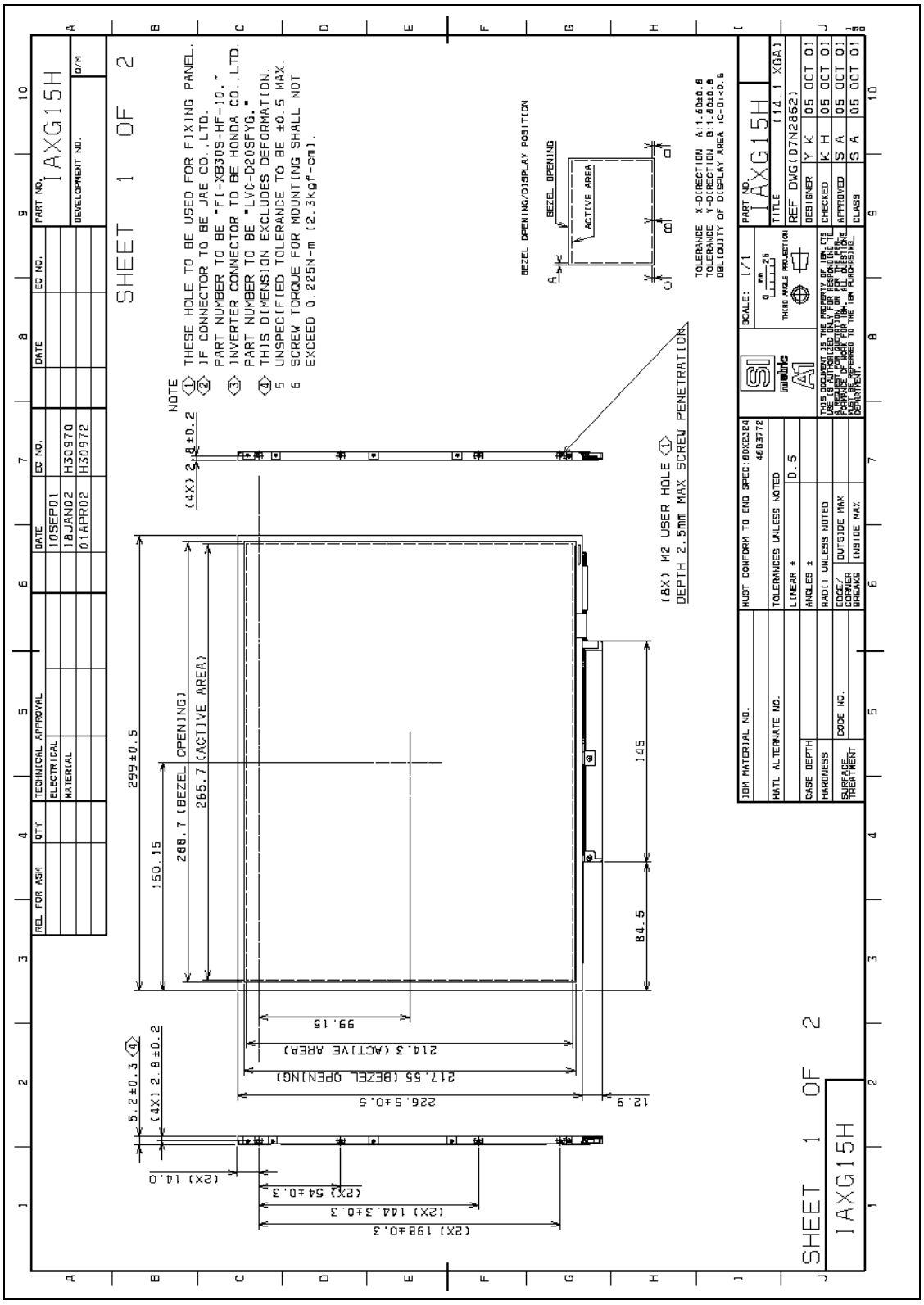
SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 20[uF]
PDD	VDD Power			1.91	[W]	Max. Pattern, VDD=3.6[V]
PDD	VDD Power		1.2		[W]	All Black Pattern, VDD=3.3[V]
IDD	VDD Current			530	[mA]	Max Pattern, VDD=3.6[V]
IDD	VDD Current		360		[mA]	All Black Pattern, VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	

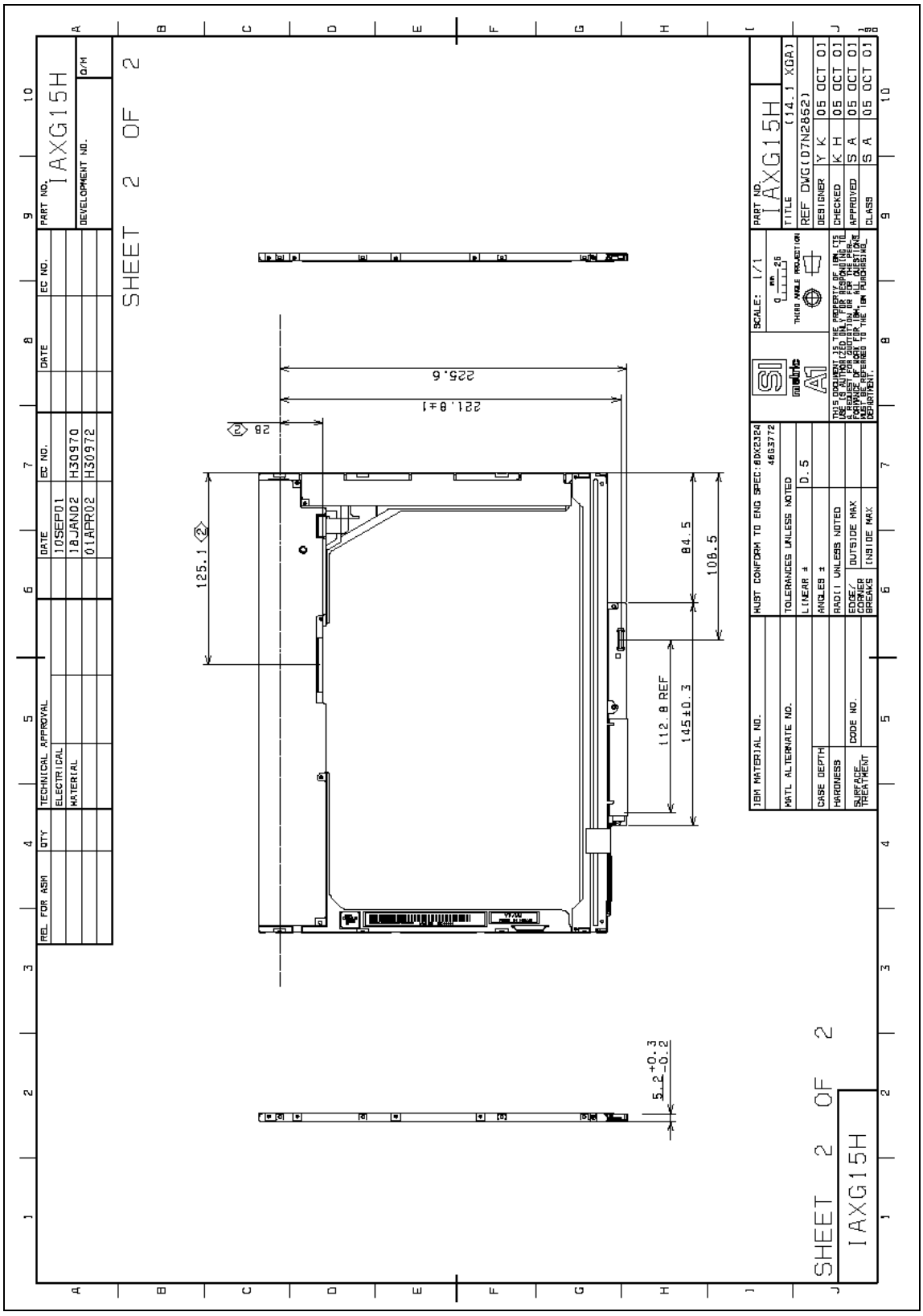
9.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



10.0 Mechanical Characteristics





11.0 National Test Lab Requirement

The display module satisfied all requirements for compliance to

UL 1950, 3rd Edition U.S.A. Information Technology Equipment

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