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Specification of Fast Response Time Driving Circuit
for 19 inch SXGA TFT-LCD

FLCB-12

Approval

Date :

By :

This Product is designed, developed and manufactured as contemplated for general use, including without limitation, general office use, personal use, household use, and ordinary industrial use, but is not designed, developed and manufactured as contemplated for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (hereinafter "High Safety Required Use"), including without limitation, nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system. If customer's product possibly falls under the category of High Safety Required Use, please consult with our sales representatives in charge before such use. In addition, FDTC shall not be liable against the customer and/or any third party for any claims or damages arising in connection with the High Safety Required Use of the Product without permission.

Specification No. : Tech Bes LCD-00205

Issue Date : Jun. 6, 2003

Issued by :



FUJITSU DISPLAY TECHNOLOGIES CORPORATION

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1. APPLICATION

This specification applies to the Fast Response Driving Time Circuit of the 19"-SXGA supported TFT LCD module for the "FLC48SXC8V-XX".

2. PRODUCT NAME AND MODEL NUMBER

2.1 Product Name: Fast Response Time Driving Circuit for FLC48SXC8V-XX

2.2 Model Number: FLCB-12

2.3 Drawing Number: NA19002-4243

3. OVERVIEW

This module is a mounting circuit, which contains a data compensation driving function for the purpose of improving the liquid crystal response of the 19" SXGA supporting TFT-LCD module.

This module can suppress the response within a frame by detecting the change of the display signal between frames and converting the data excluding an area.

The power supply is +5V DC.

The set up of this circuit is applicable to FLC48SXC8V-05.

4. CONFIGURATION

This module is configured from a LVDS receiver, controller IC, frame memory and a LVDS transmitter.

A diagram of the configuration block for this module is shown in Figure 4-1.

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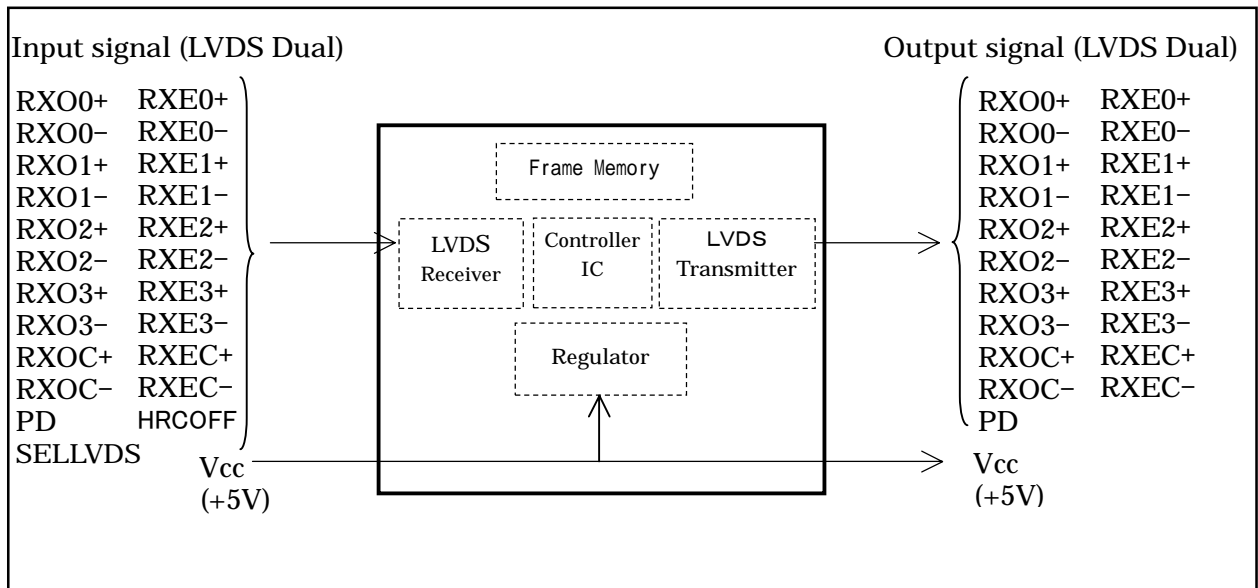


Figure 4-1 Diagram of the Configuration Block

5 . MECHANICAL SPECIFICATION

The mechanical specification for this module is shown in table 5-1.

Table 5-1 Mechanical Specifications

Item	Specification	Unit	Remarks
Outline measurement	106×142×5.3(typ)	mm	Outline diagram is shown in P19.
Weight	60 max	g	

6. ABSOLUTE MAXIMUM RATINGS

The absolute maximum rating for this module is shown in table 6-1.

Table 6 - 1 Absolute Maximum Rating

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V _{CC}	T _a =25°C	-0.3	—	6.0	V
Input Voltage (LVDS Signal, HRCOFF, SELLVDS, PD)	V _{IN}	T _a =25°C	-0.3	—	3.6	V

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7.RECOMMENDED OPERATING CONDITION

The recommended operating condition for this module is shown in Table 7-1.

Table 7-1 Recommended Operating Condition

Item	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V_{CC}	4.75	—	5.25	V
Ripple Voltage (V_{CC})	V_{RP}	—	—	0.1	V

8.ELECTRIC SPECIFICATION

The electric specification for this module is shown in Table 8-1 and measurement circuit is shown in Figure 8-1.

The equivalent circuit of the logic signal input section is shown in Figure 8-2 (A).

The equivalent circuit of the power supply input section is shown in Figure 8-2 (B)

Table 8-1 Electric Specification

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Differential Input Voltage (+)	V_{IH}	$V_{CM}=+1.2V$	—	—	100	mV	
Differential Input Voltage (-)	V_{IL}		-100	—	—	mV	
HRCOFF,SELLVDS,PD Signal Input H level	V_{IHDP}	$V_{CC}=+5\pm 0.25V$ $V_{SS}=0V$ DCLK=54MHz $T_a=25^\circ C$	2.0	—	3.3	V	
HRCOFF,SELLVDS,PD Signal Input L level	V_{ILDP}		0	—	0.8	V	
Power Supply Current	I_{CC}		—	520	1200	mA	*1

(*1) The TYP value is when the vertical stripe color bar is displayed. $V_{CC}=5.0V$

The MAX value is when 2-pixel checker is displayed. $V_{CC}=4.75V$, exclude irruption current. (Exclude the Current value of the LCD module)

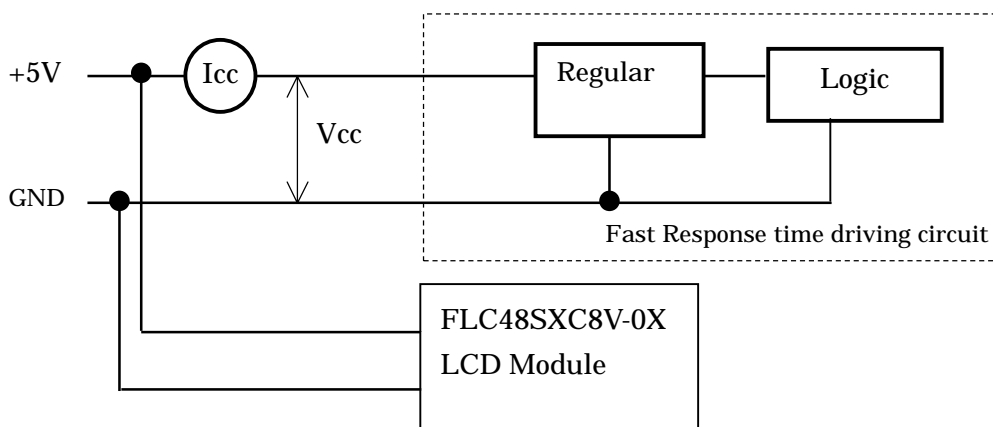


Figure 8-1 Measuring Circuit

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9. INTERFACE SPECIFICATION

9.1 Interface Signal Alignment and Connector

The signal alignment of the interface connector (CN1, CN2) is shown in Table 9-1.

Table 9-1 Interface connector (CN1, CN2) signal alignment

Input connector (CN1)				Output connector (CN2)			
Pin No.	Signal	I/O	Function	Function	I/O	Signal	Pin
1	RxO0-	I	LVDS input signal (O0-)	LVDS output signal (O0-)	O	RxO0	30
2	RxO0+	I	LVDS input signal (O0+)	LVDS output signal (O0+)	O	RxO0	29
3	RxO1-	I	LVDS input signal (O1-)	LVDS output signal (O1-)	O	RxO1	28
4	RxO1+	I	LVDS input signal (O1+)	LVDS output signal (O1+)	O	RxO1	27
5	RxO2-	I	LVDS input signal (O2-)	LVDS output signal (O2-)	O	RxO2	26
6	RxO2+	I	LVDS input signal (O2+)	LVDS output signal (O2+)	O	RxO2	25
7	GND	—	Ground	Ground	—	GND	24
8	RxOC-	I	LVDS input signal (OC-)	LVDS output signal (OC-)	O	RxO	23
9	RxOC+	I	LVDS input signal (OC+)	LVDS output signal (OC+)	O	RxO	22
10	RxO3-	I	LVDS input signal (O3-)	LVDS output signal (O3-)	O	RxO3	21
11	RxO3+	I	LVDS input signal (O3+)	LVDS output signal (O3+)	O	RxO3	20
12	RxE0-	I	LVDS input signal (E0-)	LVDS output signal (E0-)	O	RxE0	19
13	RxE0+	I	LVDS input signal (E0+)	LVDS output signal (E0+)	O	RxE0	18
14	GND	—	Ground	Ground	—	GND	17
15	RxE1-	I	LVDS input signal (E1-)	LVDS output signal (E1-)	O	RxE1	16
16	RxE1+	I	LVDS input signal (E1+)	LVDS output signal (E1+)	O	RxE1	15
17	GND	—	Ground	Ground	—	GND	14
18	RxE2-	I	LVDS input signal (E2-)	LVDS output signal (E2-)	O	RxE2	13
19	RxE2+	I	LVDS input signal (E2+)	LVDS output signal (E2+)	O	RxE2	12
20	RxEC-	I	LVDS input signal (EC-)	LVDS output signal (EC-)	O	RxEC	11
21	RxEC+	I	LVDS input signal (EC+)	LVDS output signal (EC+)	O	RxEC	10
22	RxE3-	I	LVDS input signal (E3-)	LVDS output signal (E3-)	O	RxE3	9
23	RxE3+	I	LVDS input signal (E3+)	LVDS output signal (E3+)	O	RxE3	8
24	GND	—	Ground	Ground	—	GND	7
25	SELLVDS	I	Select LVDS data alignment*1	Ground	—	GND	6
26	PD	I	LVDS control signal		O	PD	5
27	HRCOFF	I	Fast response function control*2	Open	—	TST	4
28	Vcc	—	+5V	+5V	—	Vcc	3
29	Vcc	—	+5V	+5V	—	Vcc	2
30	Vcc	—	+5V	+5V	—	Vcc	1

Used connector : FI-X30S-HF (Japan Aviation Electronics Industry Ltd.)

Applied connector : FI-X30M (FPC type) (Japan Aviation Electronics Industry Ltd.)

FI-X30H (Wire type)

FI-X30C (Co-axial cable type)

Note *1: Refer to item 9.2 for data alignment, the data alignment for CN2 output is the alignment of SELLVDS="L"

*2: The fast response function is OFF at "H". Refer to item 9.4 for change over of timing.

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9. 2. Correspondence of LVDS Data

The correspondence of LVDS data is shown in Table 9-2.

Table 9-2 LVDS data signal alignment

Input signal *1			Transmitter DS90CF383,C385		Interface connector			Receiver DS90CF386		LCD input (SELLVDS)				
SELL LVDS	Low	High	pin	INPUT	System side	LCD module		pin	OUTPUT	Low	High			
						pin								
LVDS Odd	RO2	RO0	51	TxIN0	Tx OUT0+	2	RxO0+	27	RxOUT0	RO2	RO0			
	RO3	RO1	52	TxIN1				29	RxOUT1	RO3	RO1			
	RO4	RO2	54	TxIN2				30	RxOUT2	RO4	RO2			
	RO5	RO3	55	TxIN3				32	RxOUT3	RO5	RO3			
	RO6	RO4	56	TxIN4				33	RxOUT4	RO6	RO4			
	RO7	RO5	3	TxIN6	Tx OUT0-	1	RxO0-	35	RxOUT6	RO7	RO5			
	GO2	GO0	4	TxIN7				37	RxOUT7	GO2	GO0			
	GO3	GO1	6	TxIN8				38	RxOUT8	GO3	GO1			
	GO4	GO2	7	TxIN9				39	RxOUT9	GO4	GO2			
	GO5	GO3	11	TxIN12				43	RxOUT12	GO5	GO3			
	GO6	GO4	12	TxIN13	Tx OUT1+	4	RxO1+	45	RxOUT13	GO6	GO4			
	GO7	GO5	14	TxIN14				46	RxOUT14	GO7	GO5			
	BO2	BO0	15	TxIN15				47	RxOUT15	BO2	BO0			
	BO3	BO1	19	TxIN18				51	RxOUT18	BO3	BO1			
	BO4	BO2	20	TxIN19				53	RxOUT19	BO4	BO2			
	BO5	BO3	22	TxIN20	Tx OUT2+	6	RxO2+	54	RxOUT20	BO5	BO3			
	BO6	BO4	23	TxIN21				55	RxOUT21	BO6	BO4			
	BO7	BO5	24	TxIN22				1	RxOUT22	BO7	BO5			
	RSVD	RSVD	27	TxIN24				3	RxOUT24	Not use	Not use			
	RSVD	RSVD	28	TxIN25				5	RxOUT25	Not use	Not use			
	ENAB	ENAB	30	TxIN26	Tx OUT2-	5	RxO2-	6	RxOUT26	ENAB	ENAB			
	RO0	RO6	50	TxIN27				7	RxOUT27	RO0	RO6			
	RO1	RO7	2	TxIN5				34	RxOUT5	RO1	RO7			
	GO0	GO6	8	TxIN10				41	RxOUT10	GO0	GO6			
	GO1	GO7	10	TxIN11				42	RxOUT11	GO1	GO7			
BO0	BO6	16	TxIN16	Tx OUT3+	11	RxO3+	49	RxOUT16	BO0	BO6				
BO1	BO7	18	TxIN17				50	RxOUT17	BO1	BO7				
RSVD	RSVD	25	TxIN23				2	RxOUT23	Not use	Not use				
DCLK			31				TxCLK IN	TxCLK OUT+	9	RxCLK IN+	26	RxCLK OUT	DCLK	
								TxCLK OUT-	8	RxCLK IN-				
LVDS Even	RE2	RE0	51	TxIN0	Tx OUT0+	13	RxE0+	27	RxOUT0	RE2	RE0			
	RE3	RE1	52	TxIN1				29	RxOUT1	RE3	RE1			
	RE4	RE2	54	TxIN2				30	RxOUT2	RE4	RE2			
	RE5	RE3	55	TxIN3				32	RxOUT3	RE5	RE3			
	RE6	RE4	56	TxIN4				33	RxOUT4	RE6	RE4			
	RE7	RE5	3	TxIN6	Tx OUT0-	12	RxE0-	35	RxOUT6	RE7	RE5			
	GE2	GE0	4	TxIN7				37	RxOUT7	GE2	GE0			
	GE3	GE1	6	TxIN8				38	RxOUT8	GE3	GE1			
	GE4	GE2	7	TxIN9				39	RxOUT9	GE4	GE2			
	GE5	GE3	11	TxIN12				43	RxOUT12	GE5	GE3			
	GE6	GE4	12	TxIN13	Tx OUT1+	16	RxE1+	45	RxOUT13	GE6	GE4			
	GE7	GE5	14	TxIN14				46	RxOUT14	GE7	GE5			
	BE2	BE0	15	TxIN15				47	RxOUT15	BE2	BE0			
	BE3	BE1	19	TxIN18				51	RxOUT18	BE3	BE1			
	BE4	BE2	20	TxIN19				53	RxOUT19	BE4	BE2			
	BE5	BE3	22	TxIN20	Tx OUT2+	19	RxE2+	54	RxOUT20	BE5	BE3			
	BE6	BE4	23	TxIN21				55	RxOUT21	BE6	BE4			
	BE7	BE5	24	TxIN22				1	RxOUT22	BE7	BE5			
	RSVD	RSVD	27	TxIN24				3	RxOUT24	Not use	Not use			
	RSVD	RSVD	28	TxIN25				5	RxOUT25	Not use	Not use			
	RSVD	RSVD	30	TxIN26	Tx OUT2-	18	RxE2-	6	RxOUT26	Not use	Not use			
	RE0	RE6	50	TxIN27				7	RxOUT27	RE0	RE6			
	RE1	RE7	2	TxIN5				34	RxOUT5	RE1	RE7			
	GE0	GE6	8	TxIN10				41	RxOUT10	GE0	GE6			
	GE1	GE7	10	TxIN11				42	RxOUT11	GE1	GE7			
BE0	BE6	16	TxIN16	Tx OUT3+	23	RxE3+	49	RxOUT16	BE0	BE6				
BE1	BE7	18	TxIN17				50	RxOUT17	BE1	BE7				
RSVD	RSVD	25	TxIN23				2	RxOUT23	Not use	Not use				
DCLK			31				TxCLK IN	TxCLK OUT+	21	RxCLK IN+	26	RxCLK OUT	Not use	
								TxCLK OUT-	20	RxCLK IN-				

*1 •Connect the RSVD (reserved) pin of the transmitter side to the ground.

•The odd numbers and even numbers of the input data should be inputted according to the display position of the LCD.

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9. 3. CORRESPONDENCE OF INPUT SIGNAL AND COLOR

The correspondence of input signal and color is shown in Table 9-3.

Table 9-3 Correspondence of Input and Signal and Color

Color and Brightness Gradation		Data Signal (0:Low level, 1:High level)																											
		RO RE 7	RO RE 6	RO RE 5	RO RE 4	RO RE 3	RO RE 2	RO RE 1	RO RE 0	GO GO 7	GO GO 6	GO GE 5	GO GE 4	GO GE 3	GO GE 2	GO GE 1	GO GE 0	BO BE 7	BO BE 6	BO BE 5	BO BE 4	BO BE 3	BO BE 2	BO BE 1	BO BE 0				
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Dark	2	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	↑	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	Dark	253	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
↓	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Red	255	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	Dark	2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0			
	↑	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	Bright	253	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0			
↓	254	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0				
Green	255	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0				
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1			
	Dark	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0			
	↑	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	↓	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	Bright	253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1			
↓	254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0				
Blue	255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1				

Note 1) Gradation expression : Color (n)..... n indicates the gradation level. The larger the number the brightness becomes higher.

Note 2) Data : 1:“High” level, 0:“Low level”

Note 3) By inputting 8 bit each of red, green, blue of data signal for odd number, even number dot displays, display the 256 gradation individually in red, green and blue. By combining those colors display 16,777,216 colors. The color data consists of total of 48lines, 24 lines each of odd numbers and even numbers

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9. 4. INPUT SIGNAL TIMING CHARACTERISTIC

The timing characteristic of interface is shown in Table 9-4 and Figure 9-1.

Table 9-4 Timing Characteristics (Ta=0~50°C, Vcc=5±0.25V)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Remarks	
DCLK Signal	Frequency (1)	45	—	85	ns	*1	
	Frequency (2)	20	—	85	MHz	*1	
ENAB Signal	Horizontal period	Th	Thd+56	—	Thd+511	Clock Clock	
	Horizontal display period	Thd	512	—	1280		*2
	Vertical period	Tv	Tvd+2200 clock	—	Tvd+10ms	—	
	Vertical frequency recommended area	1/Tv	50	60	61	Hz	*3
Vertical display period	Tvd	—	—	1M/Thd	Line	*4	
	Data enable timing	Tdn	0	0	0	Clock	*5
Signal delay time	Delay timing	Tdly	(32)	(32)	(32)	Clock	
Fast response function control signal	Pulse width Import timing	ThrcH	2	—	—	Clock	*6
		Ttrg		2092		Clock	

- *1) •Frequency (1) indicates the area of the response compensation behavior. Frequency (2) indicates the area of the internal circuit drive. When the frequency moves even within the specification, there is a possibility of disruption to the display.
- *2) •Automatically confirm the enable signal of the H period during the horizontal display cycle. When changing over the horizontal display period, the display may disrupt when changing over.
- *3) •A response compensation is not conducted, if deflected from the area of the recommended number of vertical frequency.
- *4) •1 Each total amount of RGB display data of the vertical cycle should be 1 MBIT and under. When changing over the vertical display cycle, the display may disrupt when changing over.
- *5) •The screen position may be displaced if the cycle of the active data and the ENAB signal of the cycle “H” is not coherent.
- *6) •The fast response function becomes invalid when the fast response function control signal (HRCOFF) is “H”. (Valid when “L” is open)
The condition of HRCOFF is taken in by the Ttrg timing and is reflected in the next vertical cycle.
The timing of Ttrg is from after the fall of the final line of the enable signal to the 2092 clock.

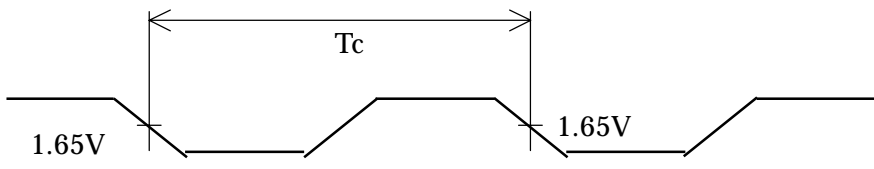
Note) The control signal timing is inputted from CN1 is outputted from CN2 without any changes. It is necessary to meet the timing specification including the connecting LCD module specification.

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A

DCLK

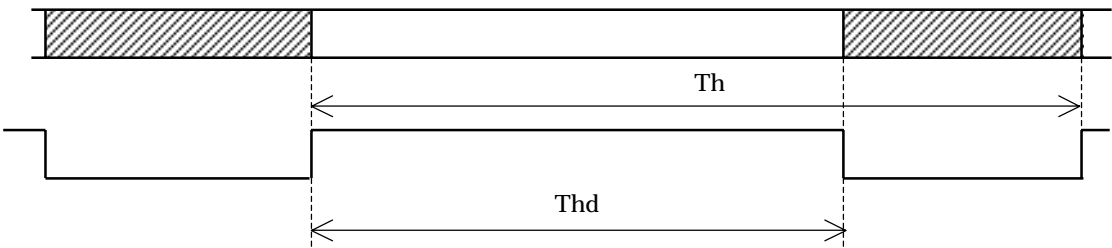


A

B

RO7-0, RE7-0
GO7-0, GE7-0
BO7-0, BE7-0

ENAB

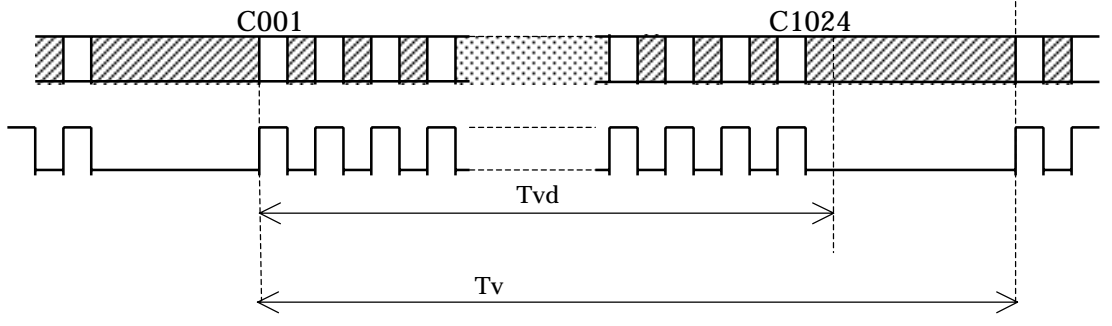


B

C

RO7-0, RE7-0
GO7-0, GE7-0
BO7-0, BE7-0

ENAB



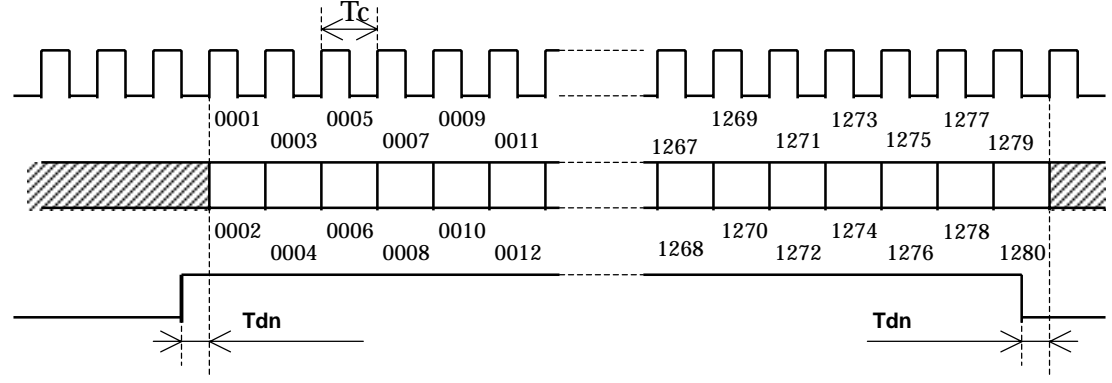
C

D

DCLK

RO7-0, RE7-0
GO7-0, GE7-0
BO7-0, BE7-0

ENAB



D

Figure 9-1 Input Signal Timing Chart

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		11/

F

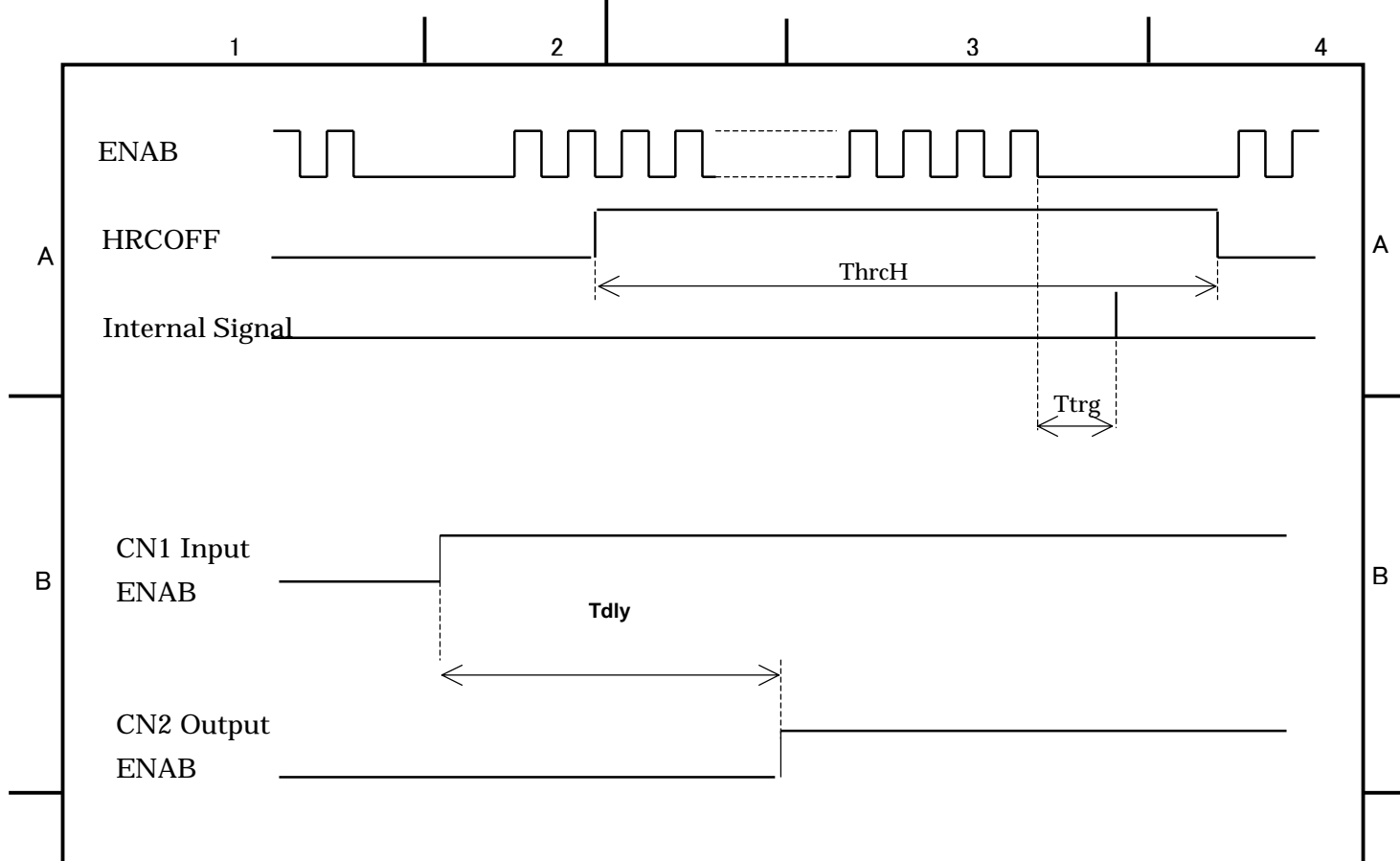


Figure 9-1 Input Signal Timing Chart (Continued)

9.5 CORRESPONDENCE OF DATA AND DISPLAY POSITION

The correspondence of the data and the position display of SXGA are shown in Figure 9-2.

	S000	S000	S000	S000	S000	S000	S000	S000	S383	S384
	1	2	3	4	5	6	7	8		9	0
C001	RO 000 1	GO 000 1	BO 000 1	RE 000 2	GE 000 2	BE 000 2	RO 000 3	GO 000 3		GE 128 0	BE 128 0
C1024	RO 000 1	GO 000 1	BO 000 1	RE 000 2	GE 000 2	BE 000 2	RO 000 3	GO 000 3		GE 128 0	BE 128 0

Figure 9-2 Correspondence of Data and Display Position

DOCUMENT CONTROL SECTION

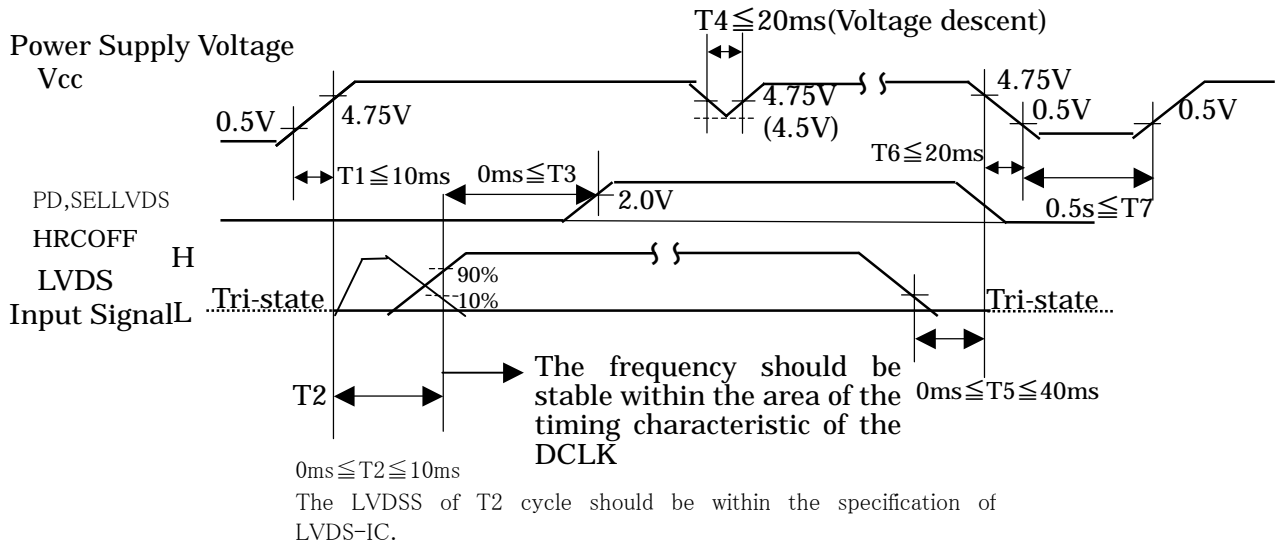
DATE

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						FUJITSU DISPLAY TECHNOLOGIES CORPORATION			DATE	12/	
EDIT	DATE	DESIG.	CHECK	APPR.	DESCRIPTION						
DESIG.			CHECK		APPR.						

9.6 ELECTRIC POWER/SIGNAL SEQUENCE

Figure 9-3 regulates the build up time for the power supply, instant voltage decent and the power supply sequence. The power supply and the sequence of the input signal is especially necessary to prevent direct current drive against the panel and to prevent latch up of the driver IC.

In addition, the sequence of the DCLK·PD·ENAB is regulated in Figure 9-4. If the DCLK is outside the specification after the build up of the power supply and signal, when conducting a PD signal control and when changing over mode, then it becomes necessary.



Note : The use of NC is possible when PD signal is not in use

Figure 9-3 Power Supply Sequence

A: Within the specification of DCLK and PD=H (or OPEN)
 B: Outside the specification of DCLK or PD=L

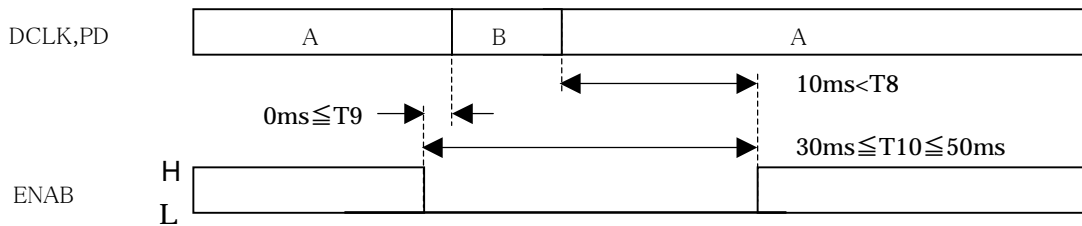


Figure 9-4-1 Signal Sequence (DCLK.PD)

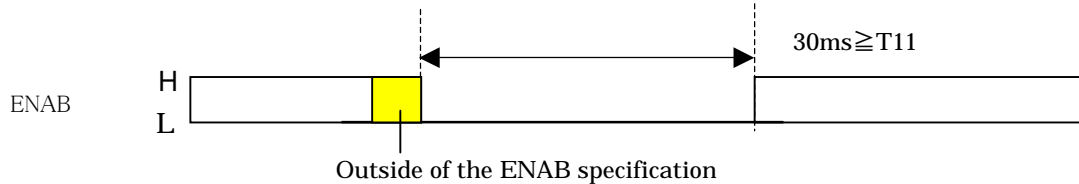


Figure 9-4-2 Signal Sequence (ENAB)

DOCUMENT CONTROL SECTION

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DESIG.			CHECK		APPR.						

10. ENVIRONMENT SPECIFICATION

Environment Specification is shown in Table 10-1.

Table 10-1 Environmental Specification

Item	Condition	Remarks
Temperature area of Compensation Driving	16~48°C	The temperature difference between the center of the display surface and the temperature sensor (refer to outline drawing M20, P21) Response compensation drive is not to be conducted when outside of area. Note 1
Operating Temperature	0~55°C	Surrounding Temperature. Data that exceed the area of the compensation driving temperature is considered as through.
Temperature difference	0±2°C	The temperature difference between the center of the display surface and the temperature sensor (refer to outline drawing M20, P21) When outside of area, the temperature is deflected from the applied compensation.
Storage Temperature	-20~60°C	Surrounding Temperature
Humid	Operation	The maximum wet bulb temperature should not exceed 29°C. There should be no condensation.
	Storage	

Note 1) The effect of the compensation drive is minimum when the area of the compensation driving temperature is low as the response speed of the liquid crystal declines noticeably.

If the temperature is high there is no need for a compensation drive, as the response speed of the liquid crystal increases and there is no need for response compensation outside the area.

Note 2) The standard for shock resistance when packaging is shown in Table 10-2 and Figure 10-1.

Table 10-2 Shock resistance Standard when Packaging

Contact point	Dropping height	No. of times
A~J	60cm	1 time each

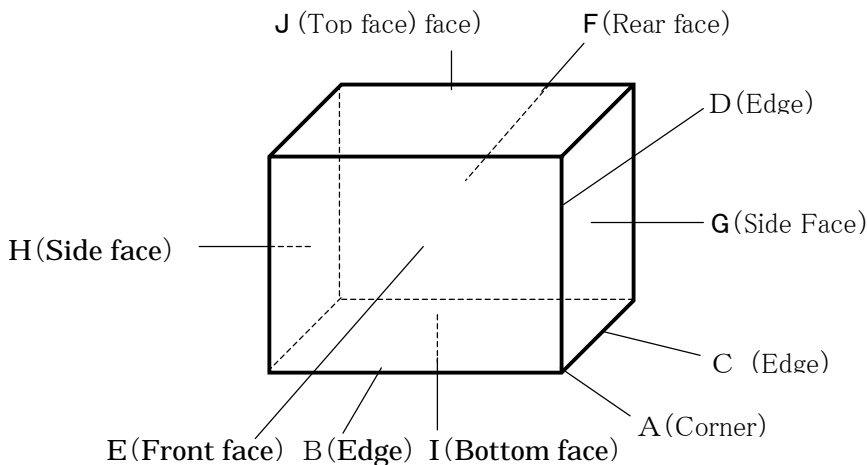


Figure 10-1 The direction of applying shock when packaging

DOCUMENT CONTROL SECTION

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11. INDICATION

The module has the following indications

- (1) Product name : FLCB-12 (Laser Marking or Magic Marker)
- (2) Product drawing No: NA19002-4243 (Laser Marking or Magic Marker)
- (3) Manufacturing No.: 2 Y 0 0 0 0 1 (Laser Marking or Sticker)
 - Ser.No.(Reset every month, reset in a day)
 - Manufacturing month (Oct.=X, Nov=Y, Dec.=Z)
 - Last digit of manufacturing year
- (4) Version No. : 008 A G (Eg.) (Laser Marking or Magic Marker)
 - Operation digits (Renewed when function is revised: AC, AD)
 - Operational version (there are no changes made to functions but is renewed when method of operation is revised)
- (5) Manufacturing Country Name : MADE IN JAPAN (Silk)
- (6) Company Name : FUJITSU DISPLAY TECHNOLOGIES CORP. (Silk)

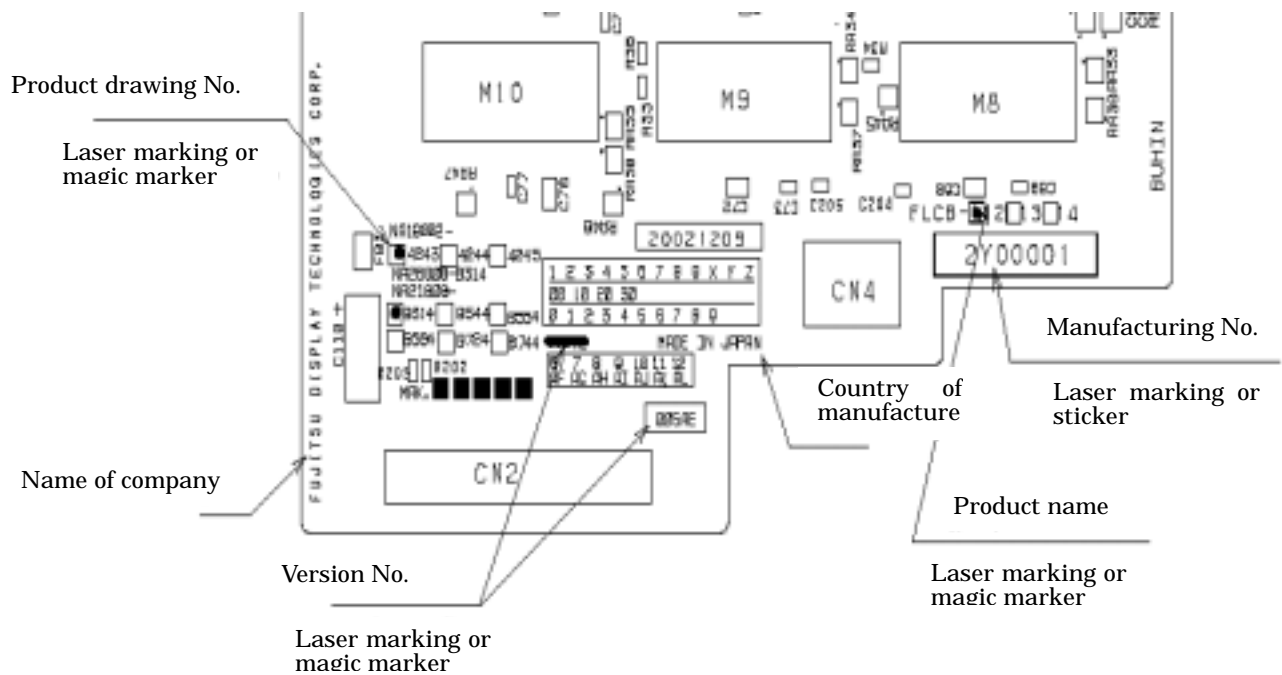


Figure 11-1 Indication

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							CUST.	
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DESIG.			CHECK	APPR.	FUJITSU DISPLAY TECHNOLOGIES CORPORATION			

12. PACKAGING SPECIFICATION

A

- (1) No. of packages : 100pcs/per box
- (2) Weight : 9kg/ per box
- (3)Packaging outline : 493mm(W)×555mm(D)×195mm(H)
- (4)Packaging method : shown in Figure 12-1.

A

Place the product in to the air cap.

B



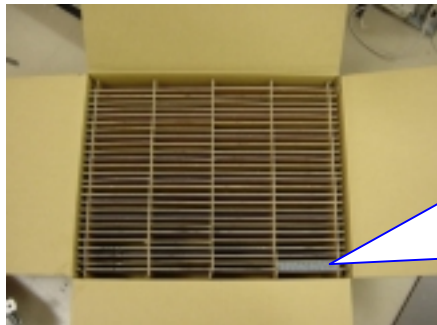
B

Tape with a masking tape

C

Place the product in partition.

C



D



D

Figure 12-1 (a) Packaging Method

E

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DATE

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F

Description of label

型番(TYPE) : FLCB-12
 図番(DRWG.No.) : NA19002-4243
 数量(QTY.) : 100
 版数(REV.No.) : 008AG
 20030115 (Date)
 FUJITSU DISPLAY TECHNOLOGIES CORP.
 MADE IN JAPAN



Figure 12-1 (b)

13. WARRANTY

The warranty period is one year after shipping. Any products that fail during this period is replaced or repaired without charge, unless failure is caused by the user.

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14. CAUTION WHEN IN USE OF PRODUCT

For proper use of the LCD module, please abide by the following precautions.

(1) Fail Safe Design

Failure of the unit may occur at some probability. Please design a safe module for when the module fails to prevent physical damage, fire accidents, any damages that can be caused to the public by conducting a lengthy design for the customers device, design to prevent over current and malfunction.

(2) Handling of the LCD Module

Take anti-electrostatic measures when assembling the module

The LCD unit contains a CMOS-IC. The following points should be taken into consideration.

- General anti-electrostatic should be taken when handling instruments.
(Cotton or conductive gloves should be worn/grounding worker/disposal of ground on floor, operating table etc./ disposal of operating tools (soldering iron, radio pliers, tweezers, etc.) etc.)
- Do not take the module out of the conductive bag until assembling the module.
- Assemble the module under a humid controlled environment (50 – 60%RH).
Do not handle the module under the humid of 50%RH.

(3) Precautions to be made when operating the LCD module

①Please abide by the specified power supply sequence

The purpose of this is to prevent latch up the CMOS-IC.

②Do not input signal and power supply when condensation occurs

③In regards to emphasis display of the high response function

Depending on the use condition of the device, the data change can be emphasized depending on the fast response function

Eg.

- If there are data changes due to noises of the analog signal in regards to the analog input device.
- If FRC and designing etc. are used.

DATE DOCUMENT CONTROL SECTION

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(4) Storage Method

① Do not leave the LCD module in an organic solvent or corrosive gas environment

• Various parts of the module may corrode or deteriorate in a corrosive gas environment.

② Please store the LCD module in a FDTC

• The LCD module within the packaging box is covered in anti-static bag.

③ The LCD module is recommended to be stored in a humidity controlled, cool and dark place

Recommended storage environment:

• Place: Dark (avoid direct sunlight)

• Temperature: 10~35°C

• Humidity: 50~60°C

(5) Return method for LCD modules when requesting for repair or analysis of the problem

• When returning the LCD module, please follow the regular packaging procedure

Please note that FDTC will not take any responsibility for damaged LCD modules that are returned where the reason for damage is due to failure of following the specified packaging procedures.

• When using packaging container other than the FDTC container

Pack each module in separate air caps etc. so that there will be no damages made to the LCD module during shipment. We will not take any responsibility for damages that are caused by failure of packaging.

(6) Others

Some residue may be left on the print substrate of this LCD module but is not a problem

We have implemented a non-washing method for the process of mounting parts.

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	DESIG.		CHECK		APPR.				

15. PRECAUTION

This product has been designed and manufactured for the purpose of general use such as general office, personal, household and usual industrial use. Therefore, as this module is not designed for devices that require extremely high safety such as nuclear reaction control, aerospace, air traffic control, traffic control of mass shipping system, life sustaining medical equipment and military system that controls the launch of missiles, if safety that is in question is not obtained, please do not use this product as a device that require high safety as this product is not designed for such purpose where it can cause direct hazard to life and the human body. Any customers that have a possibility that their device may fall into the category of high safety use, then please consult the sales group in advance. We will not be responsible for any claims from the customers or a third party or any compensation for damages that is due to customers using the product as high safety without prior notice.

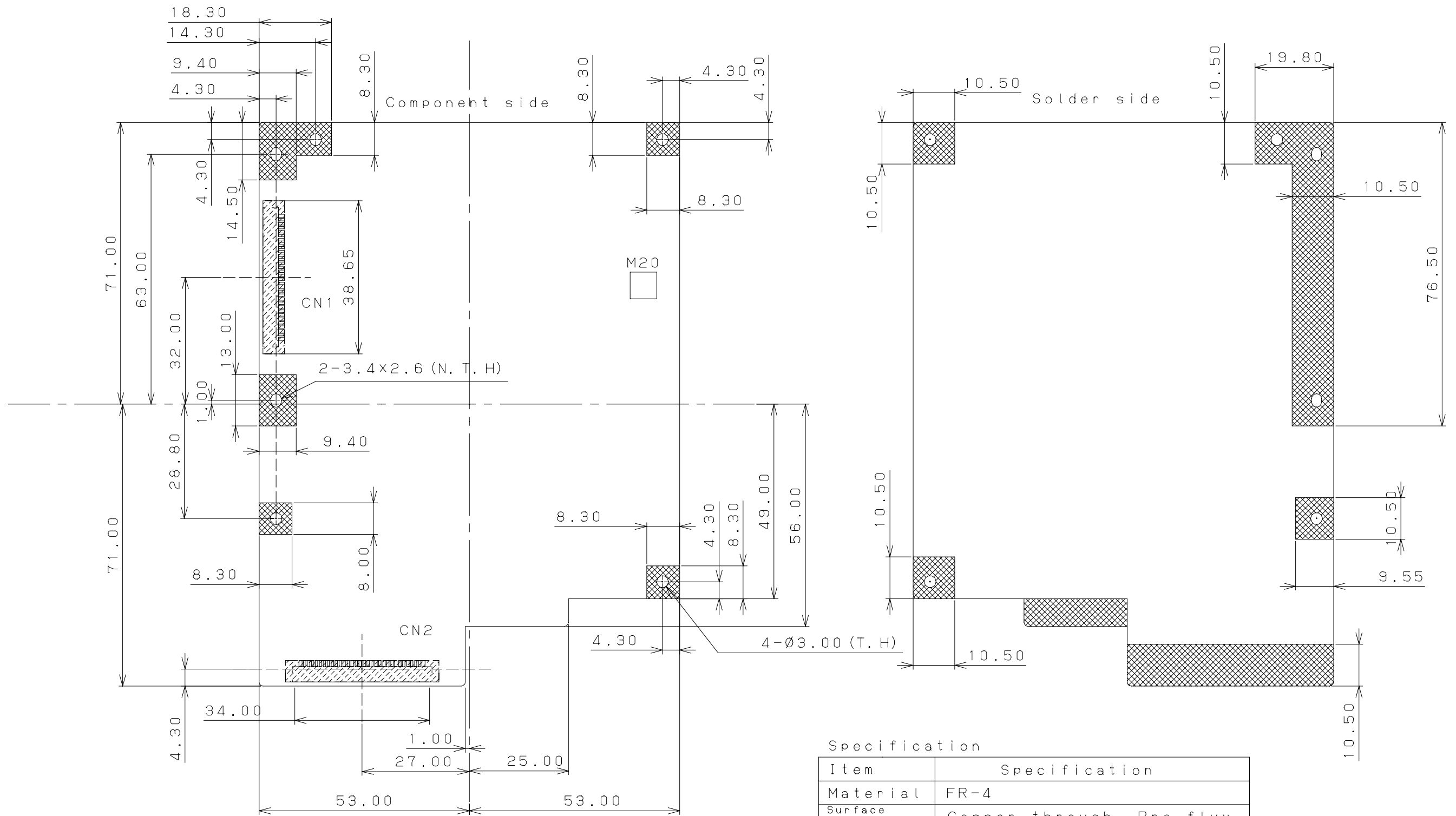
16. OTHERS

There may be changes made to the parts used in this LCD module. In those cases, a discussion will be made in advance between both parties regarding the changes that will be made to the parts.

In addition, if any doubts arise in regards to descript items in the specification, that problem should be resolved through discussion between both parties.

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	DESIG.		CHECK			APPR.			



Outline Drawing

Specification

Item	Specification
Material	FR-4
Surface treatment	Copper through Pre-flux
Thickness	t=0.8mm (TYP)
Height of mounting	4.5mm MAX (M4)

Note) The only contact point to the device side shall be area FG.

 FG area

EDIT.	DATE	DESIG.	CHECK	DESCRIPTION	TITLE	Fast Response Time
					Driving Circuit Specification	
					DRAW. NO.	
					Tech Bes LCD-00205	
DESIG.			CHECK		APPR.	