INNOLUX DISPLAY CORPORATION

LCD MODULE

SPECIFICATION

Customer:_____

Model Name: <u>AT070TN06</u> SPEC NO: <u>A070-06-TT-02</u> Date: Dec., 2004 Version:<u>2</u>

Preliminary Specification

Final Specification

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepare by
「一」「「「「「	黄郁花、杨白	月山平

InnoLux copyright 2003 All rights reserved, Copying forbidden.

Innolux Display Corporation, No.160 Kesyue Rd,, Chu-Nan Site, Hsinchu Science Park, Chu-Nan 350,Miao-Li County, Taiwan Tel: 886-37-586000 Fax: 886-37-586060

InnoLux copyright 2004 All rights reserved, Copying forbidden.

Record of Revision

Version	Revise Date	Page	Content
1	2004/12/06		Initial Release
2	2004/12/27	16	Update Mechanical dimensions

Contonte

	General Specification	2
	Electrical Specifications	2
	(1). Absolute maximum ratings	
	(2). Pin assignment	
	(a). TFT LCD panel driving section	
	(b). Backlight Unit	
	(3). Electrical characteristics	
	(a). Typical operating conditions	
	(b). Current consumption	
	(c). Backlight driving conditions	
	(4). AC timing	
	(a). Timing conditions	
	(b). Timing diagram	
3.	Optical Specifications	11
4.	Reliability Test Items	15
5.	Handling Precautions	16
	(1).Safety	
	(2). Handling	
	(3). Static electricity	
	(4). Storage	
	(5). Cleaning	
6.	Mechanical Dimensions	17

7. Packing Specifications 18

1. General Specifications

NO.	Item	Specification	Remark
1	LCD size	7.0 inch	
2	Driver element	a-Si TFT active matrix	
3	Resolution	480X3(RGB)X234	
4	Display mode	Normally white, Transmissive	
5	Dot pitch	0.107(W) X 0.370(H) mm	
6	Active area	154.08(W) X 86.58(H) mm	
7	Module size	164.9(W) X 100.0(H) X 5.7(D) mm	
8	Surface treatment	Anti-Glare	
9	Weight	160 g	

2. Electrical Characteristics

(1). Absolute maximum ratings

ltem	Symbol	Condition	Values			Remark
item	Symbol		Min.	Max. 🧹	Unit	Rellark
	V _{CC}	GND=0	-0.3	7	V	
	AV_{DD}	AVSS=0	-0.3	7	V	
Power voltage	V _{GH}		-0.3	18	V	
	V _{GL}	GND=0	-15	0.3	V	
	V _{GH} -V _{GL}			33	V	
	Vi)-	-0.3	AV _{DD} +0.3	V	Note 1
Input signal voltage	VI	/ - (-0.3	V _{cc} +0.3	V	Note 2
Operation temperature	Тор		-30	85	°C	
Storage temperature	Tst		-30	85	°C	

Note:

1. VR, VG, VB.

2. STHL, STHR, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.

(2). Pin assignment

(a). TFT LCD panel driving section

Pin no	Symbol	10	Function	Remark
1	GND	Р	Ground for logic circuit	
2	V _{cc}	Р	Supply voltage of logic control circuit for scan driver	
3	V _{GL}	Р	Negative power for scan driver	
4	V _{GH}	Р	Positive power for scan driver	

SPEC NO: A070-06-TT-02 PAGE: 3/19

5 STVR I/O Vertical start pulse Note 1 6 STVL I/O Vertical start pulse Note 1 7 CKV I Shift clock input for scan driver Note 1,2 9 OEV I UP/DOWN scan control input Note 1,2 9 OEV I Output enable control for scan driver 10 VCOM P Common electrode driving signal 11 VCOM P Common electrode driving signal 12 L/R I LEFT/RIGHT scan control Note 1,2 13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver 1 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 20 V _{ccc} P Supply voltage of log				PAGE: 3/19	
7 CKV I Shift clock input for scan driver 8 U/D I UP/DOWN scan control input Note 1,2 9 OEV I Output enable control for scan driver 10 10 VCOM P Common electrode driving signal 11 11 VCOM P Common electrode driving signal 11 12 L/R I LEFT/RIGHT scan control Note 1,2 13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver 11 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 20 V _{cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I A	5	STVR	I/O	Vertical start pulse	Note 1
8 U/D I UP/DOWN scan control input Note 1,2 9 OEV I Output enable control for scan driver Image: Scan scan scan scan scan scan scan scan s	6	STVL	I/O	Vertical start pulse	Note 1
9 OEV I Output enable control for scan driver 10 VCOM P Common electrode driving signal 11 VCOM P Common electrode driving signal 12 L/R I LEFT/RIGHT scan control Note 1,2 13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver 15 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 19 CPH1 I Sampling and shifting clock pulse for data driver 20 V _{cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Red) 23 VG I Alternated video signal (Green)	7	CKV	I	Shift clock input for scan driver	
10 VCOM P Common electrode driving signal 11 VCOM P Common electrode driving signal 12 L/R I LEFT/RIGHT scan control Note 1,2 13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver 1 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 19 CPH1 I Sampling and shifting clock pulse for data driver 20 V _{Cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Green) 23 VG I Alternated video signal (Blue) </td <td>8</td> <td>U/D</td> <td>I</td> <td>UP/DOWN scan control input</td> <td>Note 1,2</td>	8	U/D	I	UP/DOWN scan control input	Note 1,2
11 VCOM P Common electrode driving signal 12 L/R I LEFT/RIGHT scan control Note 1,2 13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver Note 3 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 20 V _{cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Green) 23 VG I Alternated video signal (Blue)	9	OEV	I	Output enable control for scan driver	
12 L/R I LEFT/RIGHT scan control Note 1,2 13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver 1 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 19 CPH1 I Sampling and shifting clock pulse for data driver 20 V _{cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Red) 23 VG I Alternated video signal (Blue)	10	VCOM	Р	Common electrode driving signal	
13 MOD I Sequential sampling and simultaneous sampling setting Note 3 14 OEH I Output enable control for data driver Note 3 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 19 CPH1 I Sampling and shifting clock pulse for data driver 20 V _{cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Green) 23 VG I Alternated video signal (Blue)	11	VCOM	Р	Common electrode driving signal	
13 MOD I sampling setting Note 3 14 OEH I Output enable control for data driver 15 STHL I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver Note 1 18 CPH2 I Sampling and shifting clock pulse for data driver 1 19 CPH1 I Sampling and shifting clock pulse for data driver 1 20 V _{cc} P Supply voltage of logic control circuit for data driver 1 21 GND P Ground for logic circuit 1 22 VR I Alternated video signal (Green) 1 23 VG I Alternated video signal (Blue) 1	12	L/R	I	LEFT/RIGHT scan control	Note 1,2
15STHLI/OStart pulse for horizontal scan lineNote 116STHRI/OStart pulse for horizontal scan lineNote 117CPH3ISampling and shifting clock pulse for data driverNote 118CPH2ISampling and shifting clock pulse for data driver119CPH1ISampling and shifting clock pulse for data driver120V _{cc} PSupply voltage of logic control circuit for data driver221GNDPGround for logic circuit223VGIAlternated video signal (Red)224VBIAlternated video signal (Blue)1	13	MOD	I		Note 3
16 STHR I/O Start pulse for horizontal scan line Note 1 17 CPH3 I Sampling and shifting clock pulse for data driver 1 18 CPH2 I Sampling and shifting clock pulse for data driver 1 19 CPH1 I Sampling and shifting clock pulse for data driver 1 20 V _{cc} P Supply voltage of logic control circuit for data driver 1 21 GND P Ground for logic circuit 1 23 VG I Alternated video signal (Green) 1 24 VB I Alternated video signal (Blue) 1	14	OEH	I	Output enable control for data driver	
17 CPH3 I Sampling and shifting clock pulse for data driver 18 CPH2 I Sampling and shifting clock pulse for data driver 19 CPH1 I Sampling and shifting clock pulse for data driver 20 V _{CC} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Red) 23 VG I Alternated video signal (Blue)	15	STHL	I/O	Start pulse for horizontal scan line	Note 1
17 CPH3 I driver 18 CPH2 I Sampling and shifting clock pulse for data driver 19 CPH1 I Sampling and shifting clock pulse for data driver 20 V _{cc} P Supply voltage of logic control circuit for data driver 21 GND P Ground for logic circuit 22 VR I Alternated video signal (Red) 23 VG I Alternated video signal (Blue)	16	STHR	I/O	Start pulse for horizontal scan line	Note 1
Image:	17	СРНЗ	I		
Image: Constraint of the second state of the seco	18	CPH2	I		
21 GND P Ground for logic circuit 22 VR I Alternated video signal (Red) 23 VG I Alternated video signal (Green) 24 VB I Alternated video signal (Blue)	19	CPH1	Ι		
22 VR I Alternated video signal (Red) 23 VG I Alternated video signal (Green) 24 VB I Alternated video signal (Blue)	20	V _{cc}	Р		
23 VG I Alternated video signal (Green) 24 VB I Alternated video signal (Blue)	21	GND	P	Ground for logic circuit	
24 VB I Alternated video signal (Blue)	22	VR		Alternated video signal (Red)	
	23	VG		Alternated video signal (Green)	
25 AV _{pp} P Supply voltage for analog circuit	24	VB		Alternated video signal (Blue)	
	25	AV _{DD}	Р	Supply voltage for analog circuit	
26 AV _{ss} P Ground for analog circuit	26	AV _{SS}	Р	Ground for analog circuit	

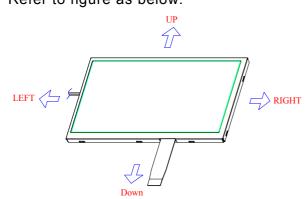
Note:

1. Selection of scanning mode (please refer to the following table)

	of scan I input	IN/C	IN/OUT state for start pulse		Scanning direction	
U/D	L/R	STVR	STVL	STHR	STHL	
GND	V _{cc}	0	Ι	0	Ι	Up to down, left to right
V _{CC}	GND	I	0	I	0	Down to up, right to left
GND	GND	0	Ι	I	0	Up to down, right to left
V _{cc}	V _{cc}	I	0	0	I	Down to up, left to right

I: input, O: output

 Definition of Scanning Direction. Refer to figure as below:



MOD=H: Simultaneous sampling.
 MOD=L: Sequential sampling.

Please set CPH2 and CPH3 to GND when MOD=H,

(b).Backlight unit

Pin no	Symbol	Function	Remark
1	HI	Power supply for backlight unit (high voltage)	Pink
2	GND	Ground for backlight unit	White

(3). Electrical characteristics

(a). Typical operating conditions (GND=AV_{ss}=0V, Note 4)

Item				Values		Remark	
		Symbol	Min.	Тур.	Max.	Unit	Kellark
		V _{cc}	4.8	5	5.2	V	
Deluar	20	AVDD	4.8	5	5.2	V	
Power	supply	V _{GH}	14.3	15	15.7	V	
		V _{GH}	-10.5	-10	-9.5	V	
		V _{iA}	0.4	-	AV _{DD} -0.4	V	Note 1
Video signal a VG,		Viac	/ -	3.5	-	V	AC component
,	,	V_{iDC}	_	$AV_{DD}/2$	-	V	DC component
VCOM		V_{CAC}	3.5	5.5	6.5	V	Note 2
		V_{CDC}	1.55	1.75	1.95	V	DC component
Input signal Voltage	H level	V _{IH}	0.8V _{CC}	-	V _{cc}	V	Nete 2
	L level	V _{IL}	0	-	$0.2V_{CC}$	V	Note 3

Note:

- 1. Refer to Fig.3-(a).
- 2. The brightness of LCD panel could be changed by adjusting the AC component of VCOM.
- 3. SRHL, STHR, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D
- 4. Be sure to apply GND, $V_{CC},$ and $V_{GL},$ to the LCD first, and then apply V_{GH}

SPEC NO: A070-06-TT-02 PAGE: 5/19

				Values	11	Remark	
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
	I _{GH}	V _{GH} =15V	-	0.2	0.5	mA	
Current for driver	I _{GL}	V _{GL} =-10V	-	0.8	1.5	mA	
	I _{cc}	V _{CC} =5V	-	3.0	6.0	mA	
	I _{DD}	AV _{DD} =5V	-	17	30	mA	

(b). Current consumption (GND=AV_{SS}=0V)

(c). Backlight driving conditions

		Values				Remark	
ltem	Symbol	Min. Typ. M		Max.	Unit	Keindik	
Lamp voltage	VL	-	560	620	Vrms	Note 1,6	
Lamp current	١ _L	-	6	7	mArms	Note 6	
Frequency	F_L	-	60	80	kHz	Note 3	
		-		900	Vrms	Note 1,4,6	
Lamp starting voltage	Vs	-	-	1100	Vrms	Note 2,4,6	
Lamp life time		10,000	-)-	Hr	Note 5	

Note:

- 1. Ta=25□
- 2. Ta=0□
- 3. The lamp frequency should be selected as different as possible from display horizontal synchronous signal to avoid interference
- 4. For starting the backlight unit, the output voltage of DC/AC's transformer should be larger than the maximum lamp starting voltage.
- 5. The "lamp life time" is defined as the module brightness decrease to 50% original brightness at Ta=25□, I_L=6mA
- 6. Measure inverter type: HIU-742A, C=11pF, Input Voltage=12.0 Vdc.

(4). AC timing

(a). Timing conditions (sequential mode)

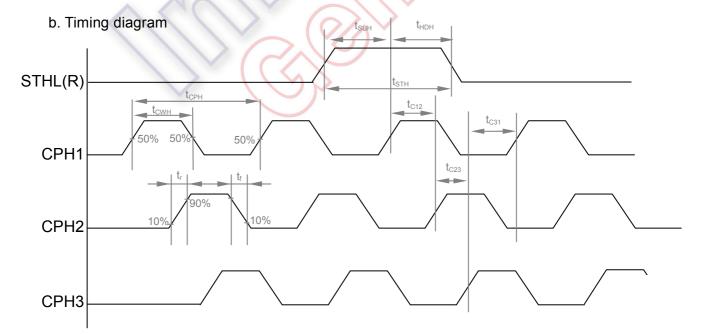
			Values	11	Remark		
Item	Symbol	Min.	Тур.	Max.	Unit		
Rising time	t _r	-	-	10	ns	Note 1	
Falling time	t _f	-	-	10	ns	Note 1	
High and low level pulse width	t _{CPH}	99	103	107	ns	CPH1~CPH3	
CPH pulse duty	t _{cwH}	40	50	60	%	CPH1~CPH3	
CPH pulse delay	t _{C12} t _{C23} t _{C31}	30	t _{CPH} /3	t _{CPH} /2	ns	CPH1~CPH3	

SPEC NO: A070-06-TT-02

				PAGE:	6/19	
STH setup time	t _{sun}	20	-	-	ns	STHR, STHL
STH hold time	t _{HDH}	20	-	-	ns	STHR, STHL
STH pulse width	t _{sth}	-	1	-	t _{CPH}	STHR, STHL
STH period	t _H	61.5	63.5	65.5	$\mu{ m S}$	STHR, STHL
OEH pulse width	t _{OEH}	-	1.22	-	$\mu{f s}$	
Sample and hold disable time	t _{DIS1}	-	8.28		$\mu{ m S}$	
OEV pulse width	t _{OEV}	-	5.40		$\mu{ m S}$	
CKV pulse width	t _{CKV}	-	4.18	-	$\mu{ m S}$	
Clean enable time	t _{DIS2}	-	3.74		$\mu{ m S}$	
Horizontal display start	t _{sH}	-	0	-	t _{CPH} /3	
Horizontal display timing range	t _{DH}	-	1440	-	t _{CPH} /3	
STV setup time	t _{SUV}	400	-	-	ns	STVL, STVR
STV hold time	t_{HDV}	400	-	-	ns	STVL, STVR
STV pulse width	t _{STV}	-	- 4		t _H	STVL, STVR
Horizontal lines per field	t _v	256	262	268	t _H	Note 2
Vertical display start	t _{SV}		3	1-1	tн	
Vertical display timing range	t _{DV}	~	234		tн	
VCOM rising time	t _{rCOM}		~	5	μs	
VCOM falling time	t _{fCOM}		-	5	μs	
VCOM delay time	t _{DCOM}		-	3	μs	
RGB delay time	t _{DRGB}		- <	V1C	μ S	
Noto						

Note:

- 1. For all of the logic signals
- 2. Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.



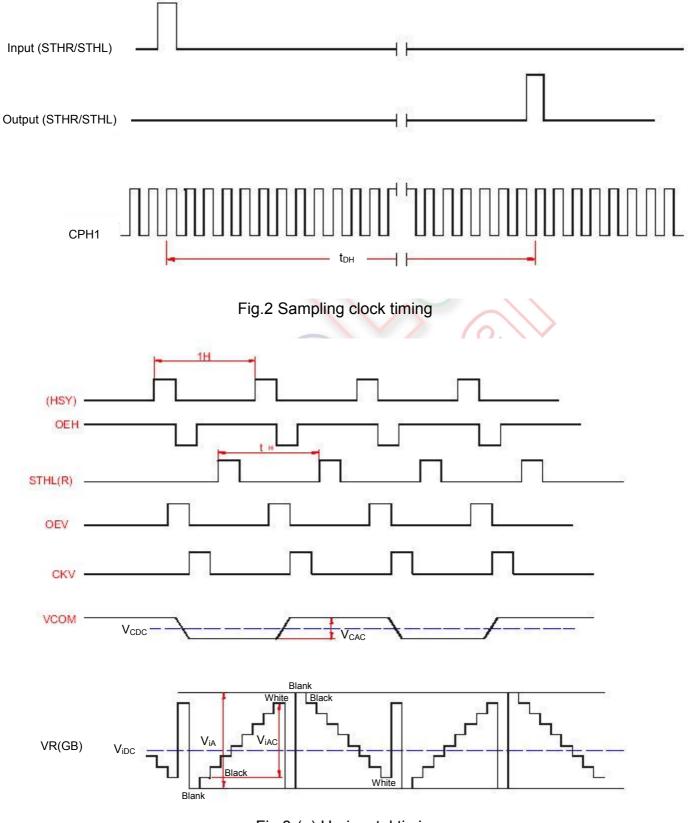
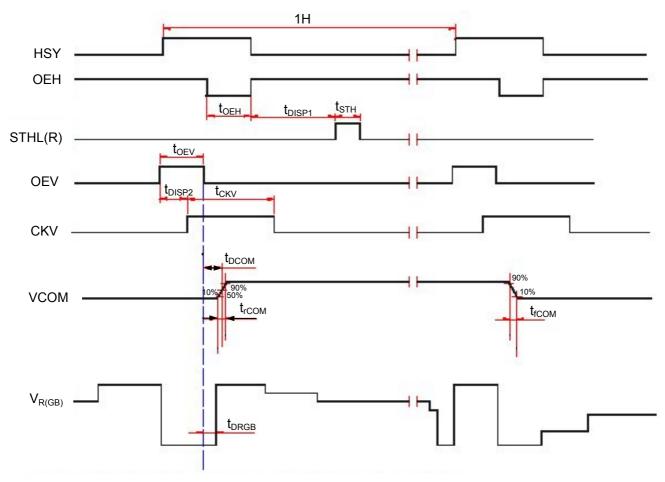


Fig.3-(a) Horizontal timing



Note: The falling edge of OEV should be synchronized with the falling edge of OEH

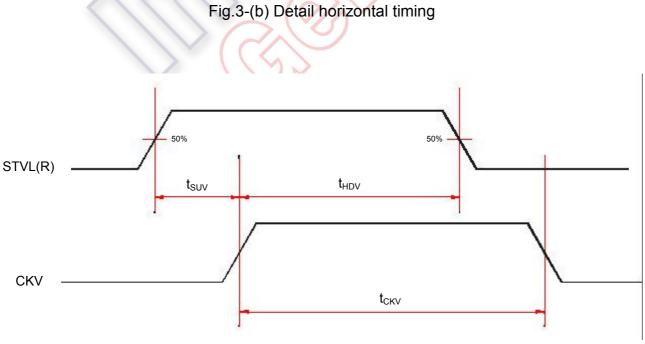
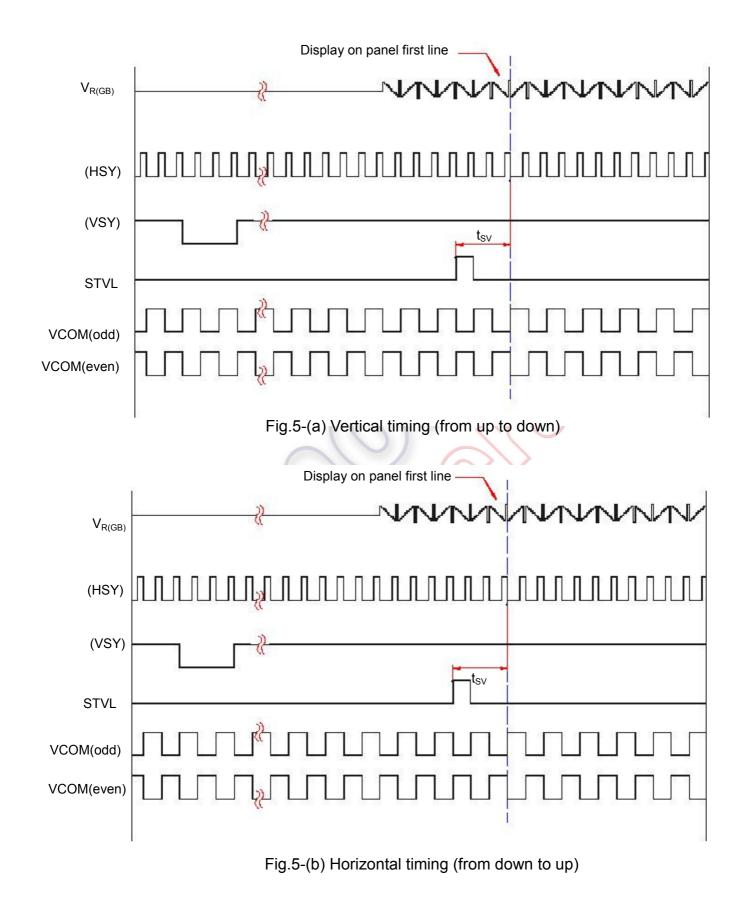
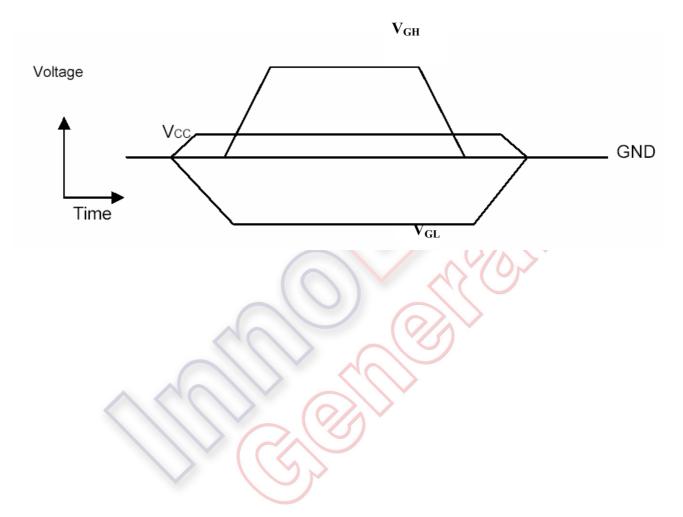


Fig.4 Vertical shift clock timing



(5) Power sequence

This module adopts high voltage driver IC, so it may be damaged by a large current flow if a wrong power on/off sequence is used! The recommend power sequence is to connect V_{CC} first, then connect power to driver gate power, V_{GL} and V_{GH}. When shutting off the power, shut off the driver gate power, V_{GL} and V_{GH}, then shut off the logic power, V_{CC}, or shut off the power simultaneously!



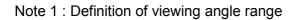
SPEC NO: A070-06-TT-02 PAGE: 11/19

3. Optical Specifications

The following items are measured under stable conditions. The optical characteristics should be measured in dark room or equivalent state.(Note 2)

Item	Symbol	Condition	Min	Тур	Max	Unit	Remark
Response time	T _{on}		-	10	50	ms	Note3
	T _{OFF}		-	20	60	ms	Notes
Contrast ratio	CR	Normal θ=Φ=0°	200	300	-		Note4
Brightness	L		400	500	-	Cd/m ²	Note6
	W _x		0.26	0.31	0.36		Note 5
Color chromaticity	Wy		0.28	0.33	0.38		Note 6 (CIE1931)
Viewing angle (CR≥10)	θι	Φ=180° (9o'clock)	50	60	-	Degree	
	θ_{R}	Φ= 0 ° (3o'clock)	50	60	1		
	θτ	Φ= 90° (12o'clock)	30	40	20	Degree	Note1
	θΒ	Φ=270° (60'clock)	50	60	-		
Luminance uniformity	Yu		70%	75%	-		Note7

Ta=25±2 \Box , I_L=6mA



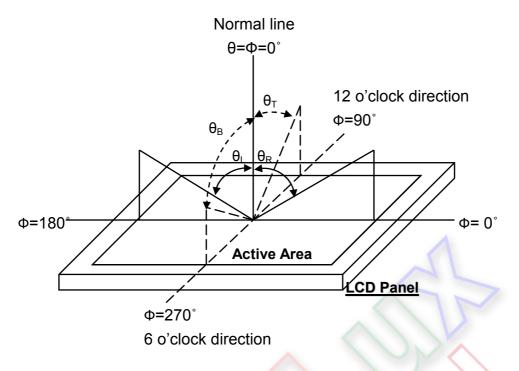
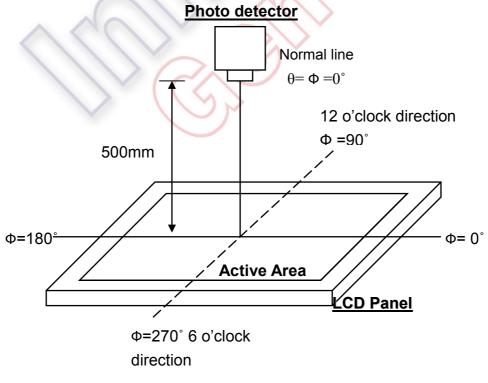


Fig. 5-1 Definition of viewing angle

Note 2 : Definition of optical measurement system.(TFT)

The optical characteristics should be measured in dark room and with ambient temperature $Ta=25^{\circ}C$. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Equipment : Photo detector TOPCON BM-5A or BM-7 /Field of view: 1° /Height: 500mm.)





Note 3 : Definition of Response time.

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (Ton) is the time between photo detector output intensity changed from 90% to 10%. And fall time (Toff) is the time between photo detector output intensity changed from 10% to 90%.

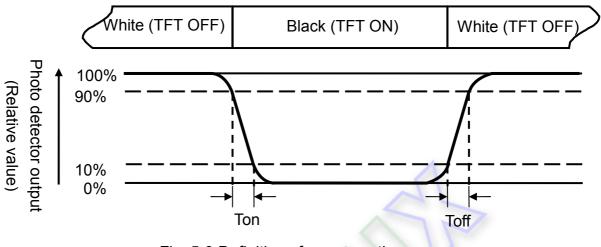


Fig. 5-3 Definition of response time

Note 4: Definition of contrast ratio:

Brightness measured when LCD is at "white"

Contrast ratio (CR) = Brightness measured when LCD is at "black"

White Vi = $Vi_{50\%} \pm 1.5 V$

Black Vi = $Vi_{50\%}$ + 2.0 V

"±"means that the analog input signal swings in phase with VCOM signal.

"+" means that the analog input signal swings out of phase with VCOM signal.

Vi_{50%}: The analog input voltage when transmission is 50%

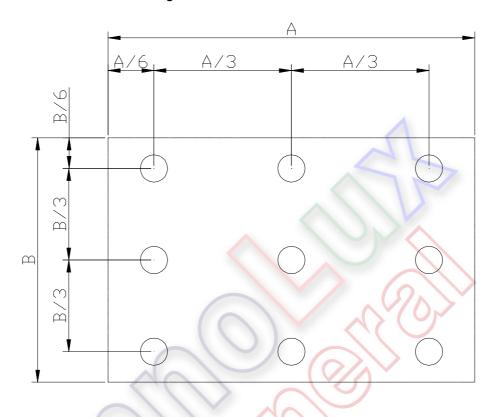
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

- Note 5 : Definition of color chromaticity (CIE1931) Color coordinates measured at the center point of LCD.
- Note 6 : Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Definition of Luminance Uniformity

To test for uniformity, the tested area, which is inside the active area, is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each box.

Luminance Uniformity (Yu) =
$$\frac{B_{min}}{B_{max}}$$



A-----Active area length B----- Active area width

B_{max} : The measured maximum luminance of all measurement position.

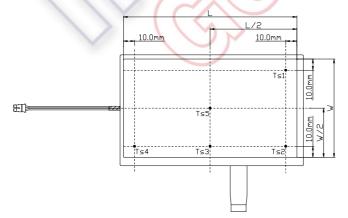
 ${\bf B}_{\rm min}~$: The measured minimum luminance of all measurement position.

4. Reliability Test Items

Test Items	Test Conditions	Remark
High Temperature Storage	Ta = 85 240 hrs	
Low Temperature Storage	Ta = - 30 240hrs	
High Temperature Operation	Ts = 85 240hrs	
Low Temperature Operation	Ta = - 30 240hrs	
Operate at High Temperature and Humidity	+60 ±3, 90%±3%RH max. for 240 hours	
Thermal Shock	-30 /30 min ~ +85 /30 min for a total 100 cycles, Start with cold temp and end with high temp	
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	JIS C7021 A-10 Condition A
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	JIS C7021 A-7 Condition C
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	IEC 68-34
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	JIS Z0202
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	EIA/JESD22-A114

Note: 1. Ta is the ambient temperature of samples.

- 2. Ts is the temperature of panel's surface.
 - Ts=(Ts1+Ts2+Ts3+Ts4+Ts5)/5.



L is the length of Top Bezel open window,

W is the width of Top Bezel open window.

3. In the standard condition, there shall be no practical problem that may affect the display function.

5. Handling Precautions

1 Safety

The liquid crystal in the LCD is poisonous. **DO NOT** put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

2 Handling

1) The LCD panel is plate glass. **DO NOT** subject the panel to mechanical shock or to excessive force on its surface.

2) The polarizer attached to the display is very easy to damage, handle it with careful attention.

3) To avoid contamination on the display surface, **DO NOT** touch the display surface with bare hands.

4) Provide a space so that the LCD panel does not come into contact with other components.

5) To protect the LCD panel from external pressure, put covering glass (acrylic board or similar board) keeping appropriate gap between them.

6) Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where dew condensation occurs.

7) Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in malfunctioning of the ICs.

8)To prevent such malfunctioning of the ICs, your design and mounting layout done are so that the IC is not exposed to light in actual use.

3 Static electricity

- 1) Ground soldering iron tips, tools and testers when you operate.
- 2) Ground your body when handling the products.
- 3) **DO NOT** apply voltage to the input terminal without applying power supply.
- 4) **DO NOT** apply voltage which exceeds the absolute maximum rating.

5) Store the products in an anti-electrostatic container.

4 Storage

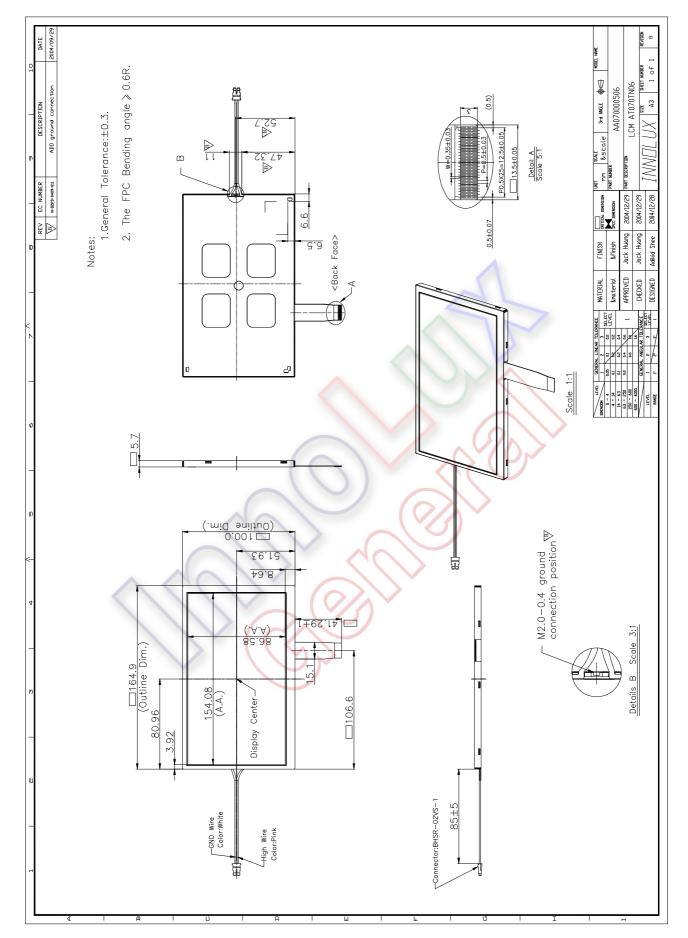
1) Store the products in a dark place at $+25 \pm 10$, low humidity (65%RH or less).

2) **DO NOT** store the products in an atmosphere containing organic solvents or corrosive gases.

5 Cleaning

1) **DO NOT** wipe the polarizer with dry cloth, as it might cause scratch.

2) Wipe the polarizer with a soft cloth soaked with petroleum IPA, other chemical might damage.



6. Mechanical Dimensions

SPEC NO: A070-06-TT-02 PAGE: 17/19

SPEC NO: A070-06-TT-02 PAGE: 18/19

7. Packing Specifications

(1). Packaging material table

Per carton

No.	Item	Model (Material)	Dimensions (mm)	Unit Weight (Kg)	Quantity	Remark
1	LCM module	AT070TN06	164.9*100*5.7	0.160	45	
2	EPP tray	EPP	516*346*26	0.495	9	Anti-static
3	Cover tray	EPP	516*346*26	0.055	1	Anti-static
4	A/S Bag	PE	160*178*0.06	0.1206	45	
4	Carton	Carton	530*355*255	1.1	1	
5	Total weight	8.970 Kg ± 5%		ZL		

(2). Packaging quantity

(1) LCM quantity per tray: 2 row x	x 2 column + 1 row x 1 column = 5	
(2) Total LCM quantity in Carton: 9	x quantity per tray 5 = 45	

(3). Packaging drawing

